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ACPL-344JT

Automotive 2.5 Amp Gate Drive Optocoupler with Integrated IGBT Desat Overcurrent Sensing, Miller Current Clamping and UnderVoltage LockOut Feedback

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

Avago's Automotive 2.5Amp Gate Drive Optocoupler features fast propagation delay with excellent timing skew performance. Smart features that are integrated to protect the IGBT include IGBT desaturation sensing with soft-shutdown protection and fault feedback, under voltage lockout and feedback and active Miller current clamping. This full featured and easy-to-implement IGBT gate drive optocoupler comes in a compact, surface-mountable SO-16 package for space-savings. It is suitable for traction power train inverter, power converter, battery charger, air-con and oil pump motor drives in HEV and EV applications and satisfies automotive AEC-Q100 semiconductor requirements.

Avago R^{2}Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram

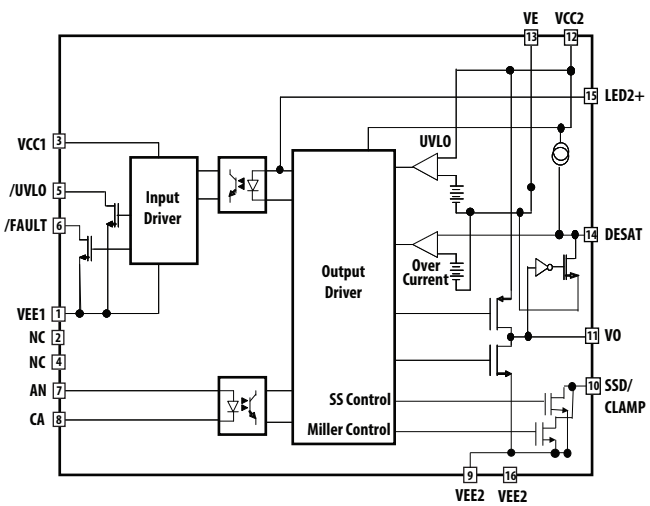


Figure 1. ACPL-344JT Functional Diagram

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- Common Mode Rejection (CMR): > 50 kV/µs at V_{CM} = 1500 V
- High Noise Immunity
  - Miller Current Clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative Gate Bias
- Peak output current: 2.5A max.
- Miller Clamp Sinking Current: 1.9 A max.
- Wide Operating Voltage: 15 V to 25 V
- Propagation delay: 250 ns max.
- Integrated fail-safe IGBT protection
  - Desat sensing, 'Soft' IGBT turn-off and Fault Feedback
  - UnderVoltage Lock-Out protection (UVLO) with Feedback
- SO-16 package with 8 mm clearance and creepage
- Regulatory approvals:
  - UL1577, CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

- Automotive isolated IGBT/MOSFET inverter gate drive
- Automotive DC-DC converter
- AC and brushless DC motor drives
- Industrial inverters for power supplies and motor controls
- Uninterruptible power supplies (UPS)

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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Ordering Information

Part Number	RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-344JT	-000E	SO-16	X		X	45 per tube
ACPL-344JT	-500E		X	X	X	850 per reel

To order, choose a part number from the Part Number column and combine with the desired option from the RoHS Compliant column to form an order entry.

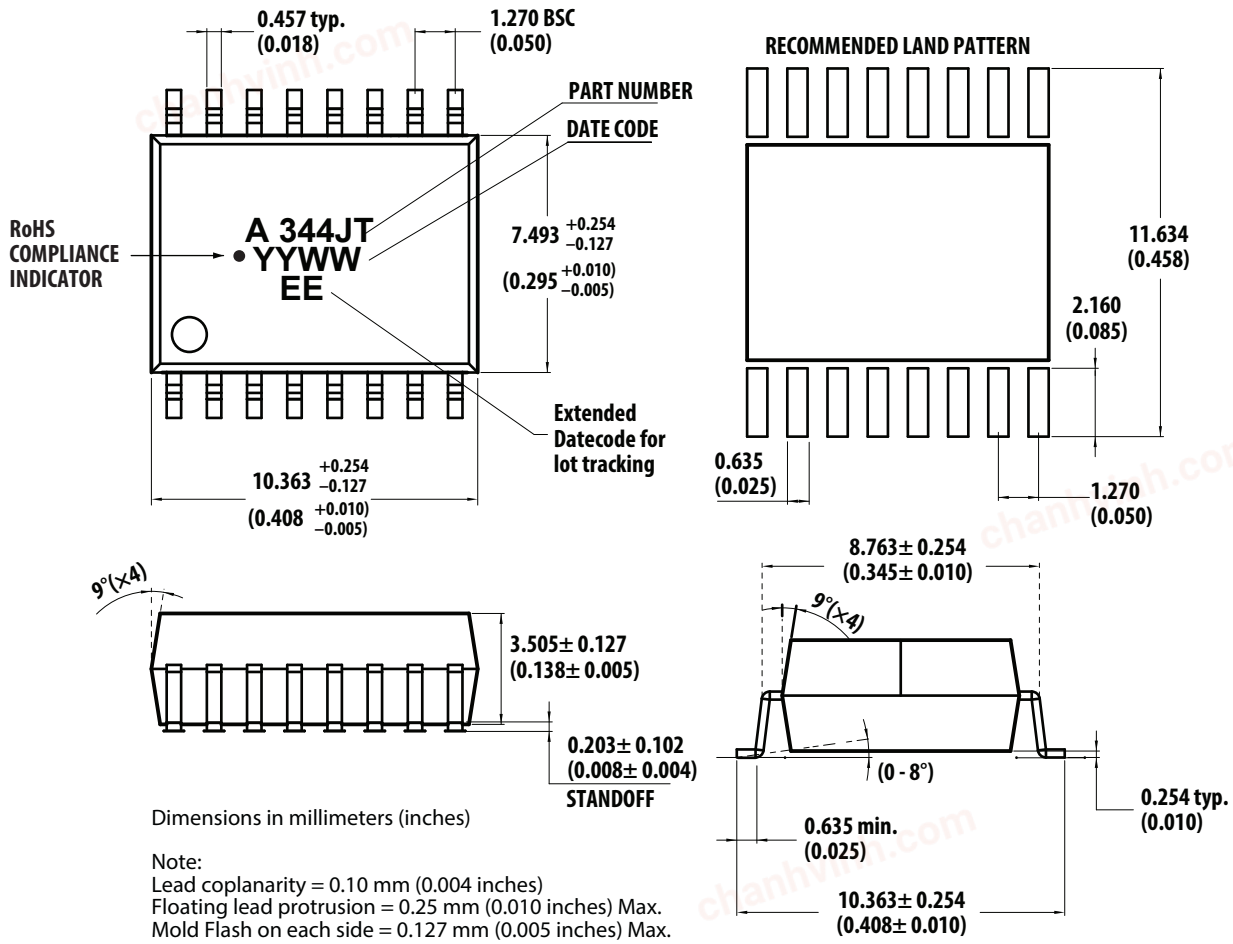
Example 1:

ACPL-344JT-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

16-Lead Surface Mount



Dimensions in millimeters (inches)

Note:
Lead coplanarity = 0.10 mm (0.004 inches)
Floating lead protrusion = 0.25 mm (0.010 inches) Max.
Mold Flash on each side = 0.127 mm (0.005 inches) Max.

Recommended Lead-free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Non-halide flux should be used.

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Product Overview Description

The ACPL-344JT (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit. It features IGBT desaturation sensing with soft-shutdown protection and fault feedback, under voltage lockout and feedback and active Miller current clamping in a SO-16 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increased its noise immunity.

Package Pin Out

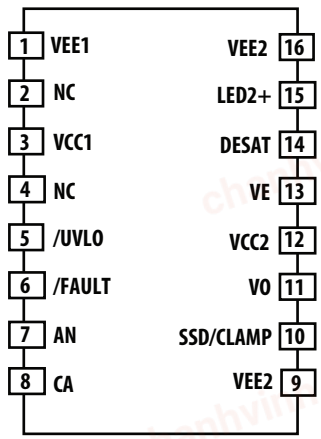


Figure 2. Pin-out of ACPL-344JT

Pin Description

Pin Name	Function	Pin Name	Function
VEE1	Input common	VEE2	Negative power supply
NC	No connection	LED2+	No connection, for testing only
VCC1	Input power supply	DESAT	Desat overcurrent sensing
NC	No connection	VE	IGBT Emitter Reference
/UVLO	VCC2 undervoltage lockout feedback	VCC2	Positive power supply
/FAULT	Overcurrent fault feedback	VO	Driver output to IGBT gate
AN	Input LED anode	SSD/CLAMP	Soft Shutdown/Miller Current clamping output. (For proper functionality, this pin must be connected to the gate of the IGBT directly or through a current buffer.)
CA	Input LED cathode	VEE2	Negative Power Supply

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Typical Application/Operation

Introduction to Fault Detection and Protection

The power stage of a typical three phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase and rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the overcurrent during a fault condition.

A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features which this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

The ACPL-344JT satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shut down, and optically isolated fault and UVLO status feedback signal into a single 16-pin surface mount package.

The fault detection method, which is adopted in the ACPL-344JT, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-344JT limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly- conservative overcurrent threshold is not needed to protect the IGBT.

Recommended Application Circuit

The ACPL-344JT has non-inverting gate control inputs, and an open collector fault and UVLO outputs suitable for wired 'OR' applications.

The recommended application circuit shown in Figure 3 illustrates a typical gate drive implementation using the ACPL-344JT.

The two supply bypass capacitors (0.1 μF) provide the large transient currents necessary during a switching transition. The Desat diode and 220 pF blanking capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10 Ω) serves to limit gate charge current and indirectly control the IGBT collector voltage rise and fall times. The open collector fault and UVLO outputs have a passive 10 kΩ pull-up resistor and a 330 pF filtering capacitor.

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DESAT Fault Detection Blanking Time

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. This time period, called the total DESAT blanking time, is controlled by the both internal DESAT blanking time $t_{DESAT(BLANKING)}$ (Figure 6) and external blanking time, determined by internal charge current, the DESAT voltage threshold, and the external DESAT capacitor.

The total blanking time is calculated in terms of internal blanking time ($t_{DESAT(BLANKING)}$), external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) as

$$t_{BLANK} = t_{DESAT(BLANKING)} + C_{BLANK} \times V_{DESAT}/I_{CHG}$$

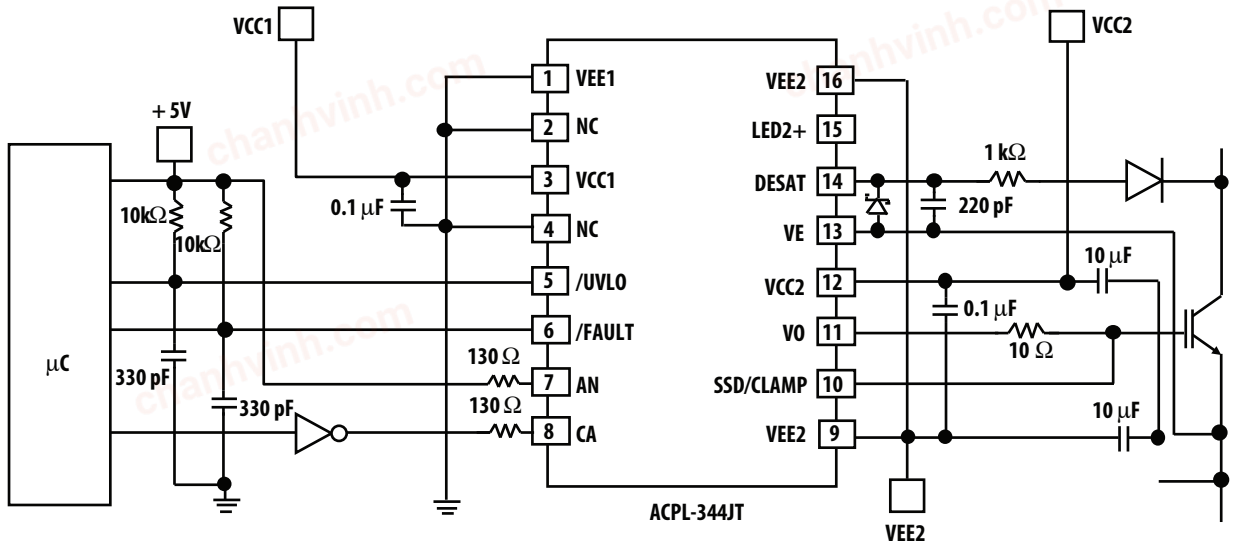


Figure 3. Typical gate drive circuit with Desat current sensing using ACPL-344JT

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of ACPL-344JT is capable of delivering 2.5 A sourcing current to drive the IGBT's gate. While LED is switched off the gate driver can provide 2.5 A sinking current to switch the gate off fast. Additional miller clamping pull-down transistor is activated when output voltage reaches about 2 V with respect to V_{EE2} to provide low impedance path to Miller Current as shown in Figure 4.

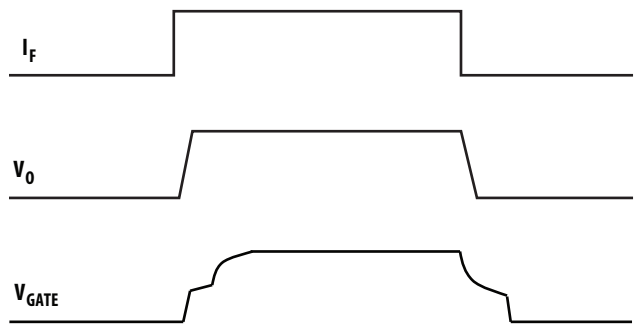


Figure 4. Gate Drive Signal Behavior

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Description of UnderVoltage LockOut

Insufficient gate voltage to IGBT can increase turn on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACPL-344JT monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect IGBT from low voltage bias. During power up, the UVLO feature forces the gate driver output to low to prevent unwanted turn-on at lower voltage.

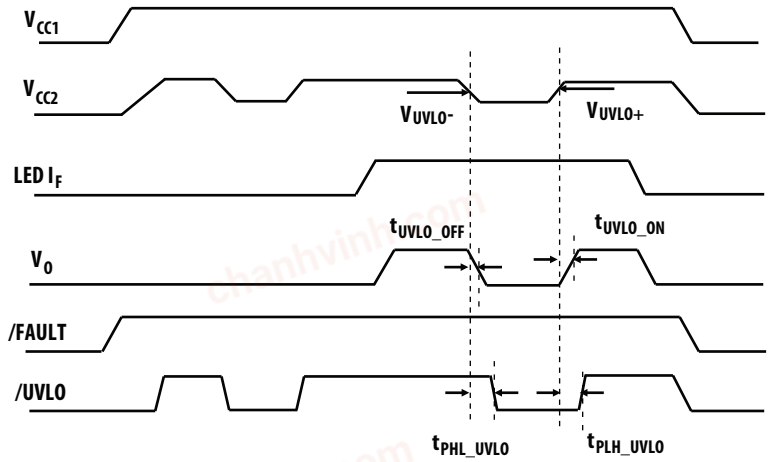


Figure 5. Circuit Behaviors at Power up and Power down

Description of operation during overcurrent condition

1. DESAT terminal monitors IGBT's V_{CE} voltage.
2. When the voltage on the DESAT terminal exceeds 7 V, the output voltage (V_{OUT}) to IGBT gate goes to Hi-Z state and the SSD/CLAMP output is slowly lowered.
3. FAULT output goes Low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.
5. When $t_{DESAT(MUTE)}$ expires, LED input needs to be kept Low for $t_{DESAT(RESET)}$ before fault condition is cleared. FAULT status will return to High and SSD/CLAMP output will return to Hi-Z state.
6. Output (V_{OUT}) starts to respond to LED input after fault condition is cleared.

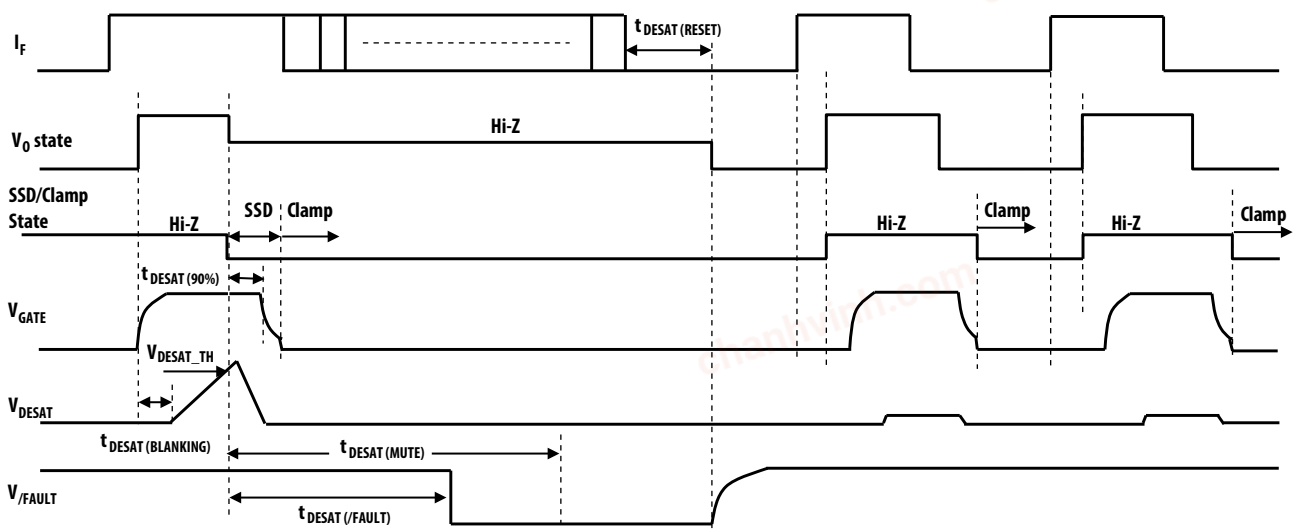


Figure 6. Circuit Behaviors During Overcurrent Event

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The ACPL-344JT is approved by the following organizations:

UL	CSA	IEC/EN/DIN EN 60747-5-5
Approved under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}	Approved under CSA Component Acceptance Notice #5, File CA 88324.	Approved under IEC 60747-5-5 EN 60747-5-5 DIN EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150V_{RMS}		I – IV	
for rated mains voltage ≤ 300V_{RMS}		I – IV	
for rated mains voltage ≤ 600V_{RMS}		I – IV	
for rated mains voltage ≤ 1000V_{RMS}		I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure (also see Figure 7)			
Case Temperature	T_S	175	°C
Input Power	$P_{S,INPUT}$	400	mW
Output Power	$P_{S,OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$> 10^9$	Ω

Notes:
1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

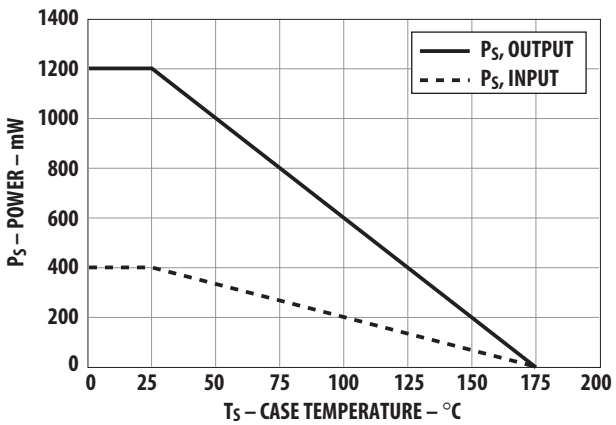


Figure 7. Dependence of safety limiting values on temperature

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Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group			IIIa	Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	150	°C	
Operating Temperature	T_A	-40	125	°C	
IC Junction Temperature	T_J		150	°C	1
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		6	V	
/Fault Output Current (Sinking)	$I_{/FAULT}$		10	mA	
/Fault Pin Voltage	$V_{/FAULT}$	-0.5	6	V	
/UVLO Output Current (Sinking)	$I_{/UVLO}$		10	mA	
/UVLO Pin Voltage	$V_{/UVLO}$	-0.5	6	V	
Positive Input Supply Voltage	V_{CC1}	-0.5	26	V	
Total Output Supply Voltage	V_{CC2}-V_{EE2}	-0.5	30	V	
Negative Output Supply Voltage	V_{EE2}-V_E	-15	0.5	V	2
Positive Output Supply Voltage	V_{CC2}-V_E	-0.5	30	V	
Gate Drive Output Voltage	Vo(peak)	-0.5	V_{CC2} + 0.5	V	
Peak Output Current	$\|I_{O(peak)}\|$		2.5	A	3
Peak Clamping Sinking Current	I_{CLAMP}		2	A	3
Miller Clamping Pin Voltage	V_{CLAMP}-V_{EE2}	-0.5	V_{CC2} + 0.5	V	
Desat Voltage	V_{DESAT}-V_E	V_E – 0.5	V_{CC2} + 0.5	V	4
Output IC Power Dissipation	P_O		580	mW	1
Input IC Power Dissipation	P_I		150	mW	

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Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	-40	125	°C	
Input Supply Voltage	V_{CC1}	8	18	V	
Total Output Supply Voltage	V_{CC2} - V_{EE2}	15	25	V	5
Negative Output Supply Voltage	V_{EE2} -V_E	-10	0	V	3
Positive Output Supply Voltage	V_{CC2} - V_E	15	25	V	
Input LED Current	$I_{F(ON)}$	10	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-5.5	0.8	V	
Input pulse width	$t_{ON(LED)}$	500		ns	

Electrical Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions, all voltages at input IC are referenced to V_{EE1}, all voltages at output IC referenced to V_{EE2}. All typical values at T_A = 25 °C, V_{CC1} = 12 V, V_{CC2}-V_{EE2} = 20 V, V_E-V_{EE2} = 0 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
IC Supply Current								
Input Supply Current	I_{CC1}		3.7	6.0	mA		8	
Output Low Supply Current	I_{CC2L}		10.5	13.2	mA	I_F = 0 mA V_{CC2} = 20 V	9	
Output High Supply Current	I_{CC2H}		10.6	13.6	mA	I_F = 10mA V_{CC2} = 20 V	9	
Logic Input and Output								
LED Forward Voltage (V_{AN} – V_{CA})	V_F	1.25	1.55	1.85	V	I_F = 10 mA	10	
LED Reverse Breakdown Voltage(V_{CA} – V_{AN})	V_{BR}	6			V	I_F = -10 µA		
LED Input Capacitance	C_{IN}		90		pF			
LED Turn on Current Threshold Low to High	I_{TH+}		2.7	6.6	mA	V_O = 5 V	11	
LED Turn on Current Threshold High to Low	I_{TH-}		2.1	6.4	mA	V_O = 5 V	11	
LED Turn on Current Hysteresis	I_{TH_HYS}		0.6		mA			
FAULT Logic Low Output Current	I_{FAULT_L}	4.0	9.0		mA	$V_{/FAULT}$ = 0.4 V		
FAULT Logic High Output Current	I_{FAULT_H}			20	uA	$V_{/FAULT}$ = 5 V		
UVLO Logic Low Output Current	I_{UVLO_L}	4.0	9.0		mA	$V_{/UVLO}$ = 0.4 V		
UVLO Logic High Output Current	I_{UVLO_H}			20	uA	$V_{/UVLO}$ = 5 V		

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Electrical Specifications (continued)

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions, all voltages at input IC are referenced to V_{EE1}, all voltages at output IC referenced to V_{EE2}. All typical values at T_A = 25 °C, V_{CC1} = 12 V, V_{CC2}-V_{EE2} = 20 V, V_E-V_{EE2} = 0 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Gate Driver								
High Level Output Current	I_{OH}		-2.0	-0.75	A	$V_O = V_{CC2}$ - 3 V	12	4
Low Level Output Current	I_{OL}	1.0	2.2		A	$V_O = V_{EE2}$ + 2.5 V	13	4
High Level Output Voltage	V_{OH}	V_{CC2} – 0.5	V_{CC2} – 0.2		V	I_O = -100 mA		6-8
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA		
V_{IN} to High Level Output Propagation Delay Time	t_{PLH}	50	130	250	ns	V_{source} = 5 V R_f = 260 Ω R_g = 10 Ω C_{load} = 10 nF f = 10 kHz Duty Cycle = 50%	14,19	9
V_{IN} to Low Level Output Propagation Delay Time	t_{PHL}	50	150	250	ns		14,19	10
Pulse Width Distortion	PWD	-100	20	100	ns			11,12
Dead Time Distortion (t_{PLH}-t_{PHL})	DTD	-150	-40	105	ns			12,13
10% to 90% Rise Time	t_R		70		ns			
90% to 10% Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50	>70		kV/µs	T_A = 25 °C, I_F = 10 mA V_{CM} = 1500 V	21	14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50	>70		kV/µs	T_A = 25 °C, I_F = 0 mA V_{CM} = 1500 V	21	15
Active Miller Clamp and Soft Shutdown								
Low Level Soft Shutdown Current During Fault Condition	I_{SSD}	22	35	48	mA	$V_{SSD} - V_{EE2}$ = 14 V	15	
Clamp Threshold Voltage	V_{TH_CLAMP}		2.0	3.0	V			
Clamp Low Level Sinking Current	I_{CLAMP}	0.75	1.9		A	V_{CLAMP} = V_{EE2} + 2.5 V		
V_{CC2} UVLO Protection (UVLO voltage V_{UVLO} reference to V_E)								
V_{CC2} UVLO Threshold Low to High	V_{UVLO+}	11.0	12.4	13.7	V	V_O > 5 V		8,16
V_{CC2} UVLO Threshold High to Low	V_{UVLO-}	10.1	11.3	12.8	V	V_O < 5 V		8,17
V_{CC2} UVLO Hysteresis	V_{UVLO_HYS}		1.1		V			8
V_{CC2} to UVLO High Delay	t_{PLH_UVLO}		10		µs			18
V_{CC2} to UVLO Low Delay	t_{PHL_UVLO}		10		µs			19
V_{CC2} UVLO to V_{OUT} High Delay	t_{UVLO_ON}		10		µs			20
V_{CC2} UVLO to V_{OUT} Low Delay	t_{UVLO_OFF}		10		µs			21

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Electrical Specifications (continued)

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions, all voltages at input IC are referenced to V_{EE1}, all voltages at output IC referenced to V_{EE2}. All typical values at T_A = 25 °C, V_{CC1} = 12 V, V_{CC2}-V_{EE2} = 20 V, V_E-V_{EE2} = 0 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Desaturation Protection (Desat voltage V_{DESAT} reference to V_E)								
Desat Sensing Threshold	V_{DESAT}	6.2	7.0	7.8	V		16	8
Desat Charging Current	I_{CHG}	-1.2	-0.9	-0.6	mA	V_{DESAT} = 2 V	17	
Desat Discharging Current	I_{DSCHG}	20	53		mA	V_{DESAT} = 8 V	18	
Internal Desat Blanking Time	$t_{DESAT(BLANKING)}$	0.3	0.6	1.0	µs	C_{SSD} =1 nF		22
Desat Sense to 90% SSD Delay	$t_{DESAT(90\%)}$		0.3		µs			23
Desat Sense to 10% SSD Delay	$t_{DESAT(10\%)}$		0.8		µs			24
Desat to Low Level /FAULT Signal Delay	$t_{DESAT(/FAULT)}$			7.0	µs			25
Output Mute Time due to Desat	$t_{DESAT(MUTE)}$	2.3	3.2	4.1	ms			26
Time for Input Kept Low Before Fault Reset to High	$t_{DESAT(RESET)}$	2.3	3.2	4.1	ms			27

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min. T_A = 25 °C	28, 29, 30
Resistance (Input-Output)	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V_{DC}	30
Capacitance (Input-Output)	C_{I-O}		1.3		pF	f = 1 MHz	
Thermal coefficient between LED and input IC	A_{EI}		35.4		°C/W		
Thermal coefficient between LED and output IC	A_{EO}		33.1		°C/W		
Thermal coefficient between input IC and output IC	A_{IO}		25.6		°C/W		
Thermal coefficient between LED and Ambient	A_{EA}		176.1		°C/W		
Thermal coefficient between input IC and Ambient	A_{IA}		92		°C/W		
Thermal coefficient between output IC and Ambient	A_{OA}		76.7		°C/W		

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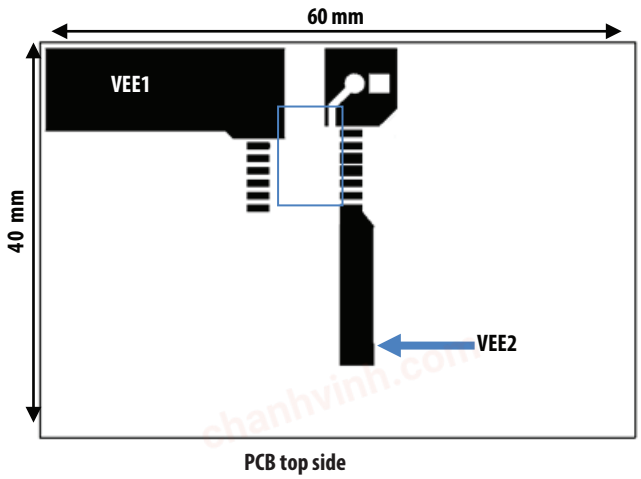
Notes:

1. Output IC power dissipation is derated linearly above 100 °C from 580 mW to 260 mW at 125 °C.
2. This supply is optional. Required only when negative gate drive is implemented.
3. Maximum pulse width = 1 µs, maximum duty cycle = 1%.
4. Maximum 500 ns pulse width if peak V_{DESAT} > 10 V.
5. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.5 V.
6. For High Level Output Voltage testing, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero.
7. Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.
8. Once V_{OUT} of the ACPL-344JT is allowed to go high (V_{CC2} - V_E > V_{UVLO}), the DESAT detection feature of the ACPL-344JT will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{CC2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the DESAT detection and UVLO features of the ACPL-344JT work in conjunction to ensure constant IGBT protection.
9. t_{PLH} is defined as propagation delay from 50% of LED input I_F to 50% of High level output.
10. t_{PHL} is defined as propagation delay from 50% of LED input I_F to 50% of Low level output.
11. Pulse Width Distortion (PWD) is defined as (t_{PHL} – t_{PLH}) of any given unit.
12. As measured from I_F to V_O.
13. Dead Time Distortion (DTD) is defined as (t_{PLH} - t_{PHL}) between any two ACPL-344JT parts under the same test conditions.
14. Common mode transient immunity in the high state is the maximum tolerable dVCM/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V).
15. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V).
16. This is the "increasing" (i.e., turn-on or "positive going" direction) of V_{CC2} - V_E.
17. This is the "decreasing" (i.e., turn-off or "negative going" direction) of V_{CC2} - V_E.
18. The delay time when V_{CC2} exceeds UVLO+ threshold to UVLO High – 50% of UVLO positive-going edge.
19. The delay time when V_{CC2} falls below UVLO- threshold to UVLO Low – 50% of UVLO negative-going edge.
20. The delay time when V_{CC2} exceeds UVLO+ threshold to 50% of High level output.
21. The delay time when V_{CC2} falls below UVLO- threshold to 50% of Low level output.
22. The delay time for ACPL-344JT to respond to a DESAT fault condition without any external DESAT capacitor.
23. The amount of time from when DESAT threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.
24. The amount of time from when DESAT threshold is exceeded to 10% of V_{GATE} at mentioned test conditions.
25. The amount of time from when DESAT threshold is exceeded to FAULT output Low – 50% of V_{CC1} voltage.
26. The amount of time when DESAT threshold is exceeded, Output is mute to LED input.
27. The amount of time when DESAT Mute time is expired, LED input must be kept Low for Fault status to return to High.
28. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥6 000 V_{RMS} for 1 second.
29. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.
30. Device considered a two terminal device: pins 1 - 8 shorted together and pins 9 - 16 shorted together.

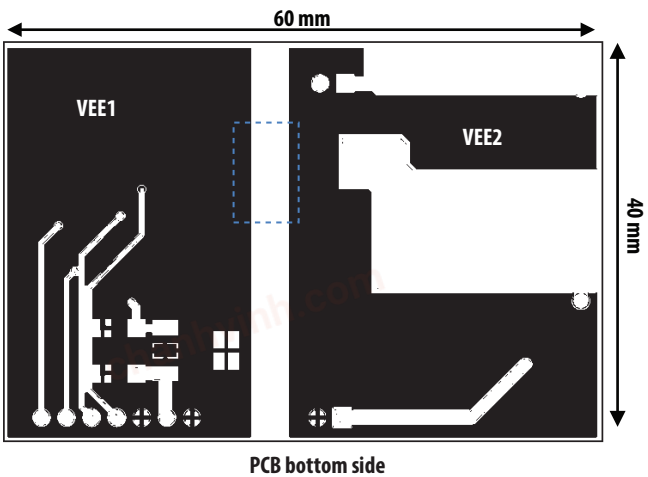
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Thermal Characteristics are based on the ground planes layout of the evaluation PCB, shown as follows:



PCB top side



PCB bottom side

Notes on Thermal Calculation

Application and environmental design for ACPL-344JT need to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150 °C. The following equations calculate the maximum power dissipation and corresponding effect on junction temperatures.

LED Junction Temperature = $A_{EA}*P_E + A_{EI}*P_I + A_{EO}*P_O + T_A$

Input IC Junction Temperature = $A_{EI}*P_E + A_{IA}*P_I + A_{IO}*P_O + T_A$

Output IC Junction Temperature = $A_{EO}*P_E + A_{IO}*P_I + A_{OA}*P_O + T_A$

P_E - LED Power Dissipation

P_I - Input IC Power Dissipation

P_O - Output IC Power Dissipation

Calculation of LED Power Dissipation

LED Power Dissipation, $P_E = I_{F(LED)}$ (Recommended Max) * $V_{F(LED)}$ (125 °C) * Duty Cycle

Example: **P_E** = 16 mA * 1.25 * 50% duty cycle = **10 mW**

Calculation of Input IC Power Dissipation

Input IC Power Dissipation, $P_I = I_{CC1\ (Max)}$ * V_{CC1} (Recommended Max)

Example: **P_I** = 6 mA * 18 V **= 108 mW**

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Calculation of Output IC Power Dissipation

Output IC Power Dissipation, $P_O = V_{CC2}$ (Recommended Max) * I_{CC2} (Max) + P_{HS} + P_{LS}

P_{HS} - High Side Switching Power Dissipation

P_{LS} - Low Side Switching Power Dissipation

$P_{HS} = (V_{CC2} * Q_G * f_{PWM}) * R_{OH(MAX)}/(R_{OH(MAX)} + R_{GH})/2$

$P_{LS} = (V_{CC2} * Q_G * f_{PWM}) * R_{OL(MAX)}/(R_{OL(MAX)} + R_{GL})/2$

Q_G - IGBT Gate Charge at Supply Voltage

f_{PWM} - LED Switching Frequency

$R_{OH(MAX)}$ – Maximum High Side Output Impedance - $V_{OH(MIN)}/I_{OH(MIN)}$

R_{GH} - Gate Charging Resistance

$R_{OL(MAX)}$ - Maximum Low Side Output Impedance - $V_{OL(MIN)}/I_{OL(MIN)}$

R_{GL} - Gate Discharging Resistance

Example:

$R_{OH(MAX)} = (V_{CC2} - V_{OH(MIN)})/ I_{OH(MIN)} = 3\ V/0.75\ A = 4\ \Omega$

$R_{OL(MAX)} = V_{OL(MIN)} / I_{OL(MIN)} = 2.5\ V/1\ A = 2.5\ \Omega$

$P_{HS} = (20\ V * 1\ \mu C * 10\ kHz) * 4\ \Omega/(4\ \Omega + 10\ \Omega)\ /2 = 28.57\ mW$

$P_{LS} = (20\ V * 1\ \mu C * 10\ kHz) * 2.5\ \Omega/(2.5\ \Omega + 10\Omega)/2 = 20\ mW$

P_O = 20 V * 13.6 mA + 28.57 mW + 20 mW **= 320.57 mW**

Calculation of Junction Temperature

LED Junction Temperature = 176.1 °C/W *10 mW + 35.4 °C/W *108 mW + 33.1 * 320.57 mW + T_A **= 16.2°C + T_A**

Input IC Junction Temperature = 35.4 °C/W * 10 mW + 92 °C/W *108 mW + 25.6 * 320.57 mW + T_A **= 18.5°C + T_A**

Output IC Junction Temperature = 33.1 °C/W * 10 mW + 25.6 °C/W *108 mW + 76.7 * 320.57 mW + T_A **= 27.7°C + T_A**

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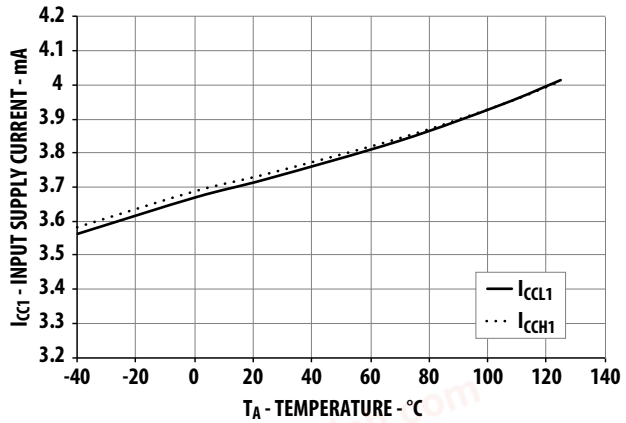


Figure 8. I_{CC1} across temperature

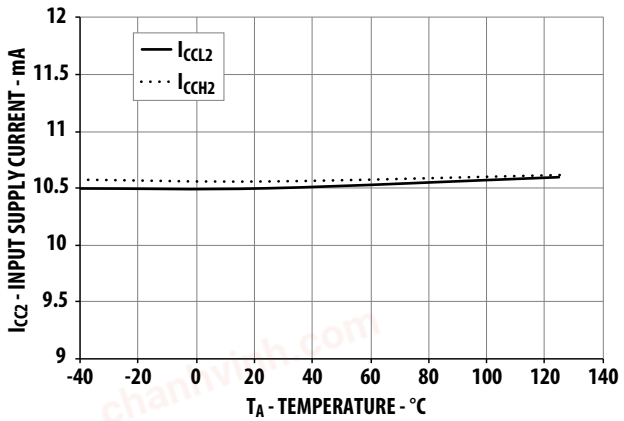


Figure 9. I_{CC2} across temperature

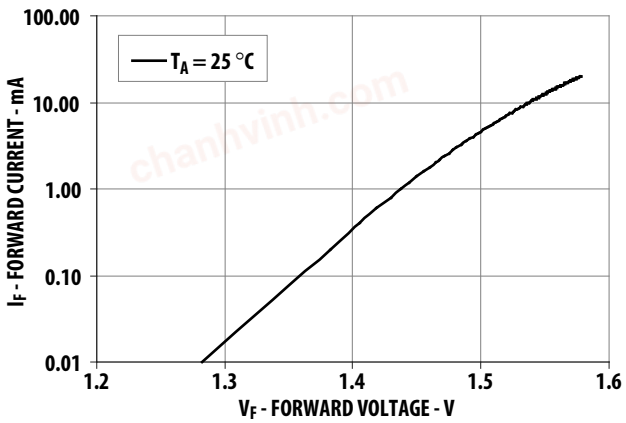


Figure 10. I_F vs. V_F

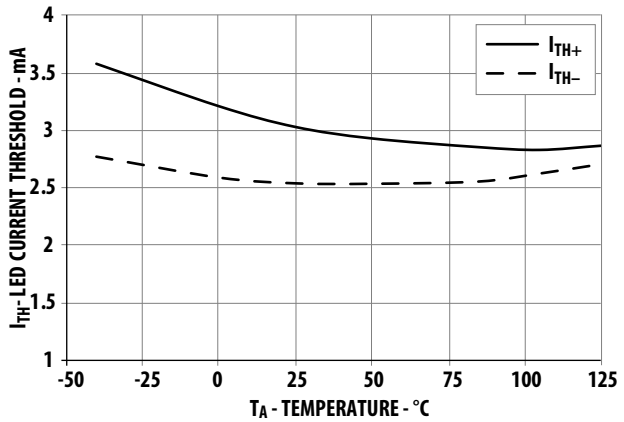


Figure 11. I_{TH} across temperature

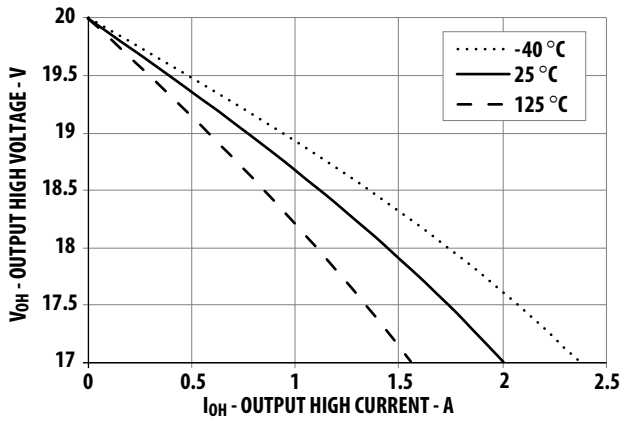


Figure 12. V_{OH} vs. I_{OH}

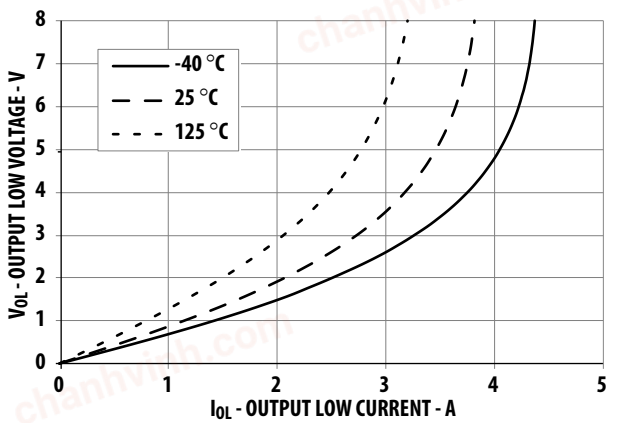


Figure 13. V_{OL} vs. I_{OL}

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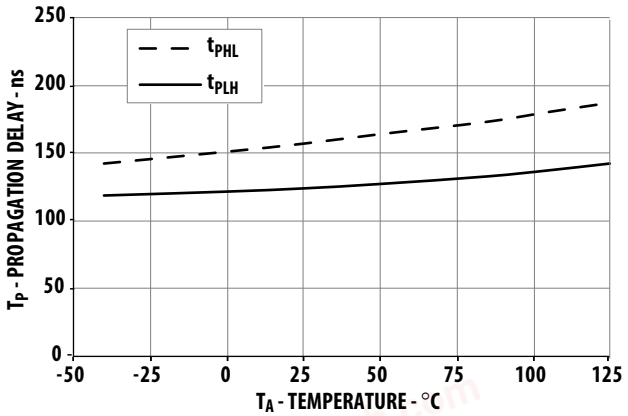


Figure 14. T_P across temperature

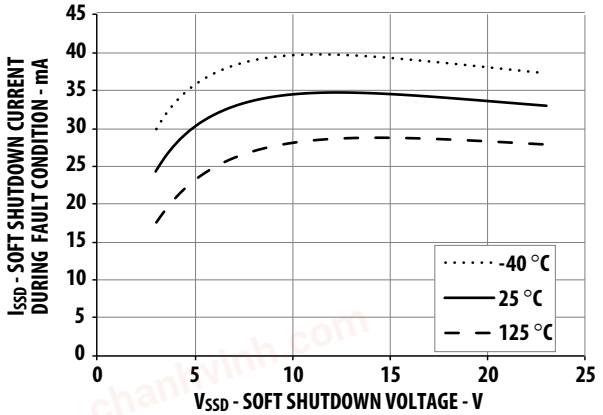


Figure 15. I_{SSD} vs. $V_{SSD/}$

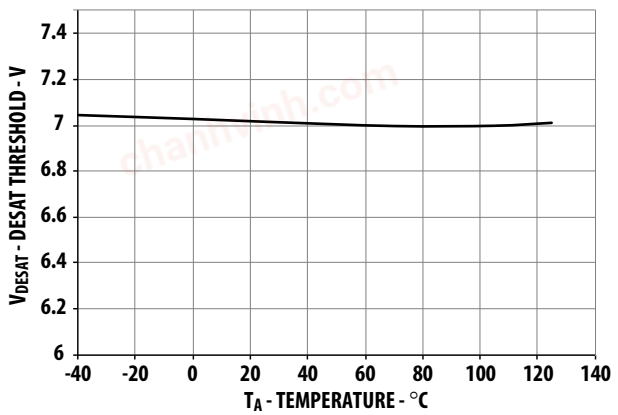


Figure 16. V_{DESAT} Threshold across temperature

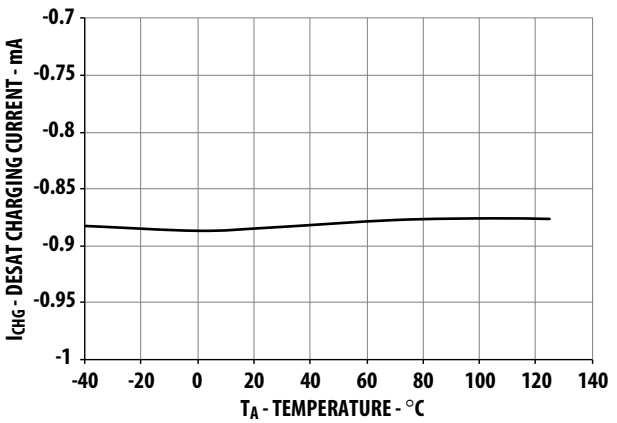


Figure 17. I_{CHG} across temperature

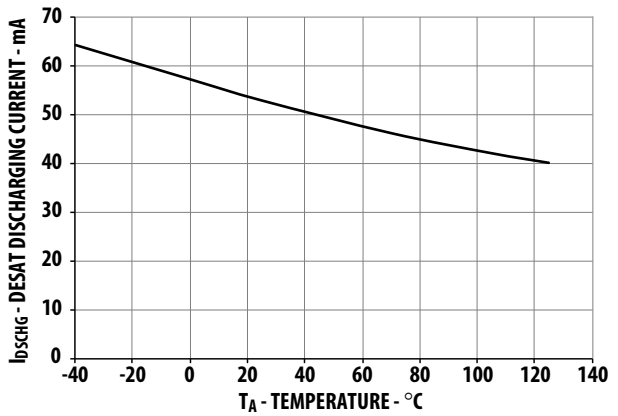


Figure 18. I_{DCHG} across temperature

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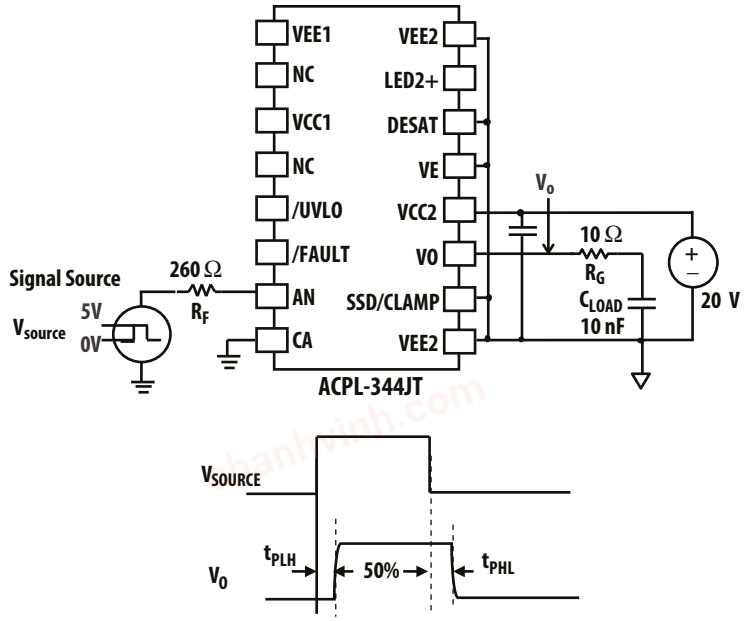


Figure 19. Propagation Delay Test Circuit

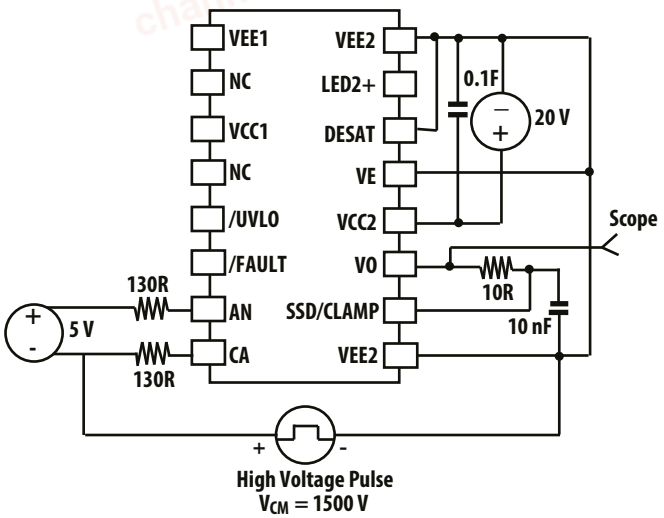


Figure 20. CMR V_O High Test Circuit

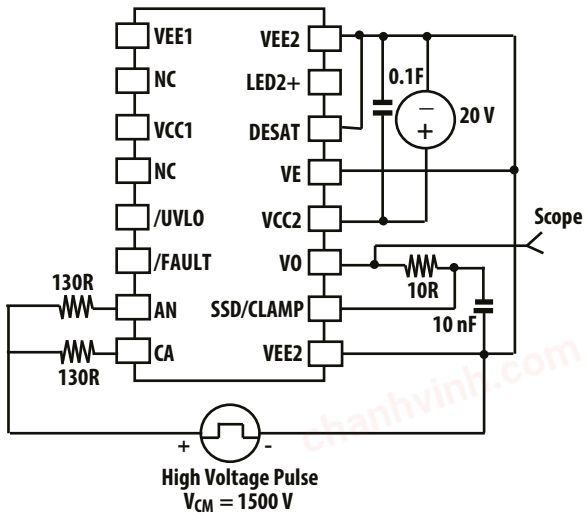


Figure 21. CMR V_O Low Test Circuit

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