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ACPL-071L and ACPL-074L

Single-channel and Dual-channel High Speed 15 MBd CMOS optocoupler with Glitch-Free Power-Up Feature

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

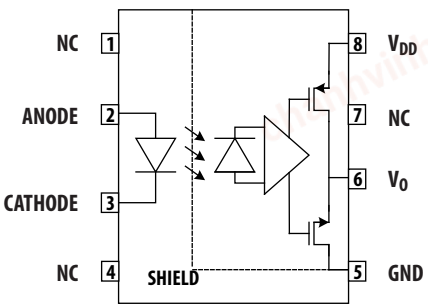
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

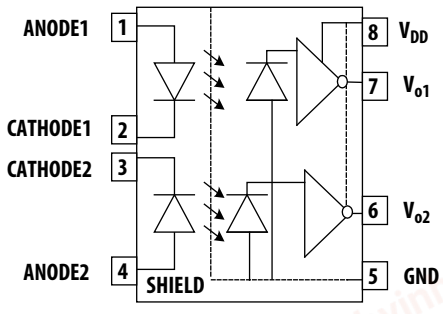
The ACPL-071L (single-channel) and ACPL-074L (dual-channel) are 15 MBd CMOS optocouplers in SOIC-8 package. The optocouplers utilize the latest CMOS IC technology to achieve outstanding performance with very low power consumption. Basic building blocks of ACPL-071L and ACPL-074L are high speed LEDs and CMOS detector ICs. Each detector incorporates an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Component Image

ACPL-071L



ACPL-074L



TRUTH TABLE

LED	V_O, OUTPUT
OFF	H
ON	L

A 0.1uF bypass capacitor must be connected between pins 5 and 8.

Features

- +3.3V and +5 V CMOS compatibility
- 30 ns max. pulse width distortion
- 40ns max. propagation delay (for 3.3V supply voltage)
- 30 ns max. propagation delay skew
- High speed: 15 MBd min
- 10 kV/µs minimum common mode rejection
- –40 to 105°C temperature range
- Glitch-Free Power-Up Feature
- Safety and regulatory approvals pending:
- UL recognized
- 3750 V rms for 1 min. per UL 1577
- CSA component acceptance Notice #5
- IEC/EN/DIN EN 60747-5-2 approved Option 060

Applications

- Digital field bus isolation:
- CANBus, RS485, USB
- Multiplexed data transmission
- Computer peripheral interface
- Microprocessor system interface
- DC/DC converter

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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Ordering Information

ACPL-071L/074L are UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Gull Wing	Tape& Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-071L	-000E	SO-8	X					100 per tube
	-500E		X		X			1500 per reel
	-060E		X				X	100 per tube
	-560E		X		X		X	1500 per reel
ACPL-074L	-000E	SO-8	X					100 per tube
	-500E		X		X			1500 per reel
	-060E		X				X	100 per tube
	-560E		X		X		X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-071L-500E to order product of Small Outline SO-8 package in Tape and Reel packaging in RoHS compliant.

Example 2:

ACPL-074L-000E to order product of Small Outline SO-8 package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

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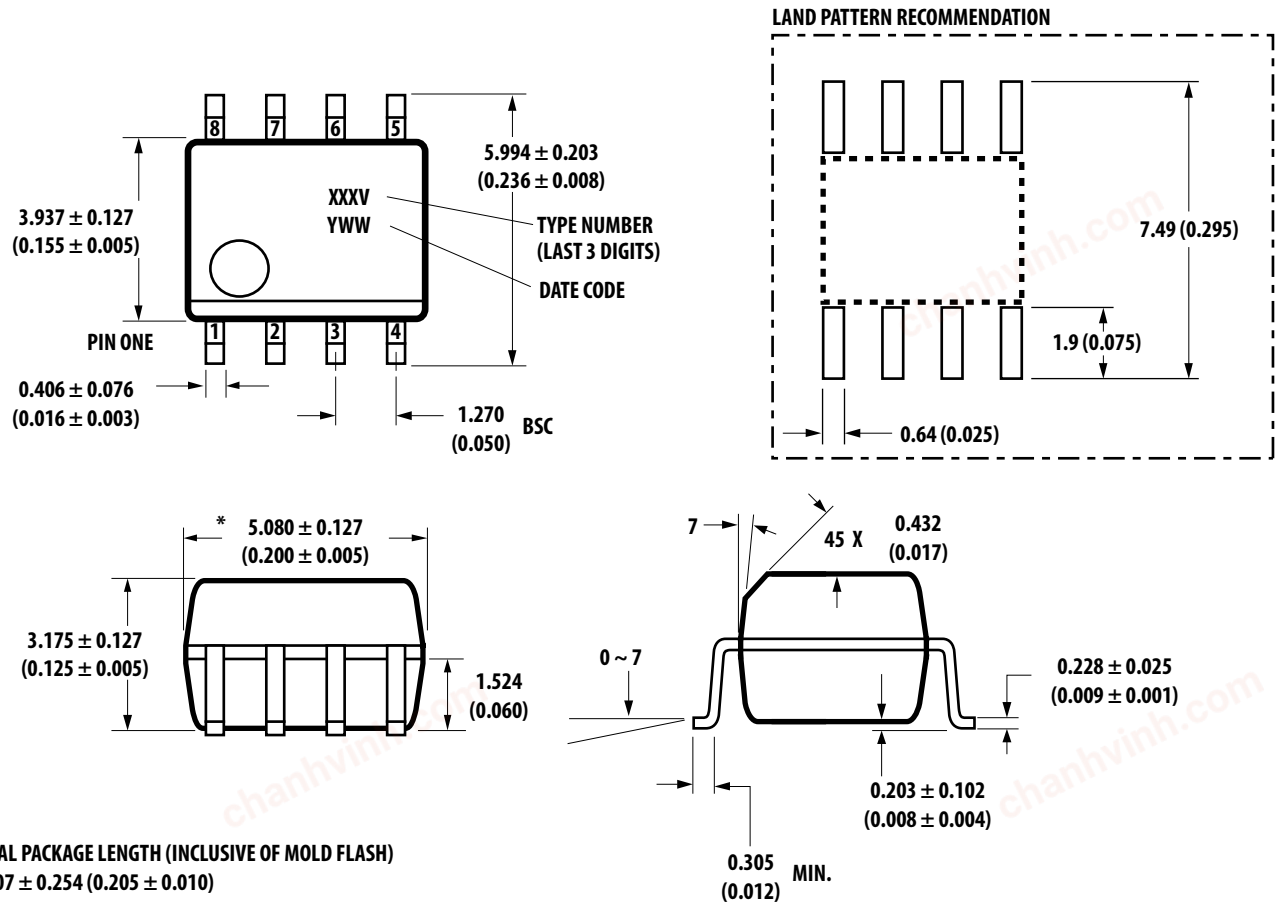
Package Dimensions

ACPL-071L and ACPL-074L (Small Outline S0-8 Package)



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

OPTION NUMBER 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

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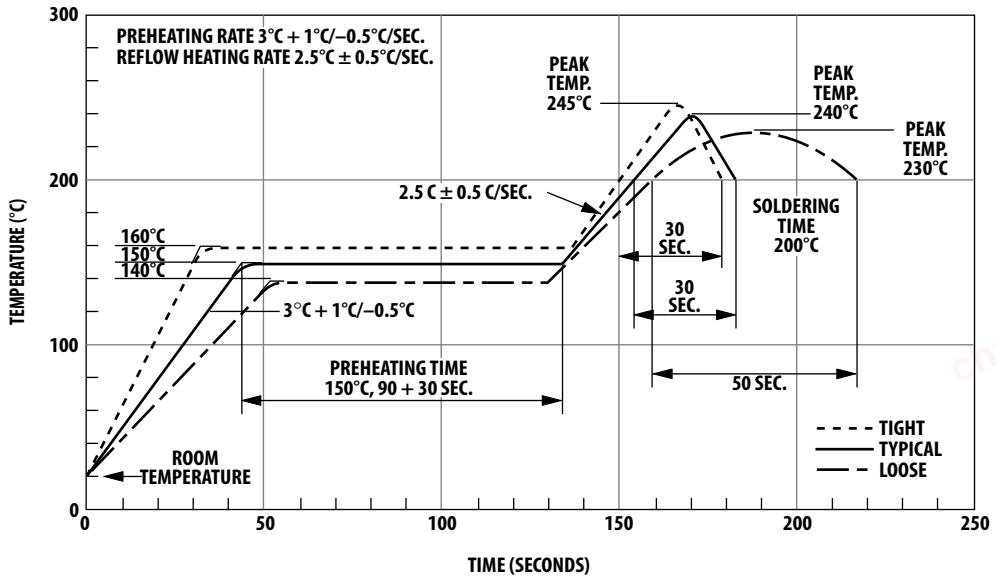
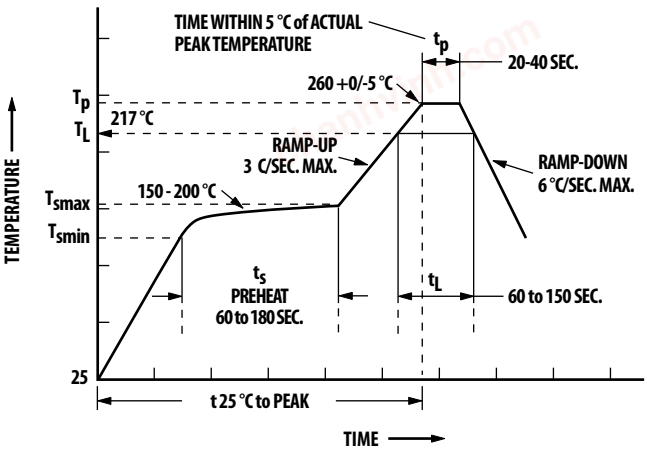
Solder Reflow Thermal profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Flow



Notes:
The time from 25 °C to peak temperature = 8 minutes max.
T_{smax} = 200 °C, T_{smin} = 150 °C
Non-halide flux should be used

Regulatory Information

The ACPL-071L and ACPL-074L have been approved by the following organizations:

UL

Recognized under UL 1577, component recognition program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA88324.

IEC/EN/DIN EN 60747-5-2

Approved under:

IEC 60747-5-2:1997 + A1:2002

EN 60747-5-2:2001 + A1:2002

DIN EN 60747-5-2 (VDE 0884Teil 2):2003-01 (Option 060 only)

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Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago Technologies data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

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IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (Option 060)

Description	Symbol	Option 060	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤150 V rms for rated mains voltage ≤300 V rms		 I-IV I-III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	V_{PEAK}
Input to Output Test Voltage, Method b† V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1050	V_{PEAK}
Input to Output Test Voltage, Method a† V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	840	V_{PEAK}
Highest Allowable Overvoltage† (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	4000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Thermal Derating curve, Figure 11.) Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S,OUTPUT}$	 150 150 600	 °C mA mW
Insulation Resistance at T_S, V_{10} = 500 V	R_{IO}	$\geq 10^9$	Ω

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	0	6.0	Volts
Output Voltage	V_O	–0.5	V_{DD} +0.5	Volts
Average Forward Input Current	I_F	-	20.0	mA
Average Output Current	I_o	-	10.0	mA
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile	See Solder Reflow Temperature Profile Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	4.5	5.5	V
		3.0	3.6	V
Input Current (ON)	I_F	9	18	mA
Supply Voltage Slew Rate[1]	S_R	0.5	500	V/ms

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Electrical Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5 V ≤ V_{DD} ≤ 5.5 V.

All typical specifications are at T_A=+25°C, V_{DD}= +3.3V.

Parameter	Symbol	Part Number	Min.	Typ.	Max.	Units	Test Conditions
Input Forward Voltage	V_F		1.3	1.5	1.8	V	I_F = 14mA
Input Reverse Breakdown Voltage	BV_R		5.0			V	I_R = 10 µA
Logic High Output Voltage	V_{OH}		V_{DD}-1	V_{DD}-0.3		V	I_F = 0, I_O = -4 mA, V_{DD}=3.3V
			V_{DD}-1	V_{DD}-0.2		V	I_F = 0, I_O = -4 mA, V_{DD}=5V
Logic Low Output Voltage	V_{OL}			0.35	0.8	V	I_F = 14mA, I_O =4mA, V_{DD}=3.3V
				0.2	0.8	V	I_F = 14mA, I_O = 4mA, V_{DD}=5V
Input Threshold Current	I_{TH}			4.5	8.8	mA	I_{OL} = 20 µA
Logic Low Output Supply Current	I_{DDL}	ACPL-071L		4.1	6.0	mA	I_F = 14 mA
		ACPL-074L		8.3	12.0	mA	I_F = 14 mA
Logic Low Output Supply Current	I_{DDH}	ACPL-071L		3.8	6.0	mA	I_F = 0
		ACPL-074L		7.6	12.0	mA	I_F = 0

Switching Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5 V ≤ V_{DD} ≤ 5.5 V.

All typical specifications are at T_A=+25°C, V_{DD} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output[2]	t_{PHL}		29	40	ns	I_F = 14mA, C_L= 15pF, V_{DD}=3.3V CMOS Signal Levels
				50	ns	I_F = 14mA, C_L= 15pF, V_{DD}=5V CMOS Signal Levels
Propagation Delay Time to Logic High Output[2]	t_{PLH}		22	40	ns	I_F = 14mA, C_L= 15pF, V_{DD}=3.3V, CMOS Signal Levels
				50	ns	I_F = 14mA, C_L= 15pF, V_{DD}=5V, CMOS Signal Levels
Pulse Width	t_{PW}	66.7			ns	
Pulse Width Distortion[3]	|PWD |	0	7	25	ns	I_F = 14mA, C_L= 15pF, V_{DD}=3.3V, CMOS Signal Levels
				30	ns	I_F = 14mA, C_L= 15pF, V_{DD}=5V, CMOS Signal Levels
Propagation Delay Skew[4]	t_{PSK}			30	ns	I_F = 14mA, C_L= 15pF CMOS Signal Levels
Output Rise Time (10% – 90%)	t_R		20		ns	I_F = 14mA, C_L= 15pF CMOS Signal Levels
Output Fall Time (90% - 10%)	t_F		25		ns	I_F = 14mA, C_L= 15pF CMOS Signal Levels
Common Mode Transient Immunity at Logic High Output[5]	| CM_H |	10	15		kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 0 mA
Common Mode Transient Immunity at Logic Low Output[6]	| CM_L |	10	15		kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 14 mA

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Package Characteristics

All Typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Insulation	I_{I-O}			1.0	µA	45% RH, t = 5 s V_{I-O} = 3 kV DC, T_A = 25°C
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			Vrms	RH ≤ 50%, t = 1 min., T_A = 25°C
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, T_A = 25°C

Notes:
1. Slew rate of supply voltage ramping is recommended to ensure no glitch more than 1V to appear at the output pin.
2. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.
3. PWD is defined as $|t_{PHL} - t_{PLH}|$.
4. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
5. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
6. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

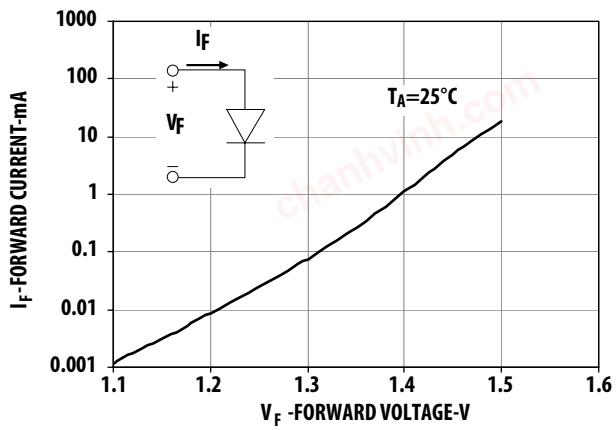

Figure 1. Typical input diode forward characteristic.

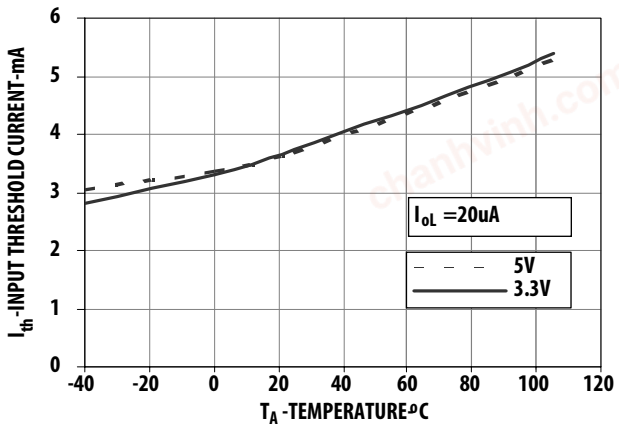

Figure 2. Typical input threshold current vs. temperature.

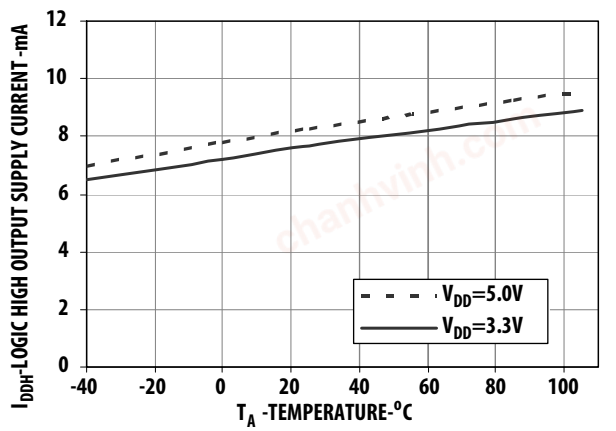

Figure 3. Typical logic high O/P supply current vs. temperature for ACPL-074L.

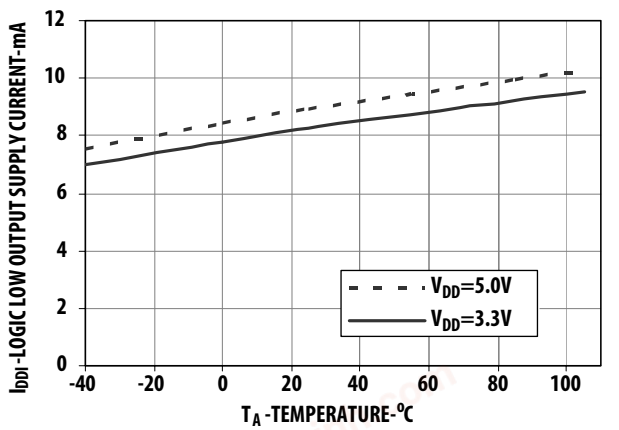

Figure 4. Typical logic low O/P supply current vs. temperature for ACPL-074L.

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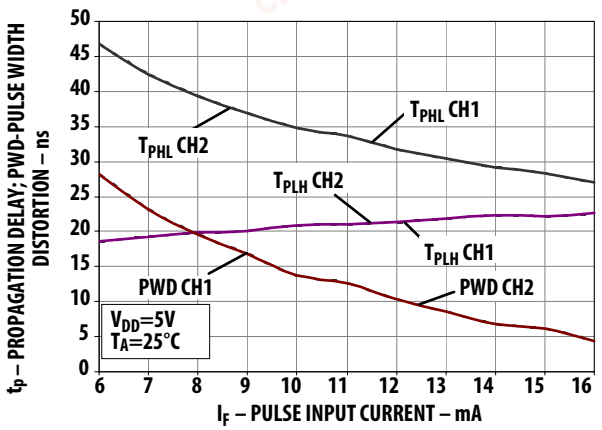


Figure 5. Typical switching speed vs. pulse input current at 5V supply voltage.

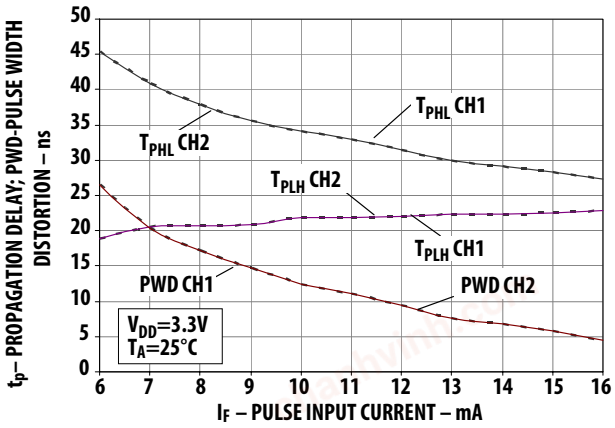


Figure 6. Typical switching speed vs. pulse input current at 3.3V supply voltage.

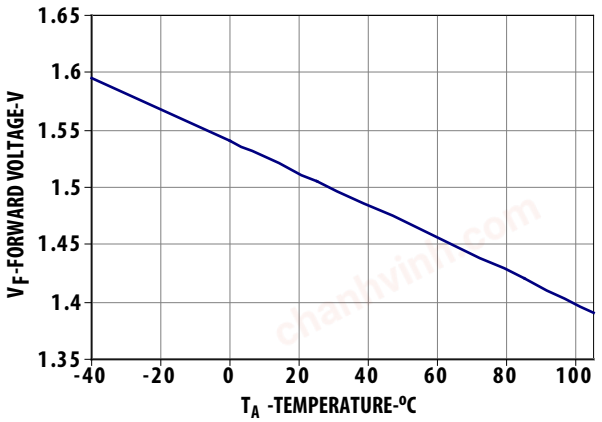


Figure 7 Typical V_F vs. temperature.

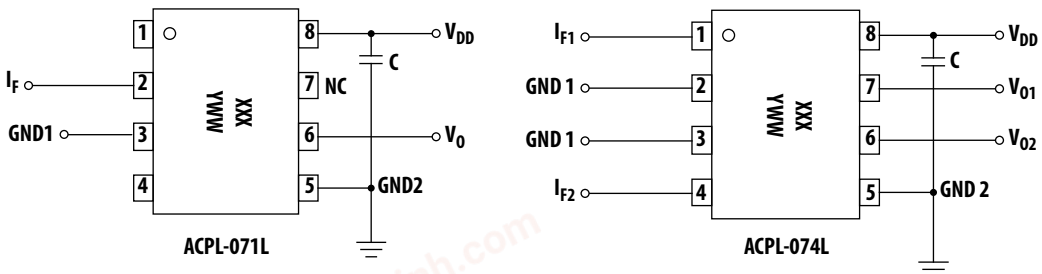
Application Information

Bypassing and PC Board Layout

The ACPL-071L and ACPL-074L optocouplers are extremely easy to use. ACPL-071L and ACPL-074L provide CMOS logic output due to the high-speed CMOS IC technology used.

The external components required for proper operation are the input limiting resistor and the output bypass capacitor. Capacitor values should be between 0.01 µF and 0.1 µF.

For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm.



C = 0.01µF to 0.1µF

Figure 8. Recommended printed circuit board layout

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Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 9).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern.

If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}. As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate.

Figure 10 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 10 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

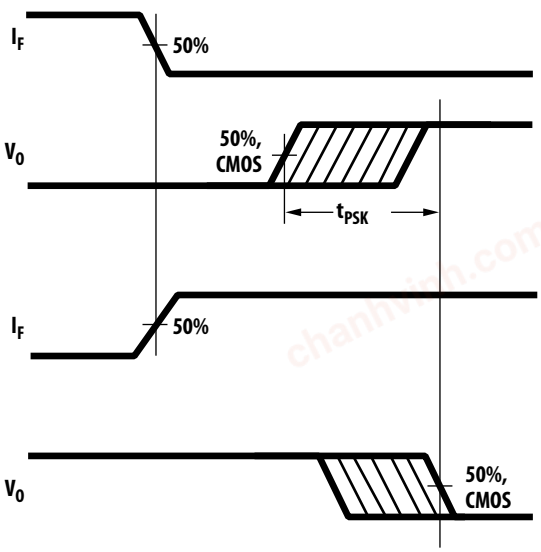

Figure 9. Propagation delay and skew waveform

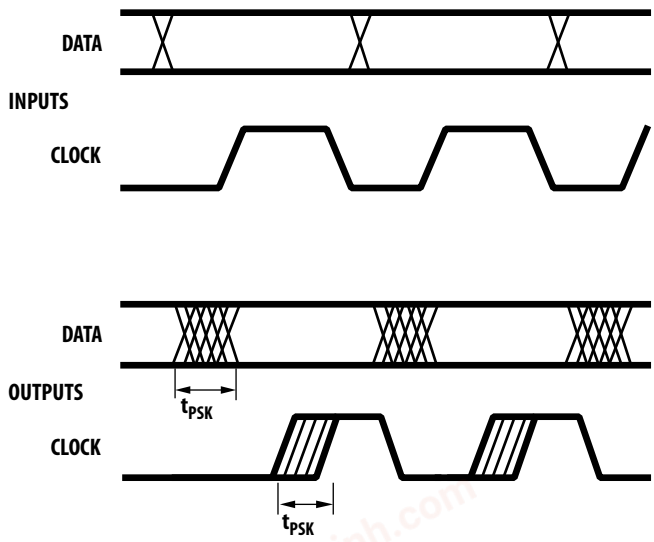

Figure 10. Parallel data transmission example

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The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

Powering Sequence

V_{DD} needs to achieve a minimum level of 3.0V before powering up the output connecting component.

Input Limiting Resistors

ACPL-071L and ACPL-074L are direct current driven (Figure 8), and thus eliminate the need for input power supply. To limit the amount of current flowing through the LED, it is recommended that a 210ohm resistor is connected in series with anode of LED (i.e. Pin 2 for ACPL-071L and Pin 1 and 4 for ACPL-074L) at 5V input signal. At 3.3V input signal, it is recommended to connect 80ohm resistor in series with anode of LED.

The recommended limiting resistors are based on the assumption that the driver output impedence is 50Ω (as shown in Figure 11).

Speed Improvement

A peaking capacitor can be placed across the input current limit resistor (Figure 11) to achieve enhanced speed performance. The value of the peaking cap is dependent to the rise and fall time of the input signal and supply voltages and LED input driving current (I_f). Figure 12 shows significant improvement of propagation delay and pulse with distortion with added peak capacitor at driving current of 14mA and 3.3V or 5V power supply.

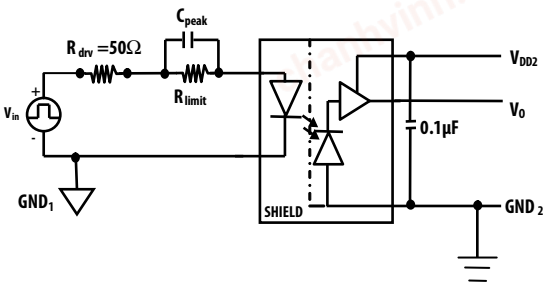
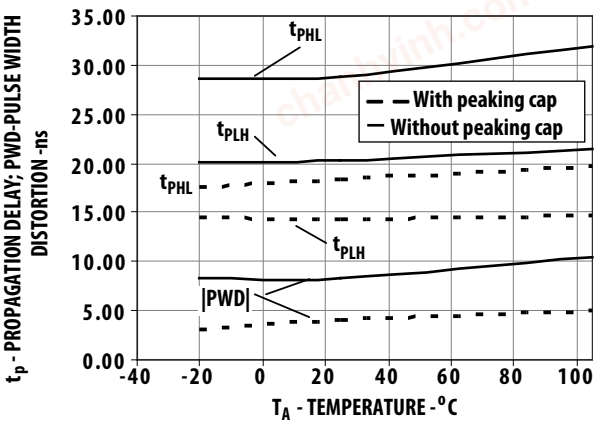
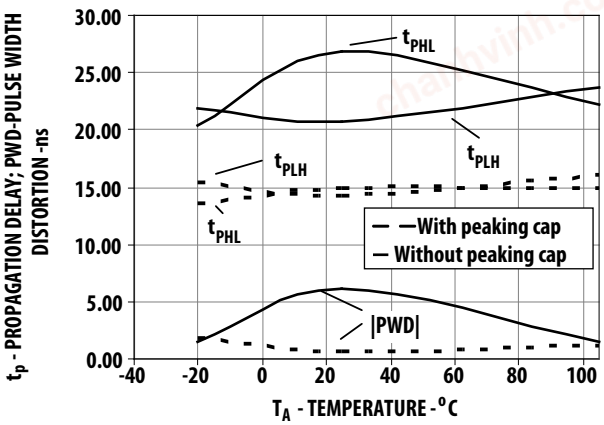


Figure 11 Connection of peaking capacitor (Cpeak) in parallel of the input limiting resistor (Rllimit) to improve speed performance



(i) V_{DD}=3.3V, C_{peak}=100pF, R_{limit}=80Ω



(ii) V_{DD}=5V, C_{peak}=100pF, R_{limit}=210Ω

Figure 12. Improvement of t_p and PWD with added 100pF peaking capacitor in parallel of input limiting resistor.

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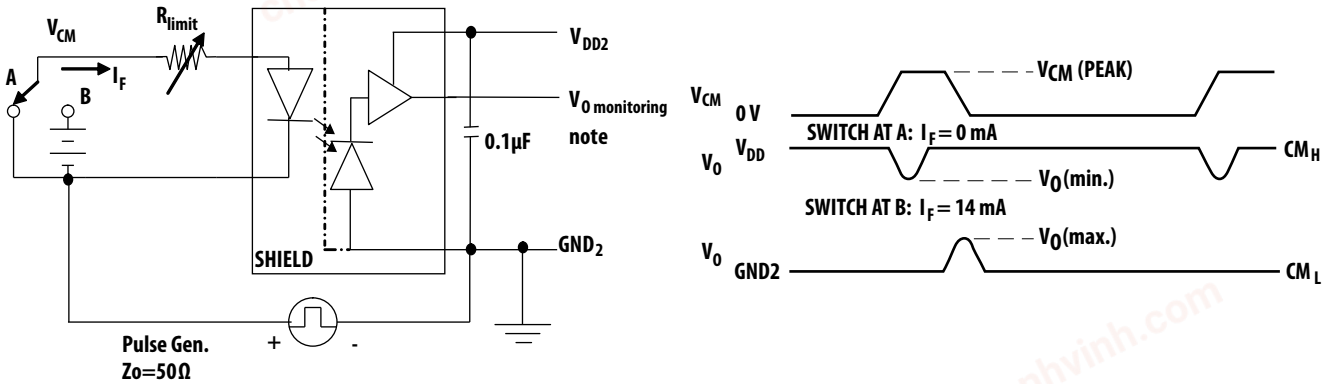

Figure 13. Test circuit for common mode transient immunity and typical waveforms. R_{total} is the total resistance of the driver output impedence (which is assumed to be 50 Ω) and the limiting resistor ($R_{total}=R_{drv}+R_{limit}$) .

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