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6N139, 6N138, HCPL-0701, HCPL-0700, HCNW138, HCNW139

Low Input Current, High Gain Optocouplers

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available; -xxxE denotes a lead-free product

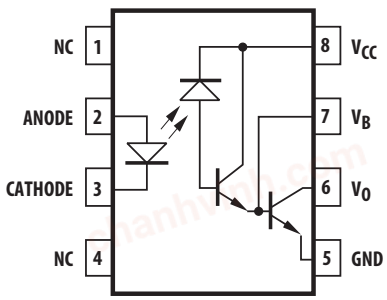
Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139, HCPL-0701, and CNW139 are for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over 0 to 70°C operating range for only 0.5 mA of LED current.

The 6N138, HCPL-0700, and HCNW138 are designed for use mainly in TTL applications. Current Transfer Ratio (CTR) is 300% minimum over 0 to 70°C for an LED current of 1.6 mA (1 TTL Unit load). A 300% minimum CTR enables operation with 1 TTL Load using a 2.2 kΩ pull-up resistor.

Functional Diagram



TRUTH TABLE	
LED	V_O
ON	LOW
OFF	HIGH

*5000 V rms/1 minute rating is for HCNW139/138 and Option 020 (6N139/138) products only.
A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

Features

- High current transfer ratio – 2000% typical (4500 % typical for HCNW139/138)
- Low input current requirements – 0.5 mA
- TTL compatible output – 0.1 V V_{OL} typical
- Performance guaranteed over temperature 0°C to 70°C
- Base access allows gain bandwidth adjustment
- High output current – 60 mA
- Safetyapproval
  UL recognized – 3750 V rms for 1 minute and 5000 V rms* for 1 minute per UL 1577
  CSA approved
  IEC/EN/DIN EN 60747-5-2 approved with V_{IORM} = 1414 V_{peak} for HCNW139 and HCNW138
- Available in 8-Pin DIP or SOIC-8 footprint or widebody package
- MIL-PRF-38534 hermetic version available (HCPL-5700/1)

Applications

- Ground isolate most logic families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low input current line receiver
- High voltage insulation (HCNW139/138)
- EIA RS-232C line receiver
- Telephone ring detector
- 117 V ac line voltage status indicator – low input power dissipation
- Low power systems – ground isolation

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Selection for lower input current down to 250 µA is available upon request.

The HCPL-0701 and HCPL-0700 are surface mount devices packaged in an industry standard SOIC-8 footprint.

The SOIC-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCNW139 and HCNW138 are packaged in a widebody encapsulation that provides creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8		Widebody Package (400 mil)	Minimum Input ON Current (I_F)	Minimum CTR	Absolute Maximum V_{CC}	Hermetic
Single Channel Package	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package				Single and Dual Channel Packages HCPL-
6N139	2731[1]	0701	0731	HCNW139	0.5 mA	400%	18 V	
6N138	2730[1]	0700	0730	HCNW138	1.6 mA	300%	7 V	
HCPL-4701[1]	4731[1]	070A[1]	073A[1]		40 µA	800%	18 V	
					0.5 mA	300%	20 V	5701[1] 5700[1] 5731[1] 5730[1]

Note:
1. Technical data are on separate Avago publications.

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Ordering Information

6N138, 6N139, HCPL-0700 and HCPL-0701 are UL Recognized with 3750 Vrms for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	non RoHS Compliant							
6N138 6N139	-000E	no option	300 mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-0700 HCPL-0701	-000E	no option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	#560		X		X		X	1500 per reel
HCNW138 HCNW139	-000E	no option	400 mil Widebody DIP-8						42 per tube
	-300E	#300		X	X				42 per tube
	-500E	#500		X	X	X			750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

6N138-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval and RoHS compliant.

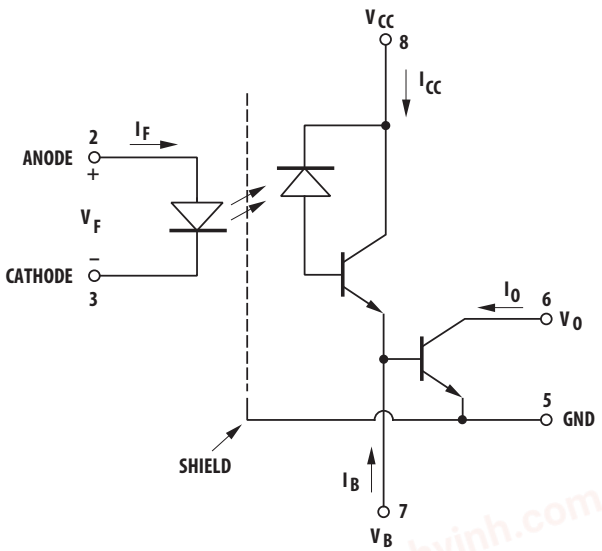
Example 2:

HCPL-0700 to order product of 300 mil DIP package in Tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

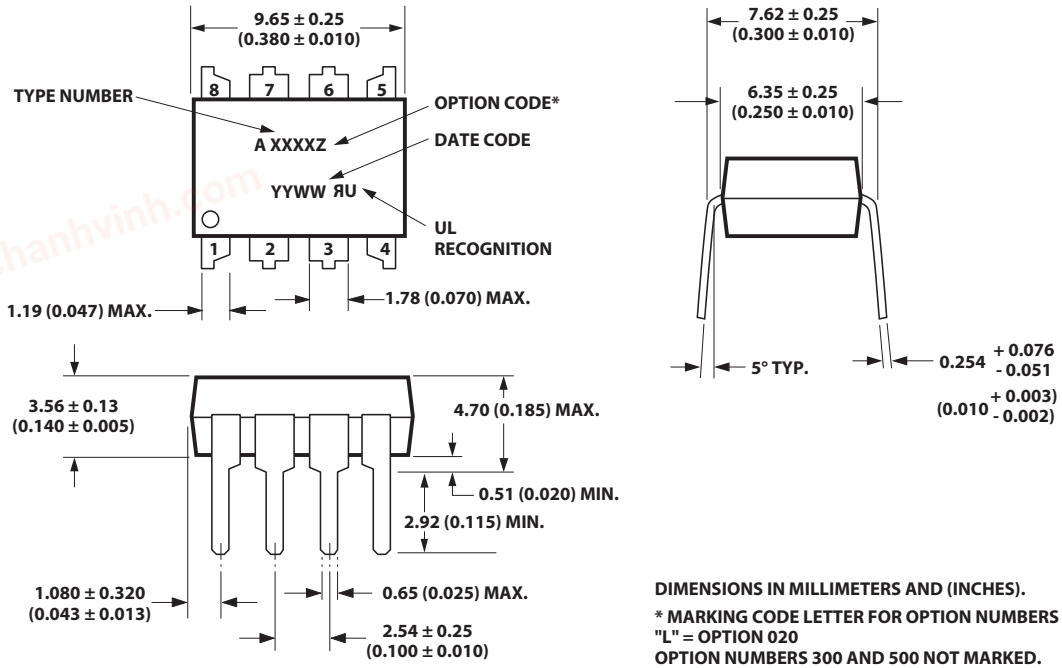
Schematic



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Package Outline Drawings

8-Pin DIP Package (6N139/6N138)**



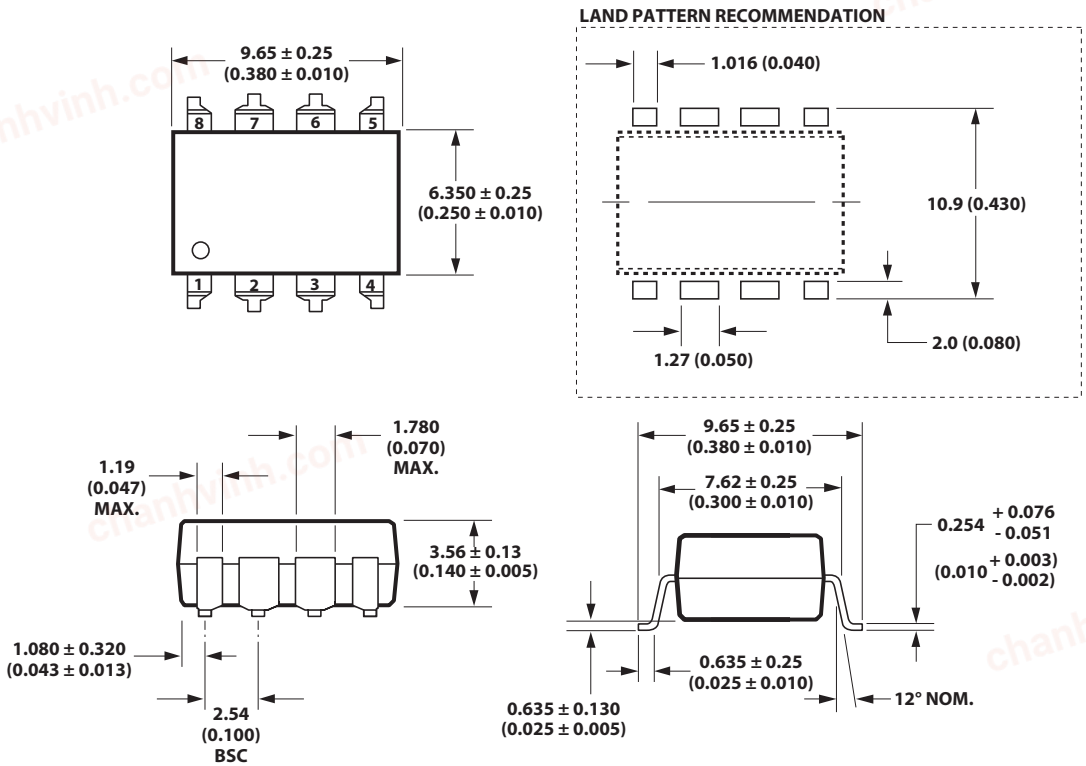
DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

**JEDEC Registered Data.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (6N139/6N138)

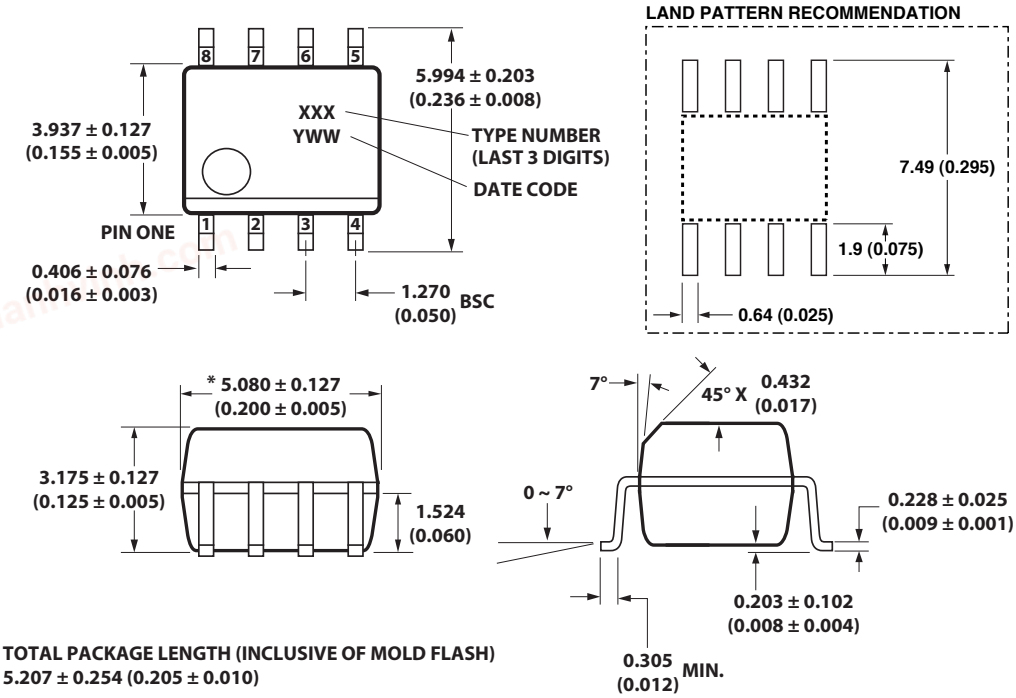


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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Small Outline SO-8 Package (HCPL-0701/HCPL-0700)

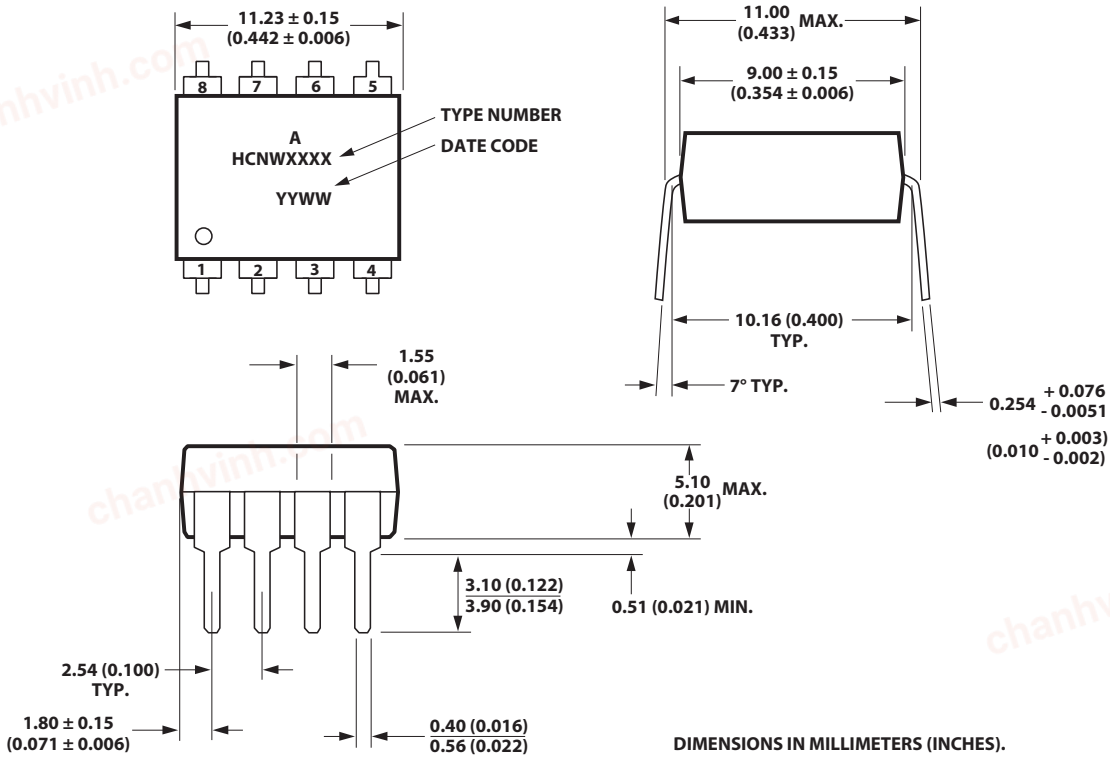


* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

8-Pin Widebody DIP Package (HCNW139/HCNW138)

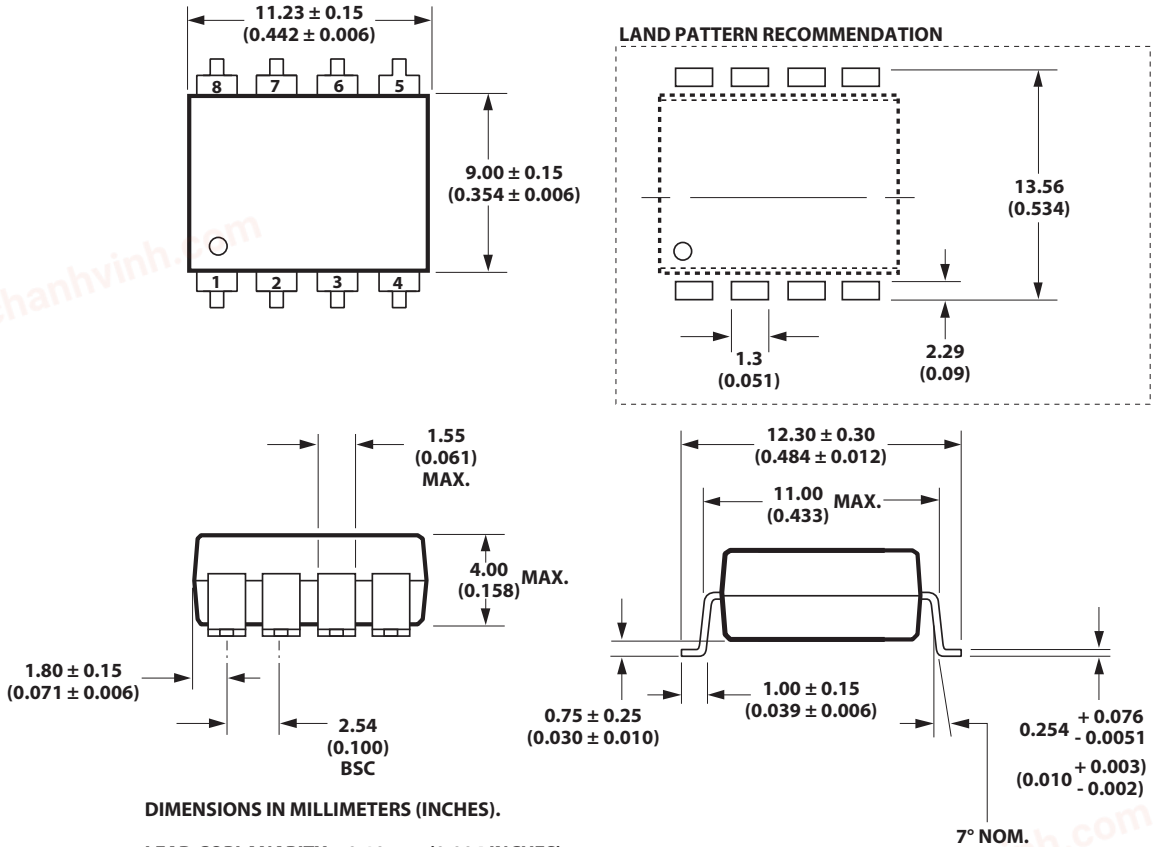


DIMENSIONS IN MILLIMETERS (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW139/HCNW138)

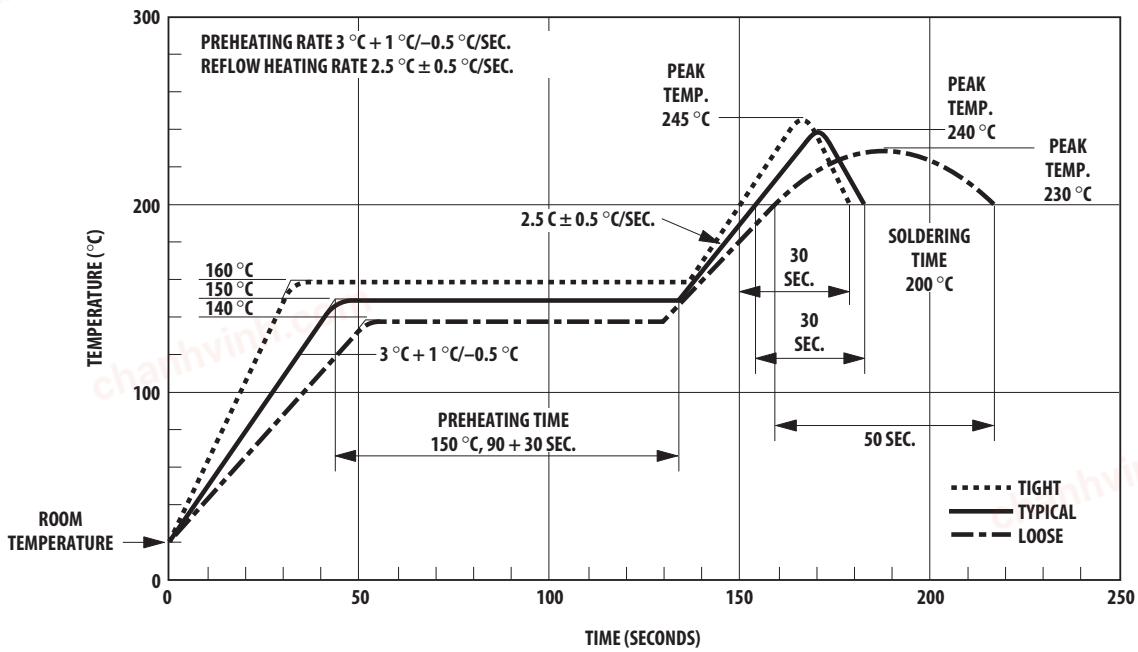


DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

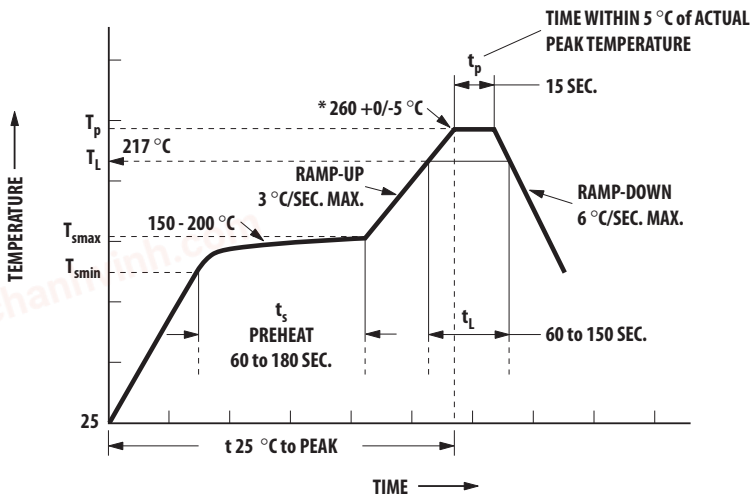
Solder Reflow Temperature Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

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Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

NOTE: NON-HALIDE FLUX SHOULD BE USED.

* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS 245 °C

Regulatory Information

The 6N139/138, HCNW139/138, and HCPL-0701/0700 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2

Approved under
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
(HCNW139/138 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

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IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (HCNW139 and HCNW138)

Description	Symbol	Characteristic	Units
Installation Classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤600 V rms		I-IV	
for rated mains voltage ≤1000 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b* V_{PR} = 1.875 x V_{IORM}, 100% Production Test with t_p = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a* V_{PR} = 1.5 x V_{IORM}, Type and Sample Test, t_p = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Current (Input Current I_F, P_S = 0)	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	> 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-2, for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

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Absolute Maximum Ratings* (No Derating Required up to 85°C)

Parameter		Symbol	Min.	Max.	Units
Storage Temperature		T_S	-55	125	°C
Operating Temperature**		T_A	-40	85	°C
Average Forward Input Current		$I_{F(AVG)}$		20	mA
Peak Forward Input Current (50% Duty Cycle, 1 ms Pulse Width)		I_{FPK}		40	mA
Peak Transient Input Current (<1 µs Pulse Width, 300 pps)		$I_{F(TRAN)}$		1.0	A
Reverse Input Voltage		V_R		5	V
	HCNW139/138			3	V
Input Power Dissipation		P_I		35	mW
Output Current (Pin 6)		I_O		60	mA
Emitter Base Reverse Voltage (Pin 5-7)		V_{EB}		0.5	V
Supply Voltage and Output Voltage (6N139, HCPL-0701, HCNW139)		V_{CC}	-0.5	18	V
Supply Voltage and Output Voltage (6N138, HCPL-0700, HCNW138)		V_{CC}	-0.5	7	V
Output Power Dissipation		P_O		100	mW
Total Power Dissipation		P_T		135	mW
Lead Solder Temperature (for Through Hole Devices)		260°C for 10 sec., 1.6 mm below seating plane			
	HCNW139/138	260°C for 10 sec., up to seating plane			
Reflow Temperature Profile (for SOIC-8 and Option #300)		See Package Outline Drawings section			

*JEDEC Registered Data for 6N139 and 6N138.
**0°C to 70°C on JEDEC Registration.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	18	V
Forward Input Current (ON)	$I_{F(ON)}$	0.5	12.0	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	°C

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Electrical Specifications

0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 18 V, 0.5 mA ≤ $I_{F(ON)}$ ≤ 12 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.
All Typicals at T_A = 25°C. See Note 7.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note	
Current Transfer Ratio	CTR	6N139 HCPL-0701	400*	2000	5000	%	I_F = 0.5 mA	V_{CC} = 4.5 V, V_O = 0.4 V	2, 3	1, 2, 4
		HCNW139	400	4500						
		6N139 HCPL-0701	500*	1600	2600		I_F = 1.6 mA			
		HCNW139	500	3000						
			300	1600			I_F = 5.0 mA			
			200	850			I_F = 12 mA			
		6N138 HCPL-0700	300*	1600	2600		I_F = 1.6 mA			
		HCNW138		1500						
Logic Low Output Voltage	V_{OL}	6N139 HCPL-0701 HCNW139		0.1	0.4	V	I_F = 0.5 mA, I_O = 2 mA	V_{CC} = 4.5	1	2
							I_F = 1.6 mA, I_O = 8 mA			
							I_F = 5.0 mA, I_O = 15 mA			
				0.2			I_F = 12 mA, I_O = 24 mA			
		6N138 HCPL-0700 HCNW138		0.1			I_F = 1.6 mA, I_O = 4.8 mA			
Logic High Output Current	I_{OH}	6N139 HCPL-0701 HCNW139		0.05	100	µA	V_O = V_{CC} = 18 V	I_F = 0 mA		2
		6N138 HCPL-0700 HCNW138		0.1	250		V_O = V_{CC} = 7 V			
Logic Low Supply Current	I_{CCL}	6N138/139 HCPL-0701/ 0700		0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		10	2
		HCNW139 HCNW138		0.5	2					
Logic High Supply Current	I_{CCH}	6N138/139 HCPL-0701/ 0700		0.01	10	µA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V			2
		HCNW139 HCNW138			1					
Input Forward Voltage	V_F	6N138 6N139 HCPL-0701 HCPL-0700	1.25	1.40	1.7*	V	T_A = 25°C	I_F = 1.6 mA	4, 8	
					1.75					
		HCNW139 HCNW138	1.0	1.45	1.85		T_A = 25°C			
			0.95		1.95					
Input Reverse Breakdown Voltage	BVR		5.0*			V	I_R = 10 µA, T_A = 25°C			
		HCNW139 HCNW138	3.0				I_R = 100 µA, T_A = 25°C			
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		8	
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V			
		HCNW139 HCNW138		90						

* JEDEC Registered Data for 6N139 and 6N138.

**All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

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Switching Specifications (AC)

Over recommended operating conditions (T_A = 0 to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max. T_A =25°C		Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	6N139 HCPL-0701 HCNW139		5	25*	30	µs	I_F = 0.5 mA, Rl = 4.7 kΩ	5, 6, 7, 9, 12	2, 4
		6N139 HCPL-0701		0.2	1*	2	µs	I_F = 12 mA, Rl = 270 Ω		
		HCNW139				11				
		6N138 HCPL-0700		1.6	10*	15	µs	I_F = 1.6 mA, Rl = 2.2 kΩ		
		HCNW138				11				
Propagation Delay Time to Logic High at Output	t_{PLH}	6N139 HCPL-0701		18	60*	90	µs	I_F = 0.5 mA, Rl = 4.7 kΩ	5, 6, 7, 9, 12	2, 4
		HCNW139				115				
		6N139 HCPL-0701		2	7*	10	µs	I_F = 12 mA, Rl = 270 Ω		
		HCNW139				11				
		6N138 HCPL-0700		10	35*	50	µs	I_F = 1.6 mA, Rl = 2.2 kΩ		
		HCNW138				70				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10000			V/µs	I_F = 0 mA, T_A = 25°C Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 Vp-p	13	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1000	10000			V/µs	I_F = 1.6 mA, T_A = 25°C Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 Vp-p	13	5, 6

* JEDEC Registered Data for 6N139 and 6N138.

**All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

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Package Characteristics

Parameter		Sym.	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage†		V_{ISO}	3750			V rms	RH < 50%, t = 1 min., T_A = 25°C		3, 8
	Option 020 HCNW139 HCNW138		5000						3, 9
Resistance (Input-Output)		R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc RH < 45%		3
Capacitance (Input-Output)		C_{I-O}		0.6		pF	f = 1 MHz		3

**All typicals at T_A = 25°C, unless otherwise noted.

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. DC CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 Open.
3. Device considered a two-terminal device. Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below 47 kΩ. For more information, please contact your local Avago Components representative.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 220 Ω.
7. Use of a 0.1 µF bypass capacitor connected between pins 8 and 5 adjacent to the device is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 4500 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 µA). This test is performed before the 100% production test shown in the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table, if applicable.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 µA). This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table, if applicable.

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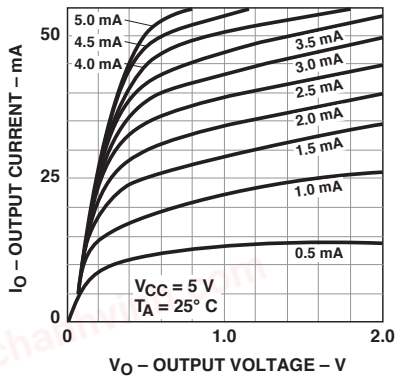


Figure 1. 6N138/6N139 DC transfer characteristics

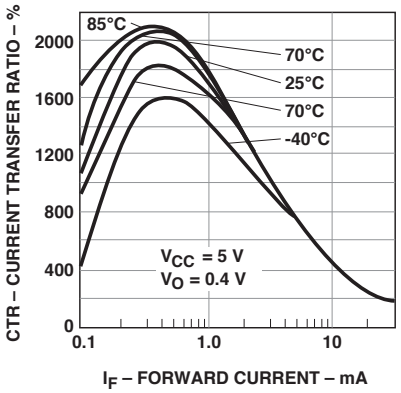


Figure 2. Current transfer ratio vs. forward current 6N138/6N139

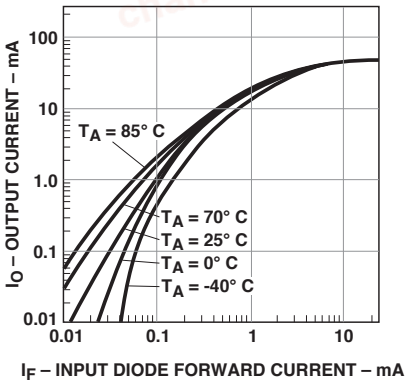


Figure 3. 6N138/6N139 output current vs. input diode forward current

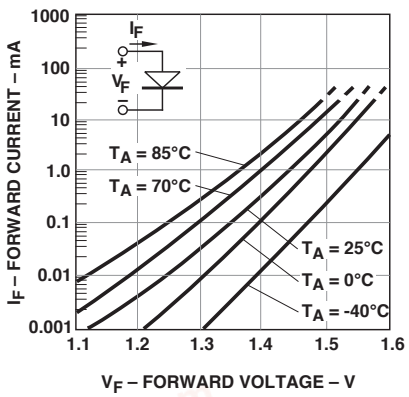


Figure 4. Input diode forward current vs. forward voltage

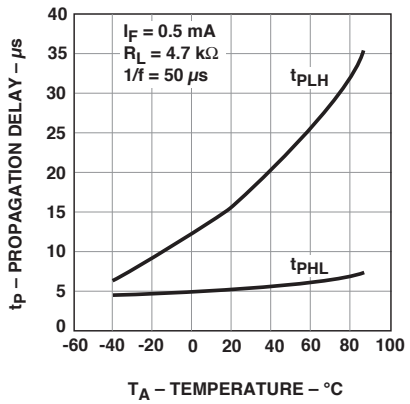


Figure 5. Propagation delay vs. temperature

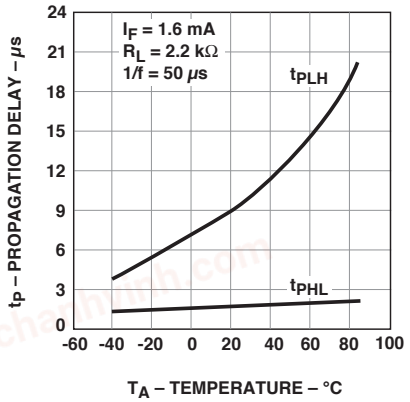


Figure 6. Propagation delay vs. temperature

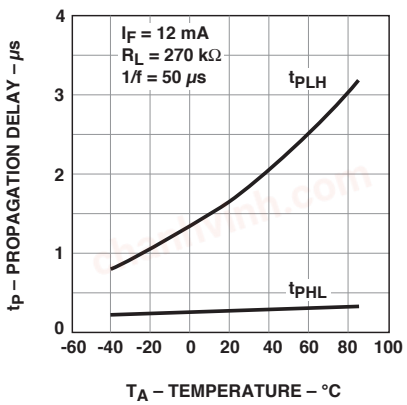


Figure 7. Propagation delay vs. temperature

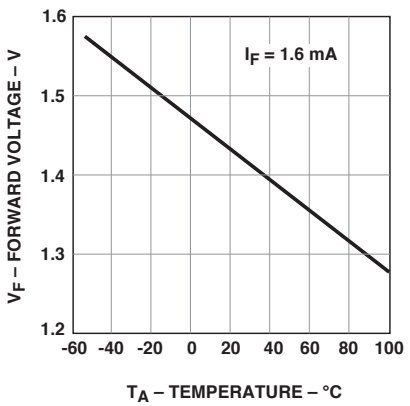


Figure 8. Forward voltage vs. temperature

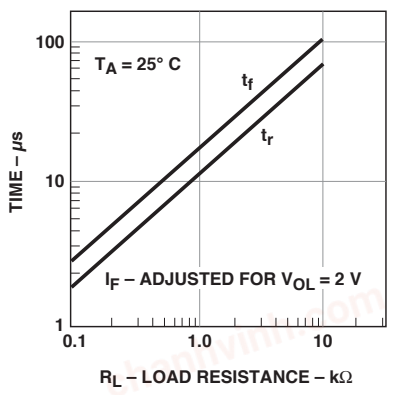


Figure 9. Nonsaturated rise and fall times vs. load resistance

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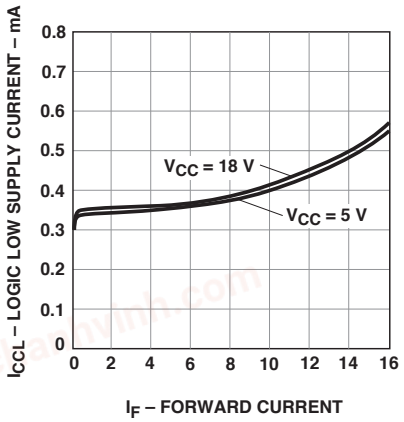


Figure 10. Logic low supply current vs. forward current

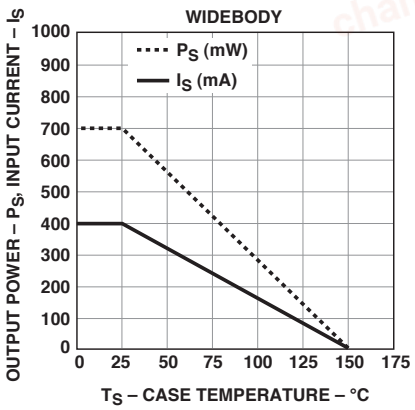
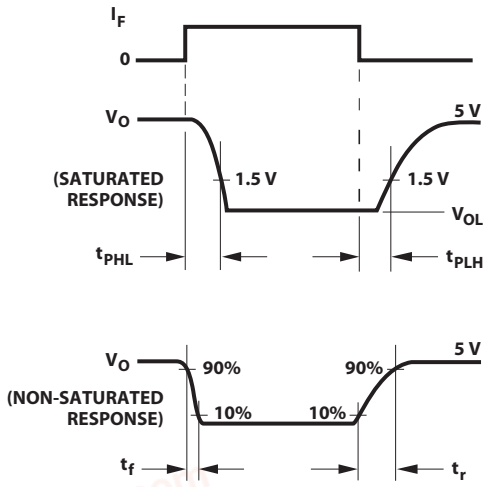


Figure 11. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-2



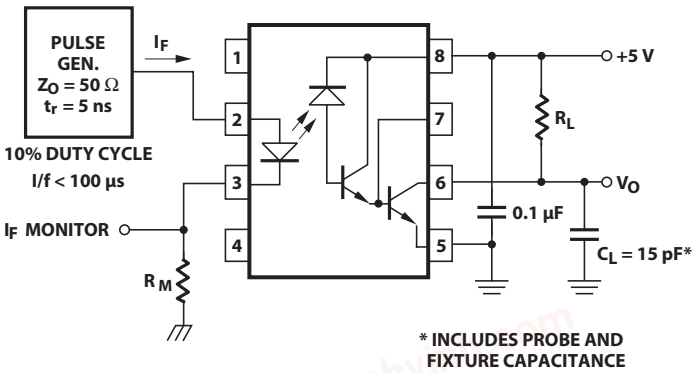
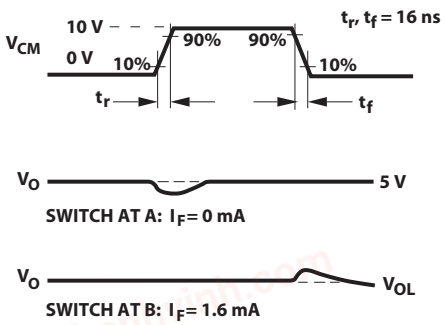


Figure 12. Switching test circuit



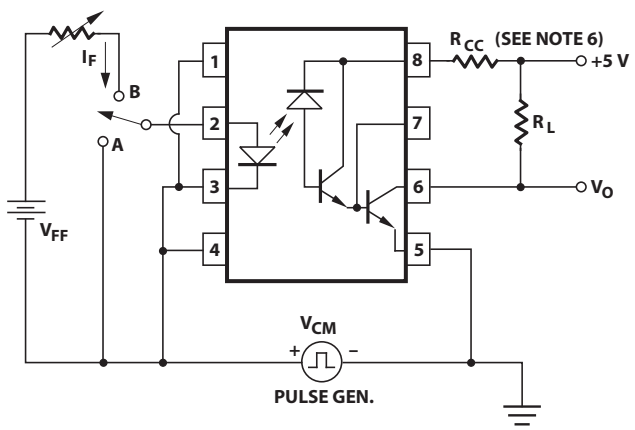


Figure 13. Test circuit for transient immunity and typical waveforms

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