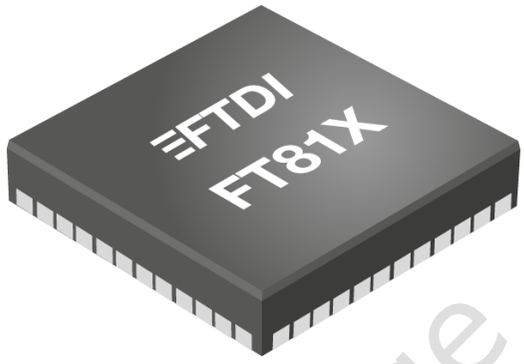
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FT81X Embedded Video Engine
Datasheet Version Draft
Clearance No.: FTDI#440

Future Technology Devices International Ltd.

FT81X

(Advanced Embedded Video Engine)



The FT81X is a series of easy to use graphic controllers targeted for embedded applications to generate high-quality Human Machine Interfaces (HMIs). It has the following features:

- Advanced Embedded Video Engine(EVE) with high resolution graphics and video playback
- FT81X functionality includes graphic control, audio control, and touch control interface.
- Pinout backward compatible with FT800 (FT810) and FT801 (FT811).
- Support multiple widgets for simplified design implementation
- Built-in graphics operations allow users with little expertise to create high-quality displays
- Support 4-wire resistive touch screen (FT810/FT812)
- Support capacitive touch screen with up to 5 touches detection (FT811/FT813)
- Hardware engine can recognize touch tags and track touch movement. Provides notification for up to 255 touch tags.
- Enhanced sketch processing
- Programmable interrupt controller provides interrupts to host MCU
- Built-in 12MHz crystal oscillator with PLL providing programmable system clock up to 60MHz
- Clock switch command for internal or external clock source. External 12MHz crystal or clock input can be used for higher accuracy.
- Video RGB parallel output; configurable to support PCLK up to 60MHz and R/G/B output of 1 to 8 bits
- Programmable timing to adjust HSYNC and VSYNC timing, enabling interface to numerous displays
- Support for LCD display with resolution up to SVGA (800x600) and formats with data enable (DE) mode and VSYNC/HSYNC mode
- Support landscape and portrait orientations
- Display enable control output to LCD panel
- Integrated 1MByte graphics RAM, no frame buffer RAM required
- Support playback of motion-JPEG encoded AVI videos
- Mono audio channel output with PWM output
- Built-in sound synthesizer
- Audio wave playback for mono 8-bit linear PCM, 4-bit ADPCM and μ-Law coding format at sampling frequencies from 8kHz to 48kHz. Built-in digital filter reduces the system design complexity of external filtering
- PWM output for display backlight dimming control
- Advanced object oriented architecture enables low cost MPU/MCU as system host using SPI interfaces
- Support SPI data lines in single, dual or quad mode; SPI clock up to 30MHz
- Power mode control allows chip to be put in power down, sleep and standby states
- Supports I/O voltage from 1.8V to 3.3V
- Internal voltage regulator supplies 1.2V to the digital core
- Build-in Power-on-reset circuit
- -40°C to 85°C extended operating temperature range
- Available in a compact Pb-free, VQFN-48 and VQFN-56 package, RoHS compliant

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1 Typical Applications

- Point of Sales Machines
- Multi-function Printers
- Instrumentation
- Home Security Systems
- Graphic touch pad – remote, dial pad
- Tele / Video Conference Systems
- Phones and Switchboards
- Medical Appliances
- Blood Pressure displays
- Heart monitors
- Glucose level displays
- Breathalyzers
- Gas chromatographs
- Power meter
- Home appliance devices
- Set-top box
- Thermostats
- Sprinkler system displays
- Medical Appliances
- GPS / Satnav
- Vending Machine Control Panels
- Elevator Controls
- ……and many more

1.1 Part Numbers

Part Number	Description	Package
FT810Q-x	EVE with 18 bit RGB, resistive touch	48 Pin VQFN, body 7 x 7 mm, pitch 0.5mm
FT811Q-x	EVE with 18 bit RGB, capacitive touch	48 Pin VQFN, body 7 x 7 mm, pitch 0.5mm
FT812Q-x	EVE with 24 bit RGB, resistive touch	56 Pin VQFN, body 8 x 8 mm, pitch 0.5mm
FT813Q-x	EVE with 24 bit RGB, capacitive touch	56 Pin VQFN, body 8 x 8 mm, pitch 0.5mm

Table 1- FT81X Embedded Video Engine Part Numbers

Note: Packaging codes for x is:

-R: Taped and Reel (3000pcs per reel)

-T: Tray packing (260 pcs per tray)

For example: FT810Q-R is 3000 VQFN pieces in taped and reel packaging

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2 FT81X Block Diagram

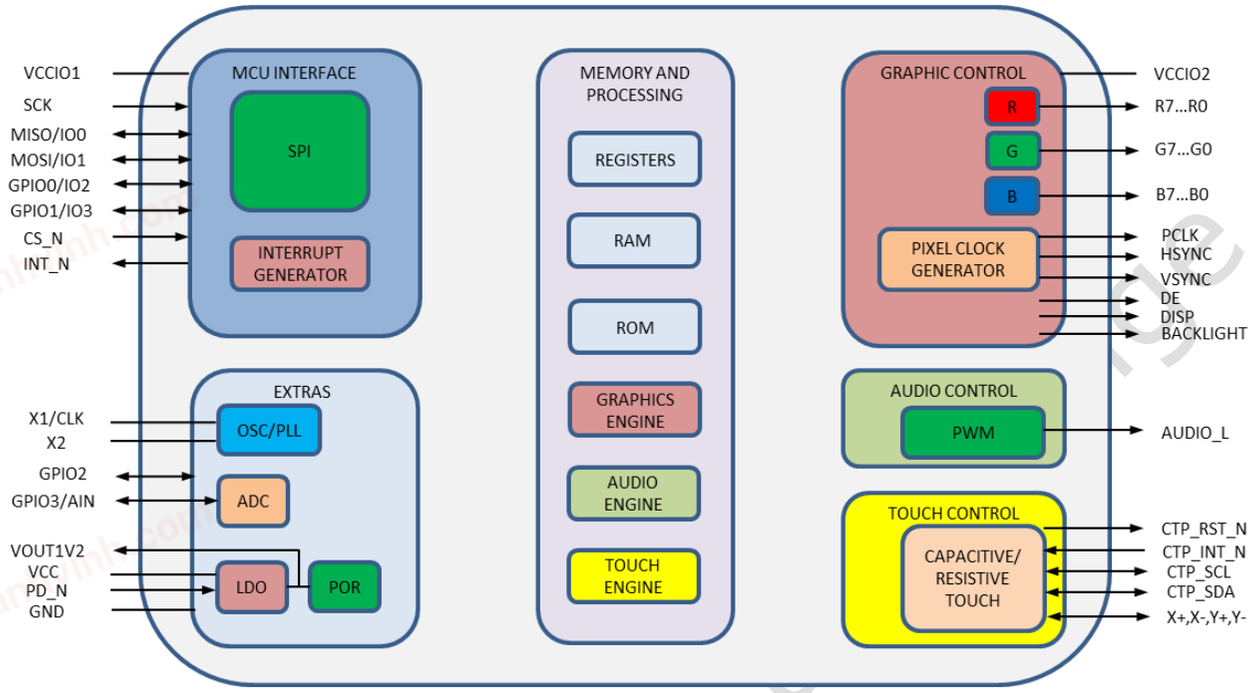


Figure 2-1 FT81X Block Diagram

For a description of each function please refer to Section 4.

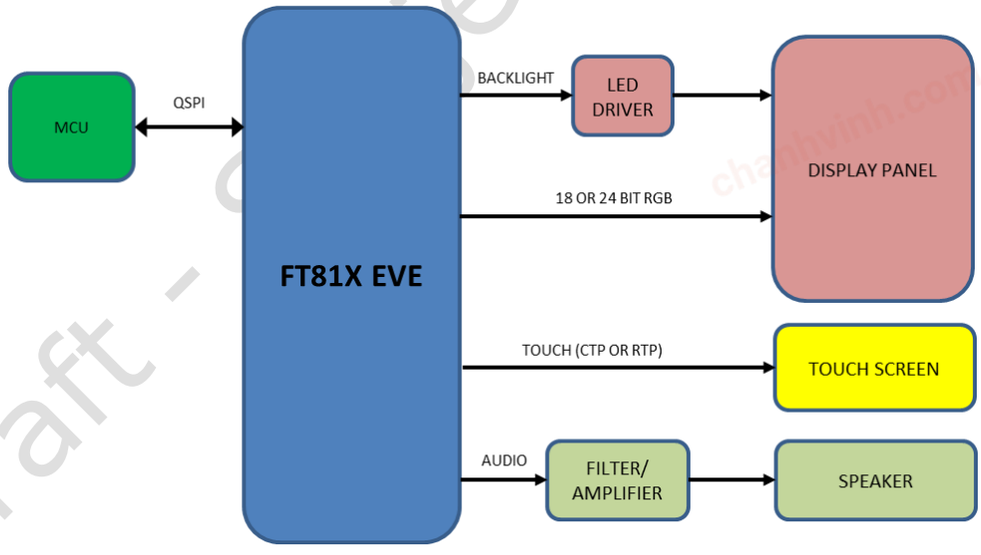


Figure 2-2 FT81X System Design Diagram

FT81X with EVE (Embedded Video Engine) technology simplifies the system architecture for advanced human machine interfaces (HMIs) by providing support for display, audio, and touch as well as an object oriented architecture approach that extends from display creation to the rendering of the graphics.

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3 Device Pin Out and Signal Description

3.1 FT810 VQFN-48 Package Pin Out

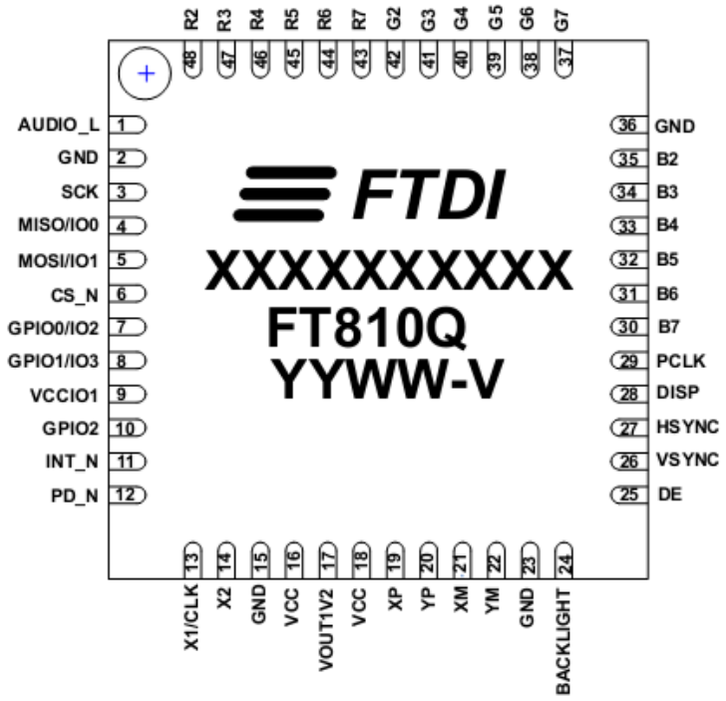


Figure 3-1 Pin Configuration FT810 VQFN-48 (top view)

3.2 FT811 VQFN-48 Package Pin Out

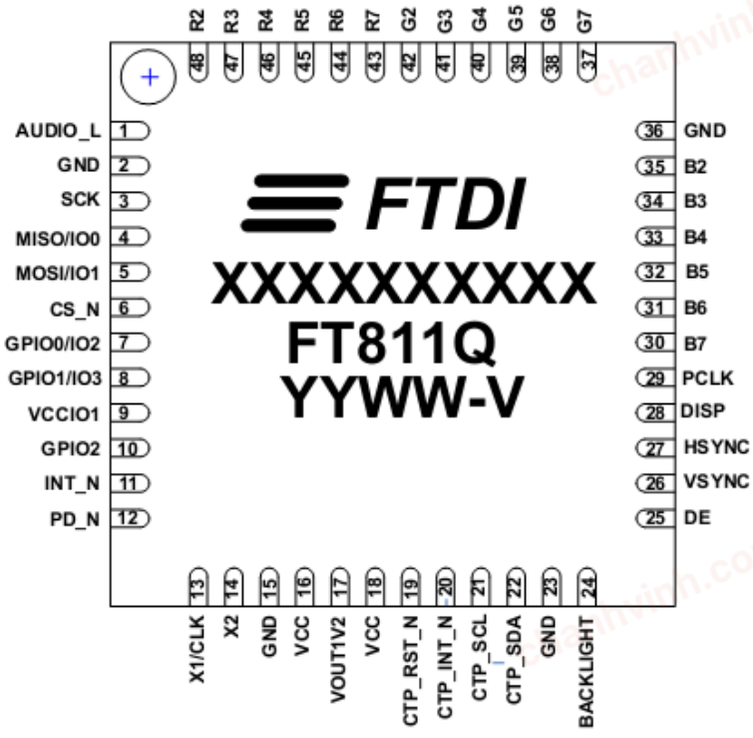


Figure 3-1 Pin Configuration FT811 VQFN-48 (top view)

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3.3 FT812 VQFN-56 Package Pin Out

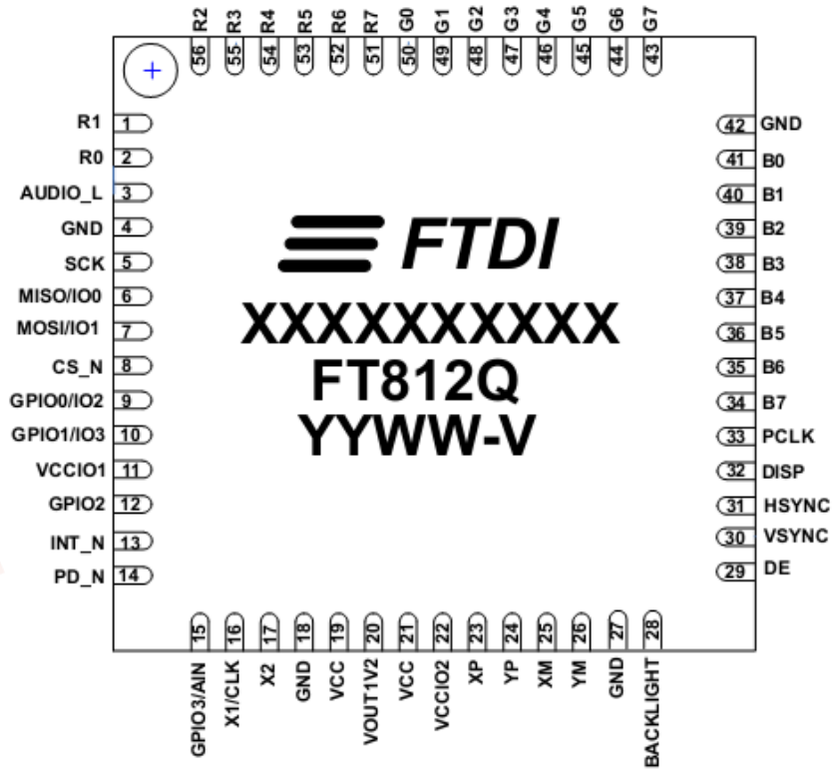


Figure 3-1 Pin Configuration FT812 VQFN-56 (top view)

3.4 FT813 VQFN-56 Package Pin Out

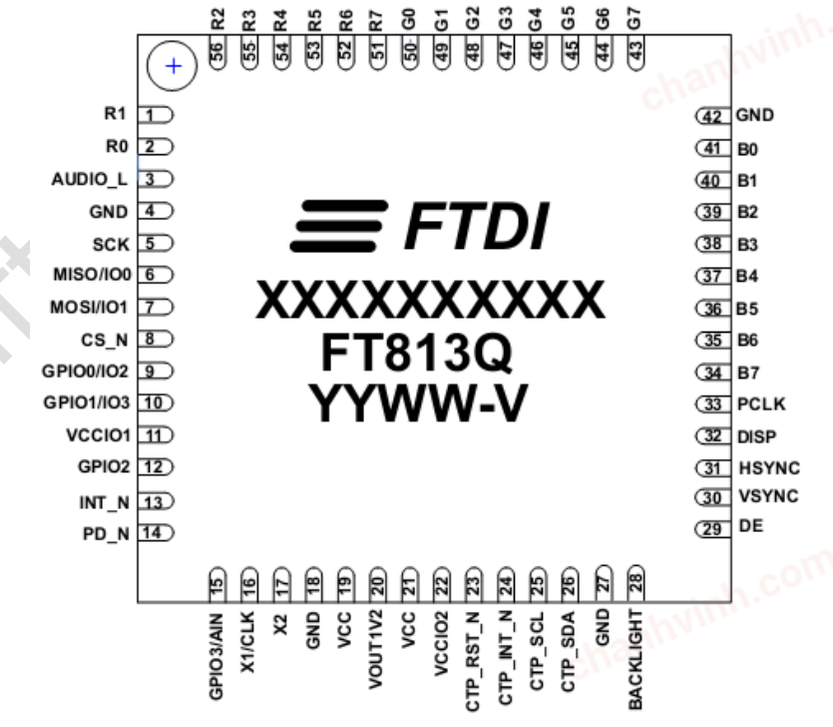


Figure 3-1 Pin Configuration FT813 VQFN-56 (top view)

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3.5 Pin Description

Table 3-1 FT81X pin description

Pin Number				Pin Name	Type	Description
FT810	FT811	FT812	FT813			
-	-	1	1	R1	O	Bit 1 of Red RGB signals Pad powered from pin VCCIO2
-	-	2	2	R0	O	Bit 0 of Red RGB signals Pad powered from pin VCCIO2
1	1	3	3	AUDIO_L	O	Audio PWM out Pad powered from pin VCC
2	2	4	4	GND	P	Ground
3	3	5	5	SCK	I	SPI clock input. Input pad with Schmitt trigger, 3.3V tolerant. Pad powered from pin VCCIO1
4	4	6	6	MISO/IO0	I/O	SPI Single mode: SPI MISO output. SPI Quad mode: SPI data line 0. Pad powered from pin VCCIO1
5	5	7	7	MOSI/IO1	I/O	SPI Single mode: SPI MOSI input. SPI Quad mode: SPI data line 1. Pad powered from pin VCCIO1
6	6	8	8	CS_N	I	SPI slave select input. Input pad with Schmitt trigger, 3.3V tolerant. Pad powered from pin VCCIO1
7	7	9	9	GPIO0/ IO2	I/O	SPI Single mode: General purpose IO 0. SPI Quad mode: SPI data line 2. Pad powered from pin VCCIO1
8	8	10	10	GPIO1/ IO3	I/O	SPI Single mode: General purpose IO 1. SPI Quad mode: SPI data line 3. Pad powered from pin VCCIO1
9	9	11	11	VCCIO1	P	I/O power supply for host interface pins. Support 1.8V, 2.5V or 3.3V. Note: VCCIO1 supply to IO pads from pin 3 to 12(QFN-48 package) or pin 5 to 14(QFN-56 package) only.
10	10	12	12	GPIO2	I	General purpose IO 2 Pad powered from pin VCCIO1.
11	11	13	13	INT_N	OD	Host interrupt, open drain output, active low, pull up to VCCIO1 through a 1kΩ ~10kΩ resistor.

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12	12	14	14	PD_N	I	Power down input, active low, 3.3V tolerant. Connect to MCU GPIO for power management or hardware reset function, or pulled up to VCCIO1 through 47kΩ resistor and 100nF to ground. Pad powered from pin VCCIO1.
-	-	15	15	GPIO3/AIN	AI/O	General purpose IO 3 or analog input for ADC. Pad powered from pin VCCIO1.
13	13	16	16	X1/ CLK	I	Crystal oscillator or clock input; Connect to GND if not used. 3.3V peak input allowed. Pad powered from pin VCC.
14	14	17	17	X2	O	Crystal oscillator output; leave open if not used. Pad powered from pin VCC.
15	15	18	18	GND	P	Ground
16	16	19	19	VCC	P	3.3V power supply input.
17	17	20	20	VOUT1V2	O	1.2V regulator output pin. Connect a 4.7uF decoupling capacitor to GND.
18	18	21	21	VCC	P	3.3V power supply input.
		22	22	VCCIO2	P	I/O power supply for RGB and touch pins. For QFN-48 package, VCCIO2 pad is bonded together with VCC pin; For QFN-56 package, VCCIO2 pad is separate from VCC, supporting 1.8V, 2.5V or 3.3V. VCCIO2 can be connected to different voltage with VCCIO1. Note: VCCIO2 supply to IO pads from pin 19 to 48(QFN-48 package) or pin 21 to 56(QFN-56 package) only.
19		23		XP	AI/O	Connect to X right electrode of 4-wire resistive touch-screen panel. Pad powered from pin VCCIO2.
20		24		YP	AI/O	Connect to Y top electrode of 4-wire resistive touch-screen panel. Pad powered from pin VCCIO2.
21		25		XM	AI/O	Connect to X left electrode of 4-wire resistive touch-screen panel. Pad powered from pin VCCIO2.
22		26		YM	AI/O	Connect to Y bottom electrode of 4-wire resistive touch-screen panel. Pad powered from pin VCCIO2.
-	19	-	23	CTP_RST_N	O	Connect to reset or wake signal of the CTPM. Pad powered from pin VCCIO2.
-	20	-	24	CTP_INT_N	I	Connect to interrupt or ready pin of the

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						CTPM. Pad powered from pin VCCIO2.
-	21	-	25	CTP_SCL	I/OD	Connect to I2C SCL pin of the CTPM. Plain input, open-drain output. Pad powered from pin VCCIO2.
-	22	-	26	CTP_SDA	I/OD	Connect to I2C SDA pin of the CTPM. Plain input, open-drain output. Pad powered from pin VCCIO2.
23	23	27	27	GND	P	Ground
24	24	28	28	BACKLIGHT	O	LED Backlight brightness PWM control signal. Pad powered from pin VCCIO2.
25	25	29	29	DE	O	LCD Data Enable. Pad powered from pin VCCIO2.
26	26	30	30	VSYNC	O	LCD Vertical Sync. Pad powered from pin VCCIO2.
27	27	31	31	HSYNC	O	LCD Horizontal Sync. Pad powered from pin VCCIO2.
28	28	32	32	DISP	O	General purpose output pin for LCD Display Enable. Pad powered from pin VCCIO2.
29	29	33	33	PCLK	O	LCD Pixel Clock. Pad powered from pin VCCIO2.
30	30	34	34	B7	O	Bit 7 of Blue RGB signals. Pad powered from pin VCCIO2.
31	31	35	35	B6	O	Bit 6 of Blue RGB signals. Pad powered from pin VCCIO2.
32	32	36	36	B5	O	Bit 5 of Blue RGB signals. Pad powered from pin VCCIO2.
33	33	37	37	B4	O	Bit 4 of Blue RGB signals. Pad powered from pin VCCIO2.
34	34	38	38	B3	O	Bit 3 of Blue RGB signals. Pad powered from pin VCCIO2.
35	35	39	39	B2	O	Bit 2 of Blue RGB signals. Pad powered from pin VCCIO2.
-	-	40	40	B1	O	Bit 1 of Blue RGB signals. Pad powered from pin VCCIO2.
-	-	41	41	B0	O	Bit 0 of Blue RGB signals. Pad powered from pin VCCIO2.
36	36	42	42	GND	P	Ground
37	37	43	43	G7	O	Bit 7 of Green RGB signals. Pad powered from pin VCCIO2.

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38	38	44	44	G6	O	Bit 6 of Green RGB signals. Pad powered from pin VCCIO2.
39	39	45	45	G5	O	Bit 5 of Green RGB signals. Pad powered from pin VCCIO2.
40	40	46	46	G4	O	Bit 4 of Green RGB signals. Pad powered from pin VCCIO2.
41	41	47	47	G3	O	Bit 3 of Green RGB signals. Pad powered from pin VCCIO2.
42	42	48	48	G2	O	Bit 2 of Green RGB signals. Pad powered from pin VCCIO2.
-	-	49	49	G1	O	Bit 1 of Green RGB signals. Pad powered from pin VCCIO2.
-	-	50	50	G0	O	Bit 0 of Green RGB signals. Pad powered from pin VCCIO2.
43	43	51	51	R7	O	Bit 7 of Red RGB signals. Pad powered from pin VCCIO2.
44	44	52	52	R6	O	Bit 6 of Red RGB signals. Pad powered from pin VCCIO2.
45	45	53	53	R5	O	Bit 5 of Red RGB signals. Pad powered from pin VCCIO2.
46	46	54	54	R4	O	Bit 4 of Red RGB signals. Pad powered from pin VCCIO2.
47	47	55	55	R3	O	Bit 3 of Red RGB signals. Pad powered from pin VCCIO2.
48	48	56	56	R2	O	Bit 2 of Red RGB signals. Pad powered from pin VCCIO2.
EP	EP	EP	EP	GND	P	Ground. Exposed thermal pad.

Note:

P : Power or ground

I : Input

O : Output

OD : Open drain output

I/O : Bi-direction Input and Output

AI/O: Analog Input and Output

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4 Function Description

The FT81X is a single chip, embedded video controller with the following function blocks:

- Quad SPI Host Interface
- System Clock
- Graphics Engine
- Parallel RGB video interface
- Audio Engine
- Touch-screen support and interface
- Power Management

The functions for each block are briefly described in the following subsections.

4.1 Quad SPI Host Interface

The FT81X uses a quad serial parallel interface (QSPI) to communicate with host microcontrollers and microprocessors.

4.1.1 QSPI Interface

The QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported. Refer to section 6.3.2 for detailed timing specification.The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD data bus modes.

By default the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH. The table below depicts the setting.

Channel Mode	REG_SPI_WIDTH[1:0]
SINGLE – default mode	00
DUAL	01
QUAD	10
Undefined	11

With DUAL/QUAD channel modes, the SPI data ports are now unidirectional. In these modes, each SPI transaction (signified by CS_N going active low) will begin with the data ports set as inputs.

Hence, for writing to the FT81X, the protocol will operate as in FT800, with "WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ …" The write operation is considered complete when CS_N goes inactive high.

For reading from the FT81X, the protocol will still operate as in FT800, with "RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ". However as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the FT81X. Therefore it is important that the firmware controlling the SPI master changes the SPI master data port direction to "input" after transmitting Addr0. The FT81X will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the FT81X will reset all its data ports' direction to input once CS_N goes inactive high (i.e. at the end of the current SPI master transaction).

The diagram depicts the behaviour of both the SPI master and slave in the master read case.

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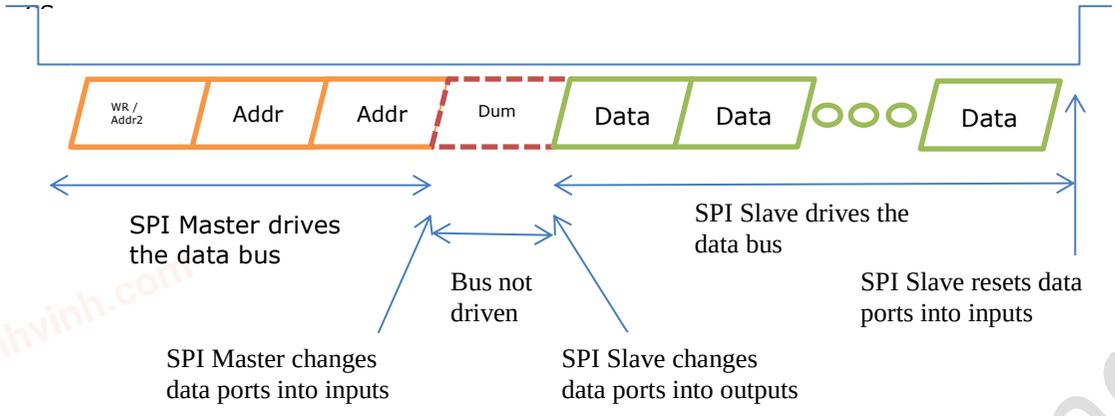


Figure 4-1 SPI master and slave in the master read case

In the DUAL channel mode, MISO (MSB) and MOSI are used while in the QUAD channel mode. IO3 (MSB), IO2, MISO and MOSI are used.

Figure 4-2 illustrates a direct connection to a 1.8-3.3V IO MPU/MCU with single SPI interface.

Figure 4-3 illustrates a direct connection to a 1.8-3.3V IO MPU/MCU with Quad SPI interface.

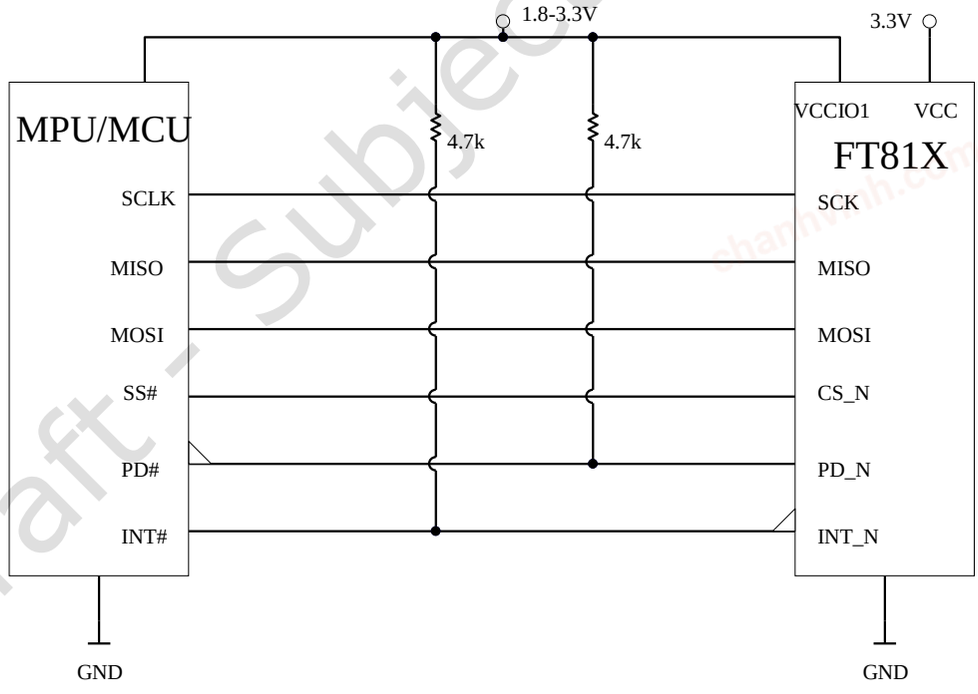


Figure 4-2 Single SPI Interface connection

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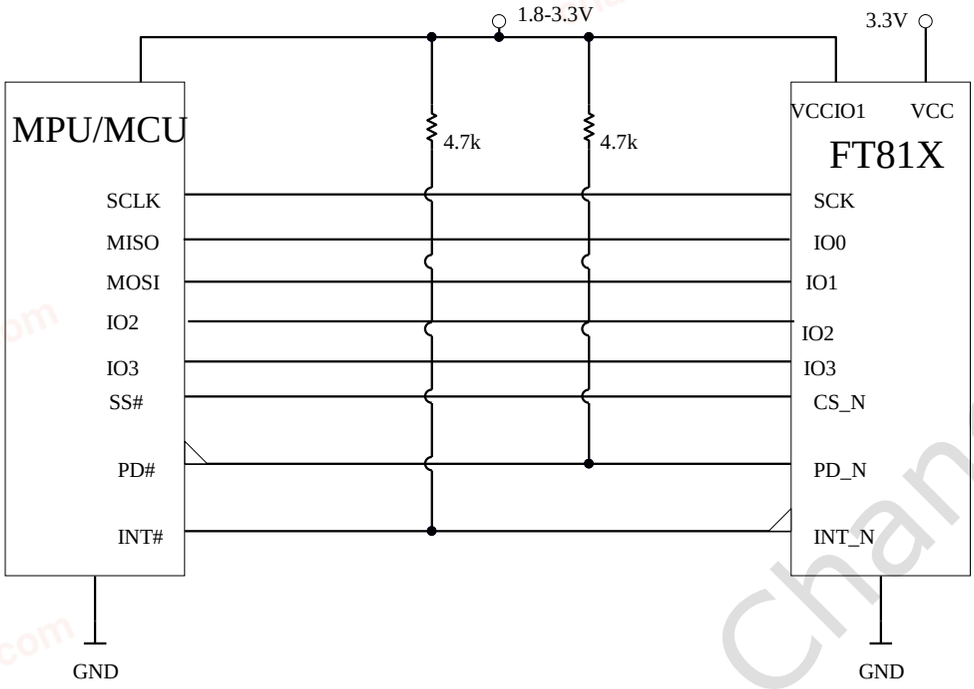


Figure 4-3 Quad SPI Interface connection

4.1.2 Serial Data Protocol

The FT81X appears to the host MPU/MCU as a memory-mapped SPI device. The host communicates with the FT81X using reads and writes to a large (4 megabyte) address space. Within this address space are dedicated areas for graphics, audio and touch control. Refer to section 5 for the detailed memory map.

The host reads and writes the FT81X address space using SPI transactions. These transactions are memory read, memory write and command write. Serial data is sent by the most significant bit first.

Each transaction starts with CS_N goes low, and ends when CS_N goes high. There's no limit on data length within one transaction, as long as the memory address is continuous.

4.1.3 Host Memory Read

For SPI memory read transactions, the host sends two zero bits, followed by the 22-bit address. This is followed by a dummy byte. After the dummy byte, the FT81X responds to each host byte with read data bytes.

Table 4-1 Host memory read transaction

7	6	5	4	3	2	1	0	
0	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Data

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Byte *n*

4.1.4 Host Memory Write

For SPI memory write transactions, the host sends a '1' bit and '0' bit, followed by the 22-bit address. This is followed by the write data.

Table 4-2 Host memory write transaction

7	6	5	4	3	2	1	0	
1	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Byte 0								Write Data
Byte *n*								

4.1.5 Host Command

When sending a command, the host transmits a 3 byte command. Table 4-4 Host Command Table lists all the host command functions.

Note: ACTIVE command is generated by a dummy memory read from address 0 when FT81X is in sleep or standby mode.

For SPI command transactions, the host sends a '0' bit and '1' bit, followed by the 6-bit command code. The 2nd byte can be either 00h, or the parameter of that command. The 3rd byte is fixed at 00h.

All SPI commands except the 3 system reset can only be executed when the SPI is in the Single channel mode. They will be ignored when the SPI is in either Dual or Quad channel mode.

Some commands are used to configure the device and these configurations will be reset upon receiving the SPI POWERDOWN command, except those that configure the pad state during power down. These commands will be sticky unless reconfigured or an overall system shut down occurs.

All SPI commands except the 3 system reset can only be executed when SPI is in the Single channel mode. They will be ignored when SPI is in either DUAL or QUAD channel mode.

Some commands are used to configure the device and these configurations will be reset upon receiving SPI PWRDOWN command, except those that configure the pad state during power down. They will be sticky unless reconfigured or an overall system shut down occurs.

Table 4-3 Host command transaction

7	6	5	4	3	2	1	0	
0	1	Command [5:0]						Byte 0
Parameter for the command								Byte 1
0	0	0	0	0	0	0	0	Byte 2

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Table 4-4 Host Command Table

<table>
<tr><th>1st Byte</th><th>2nd byte</th><th>3rd byte</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="5">Power Modes</td></tr>
<tr><td>00000000b</td><td>00000000b</td><td>00000000b</td><td>00h
ACTIVE</td><td>Switch from Standby/Sleep modes to active mode. Dummy read from address 0 generates ACTIVE command.</td></tr>
<tr><td>01000001b</td><td>00000000b</td><td>00000000b</td><td>41h
STANDBY</td><td>Put FT81X core to standby mode. Clock gate off, PLL and Oscillator remain on (default). ACTIVE command to wake up.</td></tr>
<tr><td>01000010b</td><td>00000000b</td><td>00000000b</td><td>42h
SLEEP</td><td>Put FT81X core to sleep mode. Clock gate off, PLL and Oscillator off. ACTIVE command to wake up.</td></tr>
<tr><td>01000011b</td><td>00000000b</td><td>00000000b</td><td>43h
PWRDOWN</td><td rowspan="2">Switch off 1.2V core voltage to the digital core circuits. Clock, PLL and Oscillator off. SPI is alive. ACTIVE command to wake up.</td></tr>
<tr><td>01010000b</td><td>00000000b</td><td>00000000b</td><td>50h
PWRDOWN</td></tr>
<tr><td>01000100b</td><td>xx</td><td>00000000b</td><td>49h
PDROMSADC</td><td>Select power down ROMs and ADC; Byte2 determines which to power down or up. A 1 on a bit powers down the corresponding block; a 0 on a bit powers up the corresponding block. As these are not readable, the host must remember the setting on its own.
<table>
<tr><td>Byte2[7]</td><td>1 powers down main rom;</td></tr>
<tr><td>Byte2[6]</td><td>1 powers down rcosatan rom</td></tr>
<tr><td>Byte2[5]</td><td>1 powers down sample rom;</td></tr>
<tr><td>Byte2[4]</td><td>1 powers down jaboot rom;</td></tr>
<tr><td>Byte2[3]</td><td>1 powers down j1boot rom;</td></tr>
<tr><td>Byte2[2]</td><td>reserved;</td></tr>
<tr><td>Byte2[1]</td><td>reserved;</td></tr>
<tr><td>Byte2[0]</td><td>1 powers down ADC;</td></tr>
</table></td></tr>
<tr><td colspan="5">Clock Switching</td></tr>
<tr><td>01000100b</td><td>00000000b</td><td>00000000b</td><td>44h
CLKEXT</td><td>Select PLL input from external Crystal oscillator or external input clock.</td></tr>
<tr><td>01001000b</td><td>00000000b</td><td>00000000b</td><td>48h
CLKINT</td><td>Select PLL input from Internal relaxation oscillator (default).</td></tr>
<tr><td>01100001b
01100010b</td><td>xx</td><td>00000000b</td><td>61h/62h
CLKSEL</td><td>This command will only be effective when the PLL is stopped (SLEEP mode).
For compatibility to FT800/FT801, set Byte2 to 0x00. This will set the PLL clock back to default (60 MHz).
If the second byte is non-zero, then
<table>
<tr><td>Byte2[5:0]</td><td>sets the clock frequency</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>1st Byte</th><th>2nd byte</th><th>3rd byte</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>
<table>
<tr><td>0</td><td>Set to default clock speed</td></tr>
<tr><td>1</td><td>Illegal</td></tr>
<tr><td>2 to 5</td><td>2 to 5 times the osc frequency (i.e. 24 to 60MHz with 12MHz osc)</td></tr>
</table>
<table>
<tr><td>Byte2[7:6]</td><td>sets the PLL range</td></tr>
<tr><td>0</td><td>When Byte2[5:0] = 2, 3</td></tr>
<tr><td>1</td><td>When Byte2[5:0] = 4, 5</td></tr>
</table>
</td></tr>
<tr><td colspan="5">Miscellaneous</td></tr>
<tr><td>01101000b</td><td>00000000b</td><td>00000000b</td><td>68h
CORERST</td><td>Send reset pulse to FT81X core. The behaviour is the same as POR except that settings done through SPI commands will not be affected</td></tr>
<tr><td>01101000b</td><td>00000010b</td><td>00000000b</td><td>68h
RST_ON</td><td>This will hold the system reset active.</td></tr>
<tr><td>01101000b</td><td>00100000b</td><td>00000000b</td><td>68h
RST_OFF</td><td>This will release the system reset, and the system will exit reset and behave as after POR except that settings done through SPI commands will not affected</td></tr>
<tr><td>01110000b</td><td>xx</td><td>00000000b</td><td>70h
PADDRIVE</td><td>This will set the drive strength for various pads. For FT800/FT801 compatibility, by default those settings are from the GPIO registers. FT81X supports setting the drive strength via SPI command instead.</td></tr>
<tr><td>01110001b</td><td>xx</td><td>00000000b</td><td>71h
PAD_PD_STATE</td><td>During pseudo power down, all output and inout pads will not be driven. Please refer to the pin table for their default power down state.

These settings will only be effective during power down and will not affect normal operations. Also note that these configuration bits are sticky and, unlike other configuration bits, will not reset to default values upon exiting power down. Only POR will reset them.

Byte2 determines which pad and the setting are to be updated.

Byte2[1:0] determine the pin state.
<table>
<tr><td>Byte2[1:0]</td><td>Pad Setting</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>1st Byte</th><th>2nd byte</th><th>3rd byte</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>
<table>
<tr><td>00</td><td>Float</td><td></td></tr>
<tr><td>01</td><td>Pull-Down</td><td></td></tr>
<tr><td>10</td><td>Pull-Up</td><td></td></tr>
<tr><td>11</td><td>Keep last value</td><td></td></tr>
</table>
Byte2[7:2] determine which pad/pad group to set.
Please refer to the table in PADDRIVE entry.
</td></tr>
<tr><td>01110011b</td><td>xx</td><td>00000000b</td><td>73h
ADCCFG</td><td>
This will set the ADC sampling configuration. It’s default to 2’h01.
Byte2[1:0] determines the sampling configuration.
<table>
<tr><td>Byte2[7:2]</td><td>Byte2[1:0]</td><td></td></tr>
<tr><td>6’h00</td><td>2’h0</td><td>1 c
samp</td></tr>
<tr><td>6’h00</td><td>2’h1</td><td>2 cl
samp</td></tr>
<tr><td>6’h00</td><td>2’h2</td><td>3 cl
samp</td></tr>
<tr><td>6’h00</td><td>2’h3</td><td>4 cl
samp</td></tr>
</table>
</td></tr>
</table>

NOTE: Any command code not specified is reserved and should not be used by the software

4.1.6 Interrupts

The interrupt output pin is enabled by REG_INT_EN. When REG_INT_EN is 0, INT_N is tri-state (pulled to high by external pull-up resistor). When REG_INT_EN is 1, INT_N is driven low when any of the interrupt flags in REG_INT_FLAGS are high, after masking with REG_INT_MASK. Writing a ‘1’ in any bit of REG_INT_MASK will enable the corresponding interrupt. Each bit in REG_INT_FLAGS is set by a corresponding interrupt source. REG_INT_FLAGS is readable by the host at any time, and clears when read.

Table 4-5 Interrupt Flags bit assignment

Bit	7	6	5	4
Interrupt Sources	CONVCOMPLETE	CMDFLAG	CMDEMPTY	PLAYBACK
Conditions	Touch-screen conversions completed	Command FIFO flag	Command FIFO empty	Audio playback ended

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Bit	3	2	1	0
Interrupt Sources	SOUND	TAG	TOUCH	SWAP
Conditions	Sound effect ended	Touch-screen tag value change	Resistive touch detected	Display list swap occurred

4.2 System Clock

4.2.1 Clock Source

The FT81X can be configured to use any of the three clock sources for system clock:

- Internal relaxation oscillator clock
- External 12MHz crystal
- External 12MHz square wave clock

Figure 4-4, Figure 4-5 and Figure 4-6**Error! Reference source not found.** show the pin connections for these clock options.

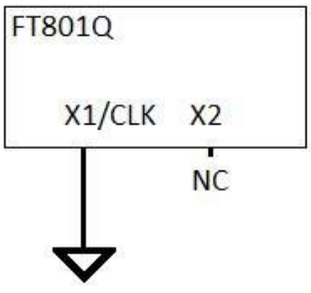


Figure 4-4 Internal relaxation oscillator connection

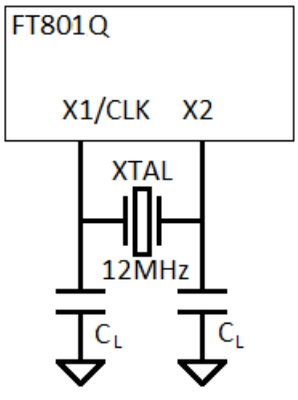


Figure 4-5 Crystal oscillator connection

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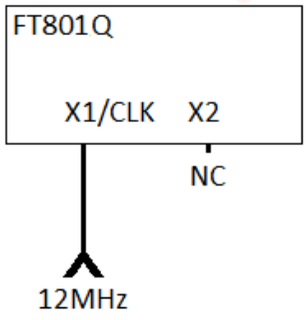


Figure 4-6 External clock input

4.2.2 Phase Locked Loop

The internal PLL takes an input clock from the oscillator, and generates clocks to all internal circuits, including the graphics engine, audio engine and touch engine.

4.2.3 Clock Enable

Upon power-on the FT81X enters standby mode. The internal relaxation oscillator is selected for the PLL clock source. The system clock will be enabled when the following step is executed:

- Host sends an "ACTIVE" command (dummy read at address 0)

If the application chooses to use the external clock source(12MHz crystal or clock), the following steps shall be executed:

- Host sends an "ACTIVE" command (dummy read at address 0)
- Host sends an "CLKEXT" command
- Host writes to REG_PCLK with non-zero value (ie 2)

4.2.4 Clock Frequency

By default the system clock is 60MHz when the input clock is 12MHz. The host is allowed to switch the system clock to other frequencies (48MHz, 36MHz, 24MHz) by the host command "CLKSEL". The clock switching command shall be sent in SLEEP mode only.

4.3 Graphics Engine

4.3.1 Introduction

The graphics engine executes the display list once for every horizontal line. It executes the primitive objects in the display list and constructs the display line buffer. The horizontal pixel content in the line buffer is updated if the object is visible at the horizontal line.

Main features of the graphics engine are:

- The primitive objects supported by the graphics processor are: lines, points, rectangles, bitmaps (comprehensive set of formats), text display, plotting bar graph, edge strips, and line strips, etc.
- Operations such as stencil test, alpha blending and masking are useful for creating a rich set of effects such as shadows, transitions, reveals, fades and wipes.
- Anti-aliasing of the primitive objects (except bitmaps) gives a smoothing effect to the viewer.
- Bitmap transformations enable operations such as translate, scale and rotate.
- Display pixels are plotted with $1/16^{th}$ pixel precision.
- Four levels of graphics states
- Tag buffer detection

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The graphics engine also supports customized built-in widgets and functionalities such as jpeg decode, screen saver, calibration etc. The graphics engine interprets commands from the MPU host via a 4 Kbyte FIFO in the FT81X memory at RAM_CMD. The MPU/MCU writes commands into the FIFO, and the graphics engine reads and executes the commands. The MPU/MCU updates the register REG_CMD_WRITE to indicate that there are new commands in the FIFO, and the graphics engine updates REG_CMD_READ after commands have been executed.

Main features supported are:

- Drawing of widgets such as buttons, clock, keys, gauges, text displays, progress bars, sliders, toggle switches, dials, gradients, etc.
- JPEG and motion-JPEG decode
- Inflate functionality (zlib inflate is supported)
- Timed interrupt (generate an interrupt to the host processor after a specified number of milliseconds)
- In built animated functionalities such as displaying logo, calibration, spinner, screen saver and sketch
- Snapshot feature to capture the current graphics display

For a complete list of graphics engine display commands and widgets refer to FT81X_Series_Programmer_Guide [FTDI Document FT_00xxxx], Chapter 4.

4.3.2 ROM and RAM Fonts

The FT81X has built in ROM character bitmaps as font metrics. The graphics engine can use these metrics when drawing text fonts. There are a total of 19 ROM fonts, numbered with font handle 16-34. The user can define and load customized font metrics into RAM_G, which can be used by display command with handle 0-18.

Each font metric block has a 148 byte font table which defines the parameters of the font and the pointer of font image. The font table format is shown in Table 4-6.

Table 4-6 Font table format

Address Offset	Size(byte)	Parameter Description
0	128	width of each font character, in pixels
128	4	font bitmap format, for example L1, L4 or L8
132	4	font line stride, in bytes
136	4	font width, in pixels
140	4	font height, in pixels
144	4	pointer to font image data in memory

The ROM fonts are stored in the memory space ROM_FONT. The ROM font table is also stored in the ROM. The starting address of the ROM font table for font index 16 is stored at ROM_FONT_ADDR, with other font tables following. The ROM font table and individual character width (in pixel) are listed in Table 4-7 through Table 4-9. Font index 16, 18 and 20-31 are for basic ASCII characters (code 0-127), while font index 17 and 19 are for Extended ASCII characters (code 128-255). The character width for font index 17 or 19 is fixed at 8 pixels for any of the Extended ASCII characters.

Table 4-7 ROM font table

Font Index	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
Font format	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L4	L4	L4	L4	L4	L4	L4	L4	L4
Line stride	1	1	1	1	2	2	2	3	3	4	6	8	9	11	14	18	23	30	39
Font width	8	8	8	8	10	13	14	17	24	30	12	16	18	22	28	36	46	60	78
Font height	8	8	16	16	13	17	20	22	29	38	16	20	25	28	36	49	63	83	108

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Image pointer start address (hex)	2FF7FC	2FFBFC	2FE7FC	2FEBFC	2FDAFC	2FCD3C	2FBD7C	2FA17C	2F7E3C	2F3D1C	2F181C	2ED61C	2E799C	2DFBBC	2D263C	2BAC3C	2945FC	251E1C	1E1B5C

Table 4-8 ROM font ASCII character width in pixels

Font Index =>			16	18	20	21	22	23	24	25	26	27	28	29	30	31
ASCII Character width in pixels	0	NULL	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	1	SOH	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2	STX	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	ETX	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	4	EOT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	5	ENQ	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	6	ACK	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	7	BEL	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	8	BS	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	9	HT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	10	LF	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	11	VT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	12	FF	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	13	CR	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	14	SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	15	SI	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	16	DLE	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	17	DC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	18	DC2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	19	DC3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	20	DC4	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	21	NAK	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	22	SYN	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	23	ETB	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	24	CAN	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	25	EM	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	26	SUB	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	27	ESC	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	28	FS	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	29	GS	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	30	RS	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	31	US	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	32	space	8	8	3	4	5	5	6	9	3	4	5	6	8	10
	33	!	8	8	3	4	5	6	6	9	4	4	6	6	8	11
	34	"	8	8	4	5	6	5	8	12	5	6	8	9	11	15
	35	#	8	8	6	8	9	10	14	19	9	11	13	15	19	26
	36	$	8	8	6	8	9	10	13	18	8	10	12	14	18	24
	37	%	8	8	9	12	14	16	22	29	10	12	15	18	23	31
	38	&	8	8	8	10	11	13	17	22	9	11	13	15	19	26
	39	'	8	8	2	3	3	3	6	6	3	4	5	5	7	9
	40	(	8	8	4	5	6	6	8	11	5	6	7	8	11	14
	41	)	8	8	4	5	6	6	8	11	5	6	7	8	10	14
	42	*	8	8	4	7	6	7	10	13	6	7	9	10	13	18
	43	+	8	8	6	9	10	10	14	19	8	10	12	14	18	24
	44	,	8	8	3	3	4	5	6	9	3	4	5	5	7	9
	45	-	8	8	4	4	5	6	8	11	6	8	9	11	14	19
	46	.	8	8	3	3	4	5	6	9	4	5	6	6	8	11
	47	/	8	8	3	4	5	5	7	9	6	7	9	10	13	17
	48	0	8	8	6	8	9	10	13	18	8	10	12	14	17	24
	49	1	8	8	6	8	9	10	13	18	8	10	12	14	17	24

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Font Index =>		16	18	20	21	22	23	24	25	26	27	28	29	30	31
50	2	8	8	6	8	9	10	13	18	8	10	12	14	17	24
51	3	8	8	6	8	9	10	13	18	8	10	12	14	17	24
52	4	8	8	6	8	9	10	13	18	8	10	12	14	17	24
53	5	8	8	6	8	9	10	13	18	8	10	12	14	17	24
54	6	8	8	6	8	9	10	13	18	8	10	12	14	17	24
55	7	8	8	6	8	9	10	13	18	8	10	12	14	17	24
56	8	8	8	6	8	9	10	13	18	8	10	12	14	17	24
57	9	8	8	6	8	9	10	13	18	8	10	12	14	17	24
58	:	8	8	3	3	4	5	6	9	4	4	5	6	8	11
59	;	8	8	3	4	4	5	6	9	4	4	5	6	8	11
60	<	8	8	6	8	10	10	15	19	7	9	11	12	16	21
61	=	8	8	5	9	10	11	15	19	8	10	12	14	17	24
62	>	8	8	6	8	10	10	15	19	7	9	11	13	16	22
63	?	8	8	6	8	9	10	12	18	7	8	10	11	15	20
64	@	8	8	11	13	17	18	25	34	13	15	19	21	28	38
65	A	8	8	7	9	11	13	17	22	9	11	13	15	20	27
66	B	8	8	7	9	11	13	17	22	9	11	13	15	20	27
67	C	8	8	8	10	12	14	18	24	9	11	13	15	20	27
68	D	8	8	8	10	12	14	18	24	9	12	14	16	21	28
69	E	8	8	7	9	11	13	16	22	8	9	12	13	17	23
70	F	8	8	6	8	10	12	14	20	8	9	12	13	17	23
71	G	8	8	8	11	13	15	19	25	9	12	14	16	21	28
72	H	8	8	8	10	12	14	18	24	10	12	15	17	22	30
73	I	8	8	3	4	4	6	8	9	4	5	6	7	9	12
74	J	8	8	5	7	8	10	13	16	8	9	12	13	17	23
75	K	8	8	7	9	11	13	18	22	9	11	14	15	20	27
76	L	8	8	6	8	9	11	14	18	8	9	12	13	17	23
77	M	8	8	9	12	13	16	21	27	12	15	18	21	27	36
78	N	8	8	8	10	12	14	18	24	10	12	15	17	22	30
79	O	8	8	8	11	13	15	18	25	10	12	14	16	21	29
80	P	8	8	7	9	11	13	16	22	9	11	13	15	20	27
81	Q	8	8	8	11	13	15	18	26	10	12	15	17	22	29
82	R	8	8	7	10	12	14	17	24	9	11	13	15	20	27
83	S	8	8	7	9	11	13	16	22	9	10	13	15	19	26
84	T	8	8	5	9	10	12	16	20	9	10	13	14	19	25
85	U	8	8	8	10	12	14	18	24	9	12	14	16	21	28
86	V	8	8	7	9	11	13	17	22	12	11	14	15	20	27
87	W	8	8	9	13	15	18	22	31	9	15	18	21	27	36
88	X	8	8	7	9	11	13	17	22	9	11	13	15	20	27
89	Y	8	8	7	9	11	13	16	22	8	11	13	15	20	27
90	Z	8	8	7	9	10	12	15	20	4	10	13	14	19	25
91	[	8	8	3	4	5	5	7	9	6	5	6	7	8	11
92	\	8	8	3	4	5	5	7	9	4	7	9	10	13	18
93	]	8	8	3	4	5	5	7	9	6	5	6	6	8	11
94	^	8	8	6	7	8	9	12	16	7	7	9	10	13	18
95	_	8	8	6	8	9	11	14	18	4	8	10	11	15	20
96	`	8	8	3	5	6	4	7	11	8	5	7	8	10	13
97	a	8	8	5	8	9	11	13	18	8	9	12	13	17	23
98	b	8	8	6	7	9	11	14	18	7	10	12	14	18	24
99	c	8	8	5	7	8	10	12	16	8	9	11	13	16	22
100	d	8	8	6	8	9	11	14	18	7	10	12	14	18	24
101	e	8	8	5	8	9	10	13	18	5	9	11	13	16	22
102	f	8	8	4	4	5	6	8	9	8	6	8	9	11	15
103	g	8	8	6	8	9	11	14	18	8	10	12	14	18	24
104	h	8	8	6	8	9	10	13	18	4	10	12	14	18	24
105	i	8	8	2	3	3	4	6	7	4	4	5	6	8	11
106	j	8	8	2	3	4	4	6	7	8	4	5	6	8	11

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Font Index =>			16	18	20	21	22	23	24	25	26	27	28	29	30	31
	107	k	8	8	5	7	8	9	12	16	4	9	11	13	16	22
	108	l	8	8	2	3	3	4	6	7	12	4	5	6	8	11
	109	m	8	8	8	11	14	16	20	27	8	15	18	21	27	37
	110	n	8	8	6	8	9	10	14	18	8	10	12	14	18	24
	111	o	8	8	6	8	9	11	13	18	8	10	12	14	18	24
	112	p	8	8	6	8	9	11	14	18	8	10	12	14	18	24
	113	q	8	8	6	8	9	11	14	18	5	10	12	14	18	24
	114	r	8	8	4	5	5	6	9	11	7	6	7	8	11	15
	115	s	8	8	5	7	8	9	12	16	5	9	11	13	16	22
	116	t	8	8	4	4	5	6	8	9	8	6	7	8	10	13
	117	u	8	8	5	7	9	10	14	18	7	10	12	14	18	24
	118	v	8	8	6	7	8	10	13	16	11	9	11	12	16	21
	119	w	8	8	8	10	12	14	18	23	7	13	16	18	23	32
	120	x	8	8	6	7	8	10	12	16	7	9	11	12	16	21
	121	y	8	8	5	7	8	10	13	16	7	9	11	12	16	21
	122	z	8	8	5	7	8	9	12	16	5	9	11	12	16	21
	123	{	8	8	3	5	6	6	8	11	3	6	7	8	11	14
	124	|	8	8	3	3	4	5	6	9	5	4	5	6	8	10
	125	}	8	8	3	5	6	6	8	11	10	6	7	8	11	14
	126	~	8	8	7	8	10	10	14	19	3	12	14	16	21	29
	127	DEL	8	8	0	0	0	0	0	0	2	4	5	6	8	10

Table 4-9 ROM font Extended ASCII characters

Decimal	Symbol	Decimal	Symbol	Decimal	Symbol	Decimal	Symbol	Decimal	Symbol	Decimal	Symbol	Decimal	Symbol	Decimal	Symbol
128	Ç	144	É	160	á	176	░	192	└	208	ð	224	Ó	240	-
129	ü	145	æ	161	í	177	▒	193	┴	209	Ð	225	ß	241	±
130	é	146	Æ	162	ó	178	▓	194	┬	210	Ê	226	Ô	242	‗
131	â	147	ô	163	ú	179	│	195	├	211	Ë	227	Ò	243	¾
132	ä	148	ö	164	ñ	180	┤	196	─	212	È	228	õ	244	¶
133	à	149	ò	165	Ñ	181	Á	197	┼	213	ı	229	Õ	245	§
134	å	150	û	166	ª	182	Â	198	ã	214	Í	230	µ	246	÷
135	ç	151	ù	167	º	183	À	199	Ã	215	Î	231	þ	247	¸
136	ê	152	ÿ	168	¿	184	©	200	╚	216	Ï	232	Þ	248	°
137	ë	153	Ö	169	®	185	╣	201	╔	217	┘	233	Ú	249	¨
138	è	154	Ü	170	¬	186	║	202	╩	218	┌	234	Û	250	·
139	ï	155	ø	171	½	187	╗	203	╦	219	█	235	Ù	251	¹
140	î	156	£	172	¼	188	╝	204	╠	220	▄	236	ý	252	³
141	ì	157	Ø	173	¡	189	¢	205	═	221	¦	237	Ý	253	²
142	Ä	158	×	174	«	190	¥	206	╬	222	Ì	238	¯	254	■
143	Å	159	ƒ	175	»	191	┐	207	¤	223	▀	239	´	255	nbsp

Note: Font 17 and 19 are extended ASCII characters, with width fixed at 8 pixels for all characters.

Note: All fonts included in the FT81X ROM are widely available to the market-place for general usage, see section nine for specific copyright data and links to the corresponding license agreements.

4.4 Parallel RGB Interface

The RGB parallel interface consists of 23 or 29 signals - DISP, PCLK, VSYNC, HSYNC, DE, 6 or 8 signals each for R, G and B.

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Several registers configure the LCD operation of these signals as follow:

REG_PCLK is the PCLK divisor. The default value is 0, which means the PCLK output is disabled.

PCLK frequency = System Clock frequency / REG_PCLK

PCLK_POL define the clock polarity, with 0 for positive active clock edge, and 1 for negative clock edge.

REG_CSPREAD controls the transition of RGB signals with respect to PCLK active clock edge. When REG_CSPREAD=0, R[7:0],G[7:0] and B[7:0] signals change following the active edge of PCLK. When REG_CSPREAD=1, R[7:0] changes a PCLK clock early and B[7:0] a PCLK clock later, which helps reduce the switching noise.

REG_DITHER enables colour dither; the default is enabled. This option improves the half-tone appearance on displays. Internally, the graphics engine computes the colour values at an 8 bit precision; however, the LCD colour at a lower precision is sufficient. The FT810/FT811 output is only 6 bits per colour in 6:6:6 formats and a 2X2 dither matrix allows the truncated bits to contribute to the final colour values.

REG_OUTBITS gives the bit width of each colour channel, the default is 6, 6, 6 bits for each RGB colour. A lower value means fewer bits are output for each channel allowing dithering on lower precision LCD displays.

REG_SWIZZLE controls the arrangement of the output colour pins, to help the PCB route different LCD panel arrangements. Bit 0 of the register causes the order of bits in each colour channel to be reversed. Bits 1-3 control the RGB order. Setting Bit 1 causes R and B channels to be swapped. Setting Bit 3 allows rotation to be enabled. If Bit 3 is set, then (R,G,B) is rotated right if bit 2 is one, or left if bit 2 is zero.

Table 4-10 REG_SWIZZLE RGB Pins Mapping

REG_SWIZZLE				PINS (FT810/FT811, 6 bits)			PINS (FT812/FT813, 8 bits)		
b3	b2	b1	b0	R7, R6, R5, R4, R3, R2	G7, G6, G5, G4, G3, G2	B7, B6, B5, B4, B3, B2	R7, R6, R5, R4, R3, R2, R1, R0	G7, G6, G5, G4, G3, G2, G1, G0	B7, B6, B5, B4, B3, B2, B1, B0
0	X	0	0	R[7:2]	G[7:2]	B[7:2]	R[7:0]	G[7:0]	B[7:0]
0	X	0	1	R[2:7]	G[2:7]	B[2:7]	R[0:7]	G[0:7]	B[0:7]
0	X	1	0	B[7:2]	G[7:2]	R[7:2]	B[7:0]	G[7:0]	R[7:0]
0	X	1	1	B[2:7]	G[2:7]	R[2:7]	B[0:7]	G[0:7]	R[0:7]
1	0	0	0	B[7:2]	R[7:2]	G[7:2]	B[7:0]	R[7:0]	G[7:0]
1	0	0	1	B[2:7]	R[2:7]	G[2:7]	B[0:7]	R[0:7]	G[0:7]
1	0	1	0	G[7:2]	R[7:2]	B[7:2]	G[7:0]	R[7:0]	B[7:0]
1	0	1	1	G[2:7]	R[2:7]	B[2:7]	G[0:7]	R[0:7]	B[0:7]
1	1	0	0	G[7:2]	B[7:2]	R[7:2]	G[7:0]	B[7:0]	R[7:0]
1	1	0	1	G[2:7]	B[2:7]	R[2:7]	G[0:7]	B[0:7]	R[0:7]
1	1	1	0	R[7:2]	B[7:2]	G[7:2]	R[7:0]	B[7:0]	G[7:0]
1	1	1	1	R[2:7]	B[2:7]	G[2:7]	R[0:7]	B[0:7]	G[0:7]

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4.5 Miscellaneous Control

4.5.1 Backlight Control Pin

The backlight dimming control pin (BACKLIGHT) is a pulse width modulated (PWM) signal controlled by two registers: *REG_PWM_HZ* and *REG_PWM_DUTY*. REG_PWM_HZ specifies the PWM output frequency, the range is 250-10000 Hz. REG_PWM_DUTY specifies the duty cycle; the range is 0-128. A value of 0 means that the PWM is completely off and 128 means completely on.
The BACKLIGHT pin will output low when the DISP pin is not enabled (ie logic 0).

4.5.2 DISP Control Pin

The DISP pin is a general purpose output that can be used to enable or as a reset control to LCD display panel. The pin is controlled by writing to Bit 7 of REG_GPIO register.

4.5.3 General Purpose IO pins

Depending on the package, the FT81X can be configured to use up to 4 GPIO pins. These GPIO pins are controlled by the REG_GPIOX_DIR and REG_GPIOX registers. Alternatively the GPIO0 and GPIO1 pins can also be controlled by REG_GPIO_DIR and REG_GPIO to maintain backward compatible to FT800/FT801.

When the QSPI is enabled in Quad mode, GPIO0/IO2 and GPIO1/IO3 pins are used as data lines of the QSPI.

4.5.4 Pins Drive Current Control

The output drive current of output pins can be changed as per the following table by writing to bit[6:2] of REG_GPIO register:

Table 4-11 Output drive current selection

REG_GPIO	Bit[6:5]				Bit[4]		Bit[3:2]			
Value	00b#	01b	10b	11b	0b#	1b	00b#	01b	10b	11b
Drive Current	5mA	10mA	15mA	20mA	5mA	10mA	5mA	10mA	15mA	20mA
Pins	GPIO1 GPIO0				PCLK DISP VSYNC HSYNC DE R7..R0 G7..G0 B7..B0 BACKLIGHT		MISO INT_N			

Note: #Default value

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4.6 Audio Engine

FT81X provides mono audio output through a PWM output pin, AUDIO_L. It outputs two audio sources, the sound synthesizer and audio file playback.

4.6.1 Sound Synthesizer

A sound processor, AUDIO ENGINE, generates the sound effects from a small ROM library of waves table. To play a sound effect listed in Table 4.3, load the REG_SOUND register with a code value and write 1 to the REG_PLAY register. The REG_PLAY register reads 1 while the effect is playing and returns a '0' when the effect ends. Some sound effects play continuously until it is interrupted or commanded to play the next sound effect. To interrupt an effect, write a new value to REG_SOUND and REG_PLAY registers; e.g. write 0 (Silence) to REG_SOUND and 1 to PEG_PLAY to stop the sound effect.

The sound volume is controlled by register REG_VOL_SOUND. The 16-bit REG_SOUND register takes an 8-bit sound in the low byte. For some sounds, marked "pitch adjust" in the table below, the high 8 bits contain a MIDI note value. For these sounds, note value of zero indicates middle C. For other sounds the high byte of REG_SOUND is ignored.

Table 4-12 Sound Effect

Value	Effect	Continuous	Pitch adjust
00h	Silence	Y	N
01h	square wave	Y	Y
02h	sine wave	Y	Y
03h	sawtooth wave	Y	Y
04h	triangle wave	Y	Y
05h	Beeping	Y	Y
06h	Alarm	Y	Y
07h	Warble	Y	Y
08h	Carousel	Y	Y
10h	1 short pip	N	Y
11h	2 short pips	N	Y
12h	3 short pips	N	Y
13h	4 short pips	N	Y
14h	5 short pips	N	Y
15h	6 short pips	N	Y
16h	7 short pips	N	Y
17h	8 short pips	N	Y
18h	9 short pips	N	Y
19h	10 short pips	N	Y
1Ah	11 short pips	N	Y
1Bh	12 short pips	N	Y
1Ch	13 short pips	N	Y
1Dh	14 short pips	N	Y
1Eh	15 short pips	N	Y
1Fh	16 short pips	N	Y
23h	DTMF #	Y	N
2Ch	DTMF *	Y	N
30h	DTMF 0	Y	N
31h	DTMF 1	Y	N
32h	DTMF 2	Y	N
33h	DTMF 3	Y	N
34h	DTMF 4	Y	N
35h	DTMF 5	Y	N
36h	DTMF 6	Y	N
37h	DTMF 7	Y	N
38h	DTMF 8	Y	N
39h	DTMF 9	Y	N
40h	harp	N	Y
41h	xylophone	N	Y
42h	tuba	N	Y
43h	glockenspiel	N	Y
44h	organ	N	Y
45h	trumpet	N	Y
46h	piano	N	Y
47h	chimes	N	Y
48h	music box	N	Y
49h	bell	N	Y
50h	click	N	N
51h	switch	N	N
52h	cowbell	N	N
53h	notch	N	N
54h	hihat	N	N
55h	kickdrum	N	N
56h	pop	N	N
57h	clack	N	N
58h	chack	N	N
60h	mute	N	N
61h	unmute	N	N

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Table 4-13 MIDI Note Effect

MIDI note	ANSI note	Freq (Hz)
21	A0	27.5
22	A#0	29.1
23	B0	30.9
24	C1	32.7
25	C#1	34.6
26	D1	36.7
27	D#1	38.9
28	E1	41.2
29	F1	43.7
30	F#1	46.2
31	G1	49.0
32	G#1	51.9
33	A1	55.0
34	A#1	58.3
35	B1	61.7
36	C2	65.4
37	C#2	69.3
38	D2	73.4
39	D#2	77.8
40	E2	82.4
41	F2	87.3
42	F#2	92.5
43	G2	98.0
44	G#2	103.8
45	A2	110.0
46	A#2	116.5
47	B2	123.5
48	C3	130.8
49	C#3	138.6
50	D3	146.8
51	D#3	155.6
52	E3	164.8
53	F3	174.6
54	F#3	185.0
55	G3	196.0
56	G#3	207.7
57	A3	220.0
58	A#3	233.1
59	B3	246.9
60	C4	261.6
61	C#4	277.2
62	D4	293.7
63	D#4	311.1
64	E4	329.6
65	F4	349.2
66	F#4	370.0
67	G4	392.0
68	G#4	415.3
69	A4	440.0
70	A#4	466.2
71	B4	493.9
72	C5	523.3
73	C#5	554.4
74	D5	587.3
75	D#5	622.3
76	E5	659.3
77	F5	698.5
78	F#5	740.0
79	G5	784.0
80	G#5	830.6
81	A5	880.0
82	A#5	932.3
83	B5	987.8
84	C6	1046.5
85	C#6	1108.7
86	D6	1174.7
87	D#6	1244.5
88	E6	1318.5
89	F6	1396.9
90	F#6	1480.0
91	G6	1568.0
92	G#6	1661.2
93	A6	1760.0
94	A#6	1864.7
95	B6	1975.5
96	C7	2093.0
97	C#7	2217.5
98	D7	2349.3
99	D#7	2489.0
100	E7	2637.0
101	F7	2793.8
102	F#7	2960.0
103	G7	3136.0
104	G#7	3322.4
105	A7	3520.0
106	A#7	3729.3
107	B7	3951.1
108	C8	4186.0

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4.6.2 Audio Playback

The FT81X can play back recorded sound through its audio output. To do this, load the original sound data into the FT81X's RAM, and set registers to start the playback.

The registers controlling audio playback are:

REG_PLAYBACK_START:	the start address of the audio data
REG_PLAYBACK_LENGTH:	the length of the audio data, in bytes
REG_PLAYBACK_FREQ:	the playback sampling frequency, in Hz
REG_PLAYBACK_FORMAT:	the playback format, one of LINEAR SAMPLES, uLAW SAMPLES, or ADPCM SAMPLES
REG_PLAYBACK_LOOP:	if zero, the sample is played once. If one, the sample is repeated indefinitely
REG_PLAYBACK_PLAY:	a write to this location triggers the start of audio playback, regardless of writing '0' or '1'. Read back '1' when playback is ongoing, and '0' when playback finishes
REG_VOL_PB:	playback volume, 0-255

The mono audio format supported is 8-bits PCM, 8-bits uLAW and 4-bits IMA-ADPCM. For ADPCM_SAMPLES, each sample is 4 bits, so two samples are packed per byte, the first sample is in bits 0-3 and the second is in bits 4-7.

The current audio playback read pointer can be queried by reading the REG_PLAYBACK_READPTR. Using a large sample buffer, looping, and this read pointer, the host MPU/MCU can supply a continuous stream of audio.

4.7 Touch-Screen Engine

The FT81X touch-screen engine supports either resistive or capacitive touch panels. FT810 and FT812 support resistive touch, while FT811 and FT813 support capacitive touch.

4.7.1 Resistive Touch Control

The resistive touch-screen consists of a touch screen engine, ADC, Axis-switches, and ADC input multiplexer. The touch screen engine reads commands from the memory map register and generates the required control signals to the axis-switches and inputs mux and ADC. The ADC data are acquired and processed and updated in the respective register for the MPU/MCU to read.

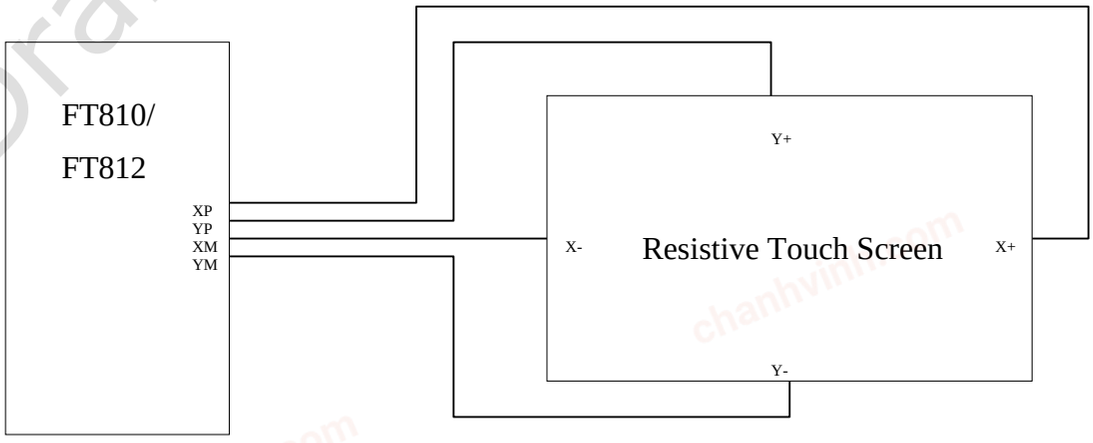


Figure 4-7 Resistive Touch screen connection

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The host controls the TOUCH SCREEN ENGINE operation mode by writing the REG_TOUCH_MODE.

Table 4-14 Touch Controller Operating Mode

REG_TOUCH_MODE	Mode	Description
0	OFF	Acquisition stopped, only touch detection interrupt is still valid.
1	ONE-SHOT	Perform acquisition once every time MPU write '1' to REG_TOUCH_MODE.
2	FRAME-SYNC	Perform acquisition for every frame sync (~60 data acquisition/second.
3	CONTINUOUS	Perform acquisition continuously at approximately 1000 data acquisition / second.

The Touch Screen Engine captures the raw X and Y coordinate and writes to register REG_TOUCH_RAW XY. The range of these values is 0-1023. If the touch screen is not being pressed, both registers read 65535 (FFFFh).

These touch values are transformed into screen coordinates using the matrix in registers REG_TOUCH_TRANSFORM_A-F. The post-transform coordinates are available in register REG_TOUCH_SCREEN_XY. If the touch screen is not being pressed, both registers read -32768 (8000h). The values for REG TOUCH TRANSFORM A-F may be computed using an on-screen calibration process.

If the screen is being touched, the screen coordinates are looked up in the screen's tag buffer, delivering a final 8-bit tag value, in REG TOUCH TAG. Because the tag lookup takes a full frame, and touch coordinates change continuously, the original (x; y) used for the tag lookup is also available in REG_TOUCH_TAG_XY.

Screen touch pressure is available in REG_TOUCH_RZ. The value is relative to the resistance of the touch contact, a lower value indicates more pressure. The register defaults to 32767 when touch is not detected. The REG_TOUCH_THRESHOLD can be set to accept a touch only when the force threshold is exceeded.

4.7.2 Capacitive Touch Control

The Capacitive Touch Screen Engine (CTSE) of the FT81X communicates with the external capacitive touch panel module (CTPM) through an I^2C interface. The CTPM will assert its interrupt line when there is a touch detected. Upon detecting CTP_INT_N line active, the FT81X will read the touch data through I^2C. Up to 5 touches can be reported and stored in FT81X registers. FT81X supports CTPM with FT5x06, FT5x16 or IQS5xx driver chip.

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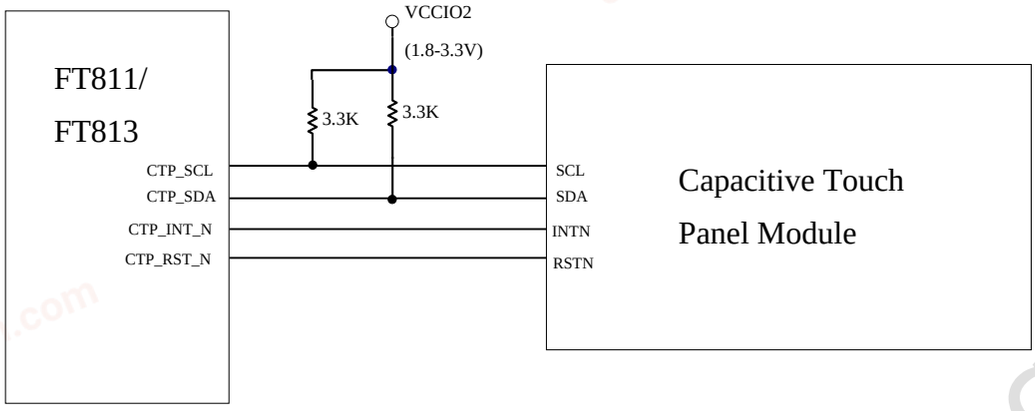


Figure 4-8 Touch screen connection

The host controls the CTSE operation mode by writing the REG_CTOUCH_MODE.

Table 4-15 Touch Controller Operating Mode

REG_CTOUCH_MODE	Mode	Description
0	OFF	Acquisition stopped
1	Reserved	Reserved
2	Reserved	Reserved
3	CONTINUOUS	Perform acquisition continuously at the reporting rate of the connected CTPM.

The FT81X CTSE supports compatibility mode and extended mode. By default the CTSE runs in compatibility mode where the touch system provides an interface very similar to the resistive touch engine. In this mode the same application code can run on FT810/FT812 and FT811/FT813 without alteration. In extended mode, the touch register meanings are modified, and a second set of registers are exposed. These allow multi-touch detection.

4.7.3 Compatibility mode

The CTSE reads the X and Y coordinates from the CTPM and writes to register REG_CTOUCH_RAW_XY. If the touch screen is not being pressed, both registers read 65535 (FFFFh).

These touch values are transformed into screen coordinates using the matrix in registers REG_CTOUCH_TRANSFORM_A-F. The post-transform coordinates are available in register REG_CTOUCH_SCREEN_XY. If the touch screen is not being pressed, both registers read -32768 (8000h). The values for REG_CTOUCH_TRANSFORM_A-F may be computed using an on-screen calibration process.

If the screen is being touched, the screen coordinates are looked up in the screen's tag buffer, delivering a final 8-bit tag value, in REG_TOUCH_TAG. Because the tag lookup takes a full frame, and touch coordinates change continuously, the original (x; y) used for the tag lookup is also available in REG_TOUCH_TAG_XY.

4.7.4 Extended mode

Setting REG_CTOUCH_EXTENDED to 1b'0 enables extended mode. In extended mode a new set of readout registers are available, allowing gesture and up to five touches to be read. There are two classes

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of registers: control registers and status registers. Control registers are written by the MCU. Status registers can be read out by the MCU and the FT81X's hardware tag system.

The five touch coordinates are packed in REG_CTOUCH_TOUCH0_XY, REG_CTOUCH_TOUCH1_XY, REG_CTOUCH_TOUCH2_XY, REG_CTOUCH_TOUCH3_XY, REG_CTOUCH4_X and REG_CTOUCH4_Y.

Coordinates stored in these registers are signed 16-bit values, so have range -32768 to 32767. The no-touch condition is indicated by x=y= -32768. These coordinates are already transformed into screen coordinates based on the raw data read from the CTPM, using the matrix in registers REG_CTOUCH_TRANSFORM_A-F. To obtain raw (x,y) coordinates read from CTPM, the user sets the REG_CTOUCH_TRANSFORM_A-F registers to the identity matrix.

The FT81X tag mechanism is implemented by hardware, and can only query a single (x,y) location. REG_TOUCH_TAG always reports the first touch, that is, the (x,y) from REG_CTOUCH_TOUCH0_XY.

4.8 Power Management

4.8.1 Power supply

The FT81X may be operated with a single supply of 3.3V applied to VCC and VCCIO pins. For operation with a host MPU/MCU at a lower supply, connect the VCCIO1 to the MPU IO supply to match the interface voltage. For operation with LCD/touch panels at lower voltages, connect the VCCIO2 to the LCD/touch IO supply.

Table 4-16 Power supply

Symbol	Typical	Description
VCCIO1	1.8V, or 2.5V, or 3.3V	Supply for Host interface digital I/O pins
VCCIO2	1.8V, or 2.5V, or 3.3V	Supply for RGB and touch interface I/O pins
VCC	3.3V	Supply for 3.3V circuits and internal 1.2V regulator
VOUT1V2	1.2V	Supply for digital core. Generated by internal 1.2V regulator

4.8.2 Internal Regulator and POR

The 1.2V internal regulator provides power to the core circuit. A 47kΩ resistor is recommended to pull the PD_N pin up to VCCIO1, together with a 100nF capacitor to ground in order to delay the 1.2V regulator powering up after the VCC and VCCIO are stable.

The 1.2V internal regulator requires a compensation capacitor to be stable. A typical design requires a 4.7uF capacitor with ESR >0.5Ω between the VOUT1V2 to GND pins. Do not connect any load to this pin.

The 1.2V regulator will generate a Power-On-Reset (POR) pulse when the output voltage rises above the POR threshold. The POR will reset all the core digital circuits.

It is possible to use PD_N pin as an asynchronous hardware reset input. Drive PD_N low for at least 5ms and then drive it high will reset the FT81X chip.

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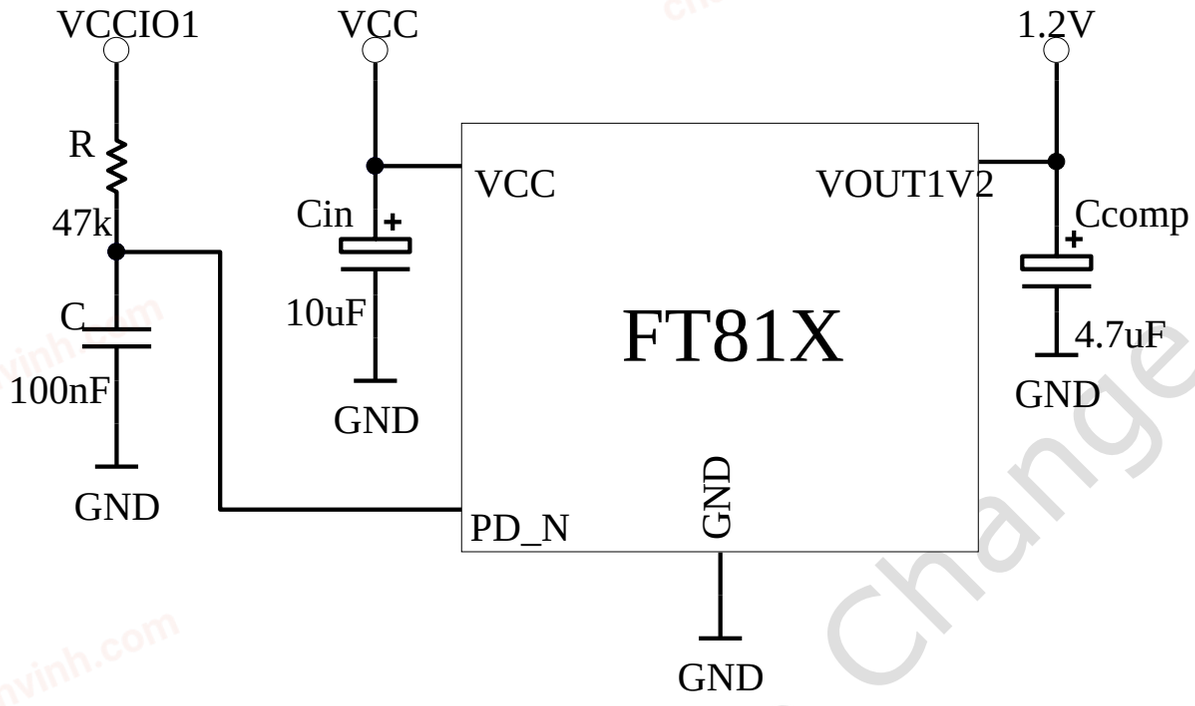


Figure 4-9 1.2V regulator

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4.8.3 Power Modes

When the supply to VCCIO and VCC is applied, the internal 1.2V regulator is powered by VCC. An internal POR pulse will be generated during the regulator power up until it is stable. After the initial power up, the FT81X will stay in the STANDBY state. When needed, the host can set the FT81X to the ACTIVE state by performing a dummy read to address 0. The graphics engine, the audio engine and the touch engine are only functional in the ACTIVE state. To save power the host can send a command to put the FT81X into any of the low power modes: STANDBY, SLEEP and POWERDOWN. In addition, the host is allowed to put the FT81X in POWERDOWN mode by driving the PD_N pin to low, regardless of what state it is currently in. Refer to Figure 4-10 for the power state transitions.

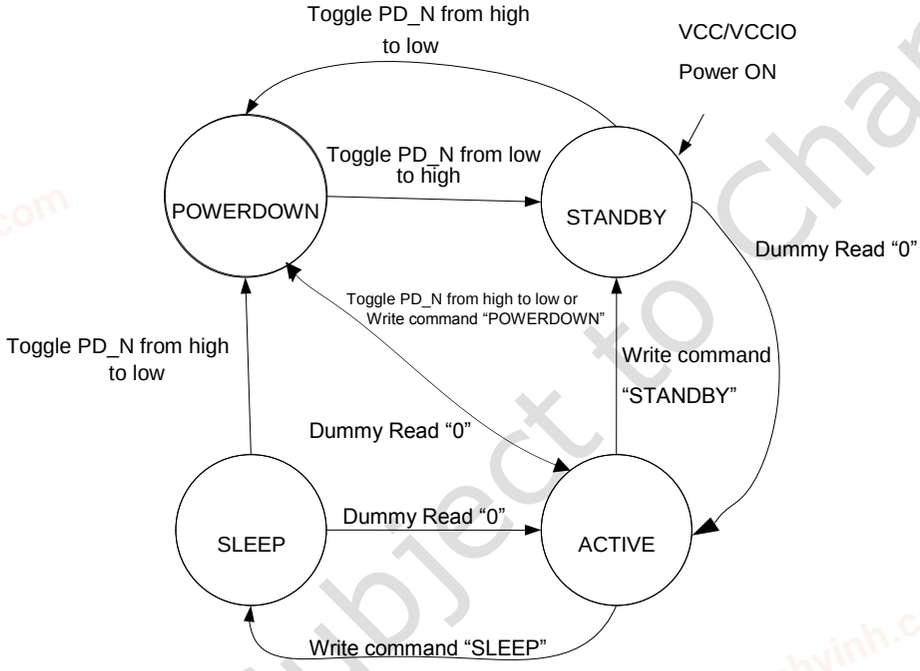


Figure 4-10 Power State Transition

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4.8.3.1 ACTIVE state

In ACTIVE state, the FT81X is in normal operation. The crystal oscillator and PLL are functioning. The system clock applied to the FT81X core engines is enabled.

4.8.3.2 STANDBY state

In STANDBY state, the crystal oscillator and PLL remain functioning; the system clock applied to the FT81X core engines is disabled. All register contents are retained.

4.8.3.3 SLEEP state

In SLEEP state, the crystal oscillator, PLL and system clock applied to the FT81X core engines are disabled. All register contents are retained.

4.8.3.4 POWERDOWN state

In POWERDOWN state, the crystal oscillator, the PLL and the system clock applied to the FT81X core is disabled. The core engines are powered down while the SPI interface for host commands remains functional. All register contents are lost and reset to default when the chip is next switched on. The internal regulator remains on.

4.8.3.5 Wake up to ACTIVE from other power states

When in the POWER DOWN state, if the device enters this state via an SPI command, then only the SPI ACTIVE command will bring the device back to the ACTIVE state, provided PD_N pin is also high. However, if PD_N is used instead, then making PD_N high followed by a SPI ACTIVE command will wake up the device. Upon exiting this state, the device will perform a global reset, and will go through the same power up sequence. All settings from SPI commands will be reset except those that pertain to pin state during power down. The clock enable sequence mentioned in section 4.2.3 shall be executed to properly enable the system clock.

From the SLEEP state, the host MPU reads at memory address 0 to wake the FT81X into the ACTIVE state. The host needs to wait for at least 20ms before accessing any registers or commands. This is to guarantee the crystal oscillator and PLL are up and stable.

From the STANDBY state, the host MPU reads at memory address 0 to wake the FT81X into the ACTIVE state. The host can immediately access any register or command.

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4.8.3.6 Pin Status at Different Power States

The FT81X pin status depends on the power state of the chip. See the following table for more details. At the power transition from ACTIVE to STANDBY or ACTIVE to SLEEP, all pins retain their previous status. The software needs to set AUDIO_L, BACKLIGHT to a known state before issuing power transition commands.

Table 4-17 Pin Status

Pin Name	Default Drive	Reset	Normal	Power Down
AUDIO_L	20mA	Out, Float	Out	Retain
SCK	-	In	In	In
MISO	5mA	Out, Float (SSN = 1)	IO	Out, Float
MOSI	5mA	In	IO	In
CS_N	-	In	In	In
IO2 GPIO0	5mA 5mA	In In	IO IO	Float Float
IO3 GPIO1	5mA 5mA	In In	IO IO	Float Float
GPIO2	5mA	In	IO	Float
INT_N	5mA	OD, Float	OD / Out	Float
PD_N	-	In	In	In
GPIO3	5mA	In	IO	Float
X1/CLK	-	In	In	-
XP	-	IO, Float	IO	Retain
YP	-	IO, Float	IO	Retain
XM	-	IO, Float	IO	Retain
YM	-	IO, Float	IO	Retain
CTP_RST_N	5mA	Out	Out	Low
CTP_INT_N	-	In (internal pull-up)	In (internal pull-up)	In (internal pull-up)
CTP_SCL	20mA	OD	IO	Float
CTP_SDA	20mA	OD	IO	Float
BACKLIGHT	5mA	Out	Out	Retain

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Pin Name	Default Drive	Reset	Normal	Power Down
DE	5mA	Out	Out	Low
VSYNC	5mA	Out	Out	Low
HSYNC	5mA	Out	Out	Low
DISP	5mA	Out	Out	Low
PCLK	5mA	Out	Out	Low
R/G/B	5mA	Out	Out	Low

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5 FT81X Memory Map

All memory and registers in the FT81X core are memory mapped in 22-bits address space with a 2-bit SPI command prefix. Prefix 0'b00 for read and 0'b10 for write to the address space, 0'b01 reserved for Host Commands and 0'b11 undefined. The following are the memory space definition.

Table 5-1 FT81X Memory Map

Start Address	End Address	Size	NAME	Description
00 0000h	0F FFFFh	1024 kB	RAM_G	General purpose graphics RAM
30 0000h	30 1FFFh	8 kB	RAM_DL	Display List RAM
30 2000h	30 2FFFh	380 B	REG_*	Registers
30 8000 h	30 8FFFh	4 kB	RAM_CMD	Command buffer

Note 1: The addresses beyond this table are reserved and shall not be read or written unless otherwise specified.

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5.1 FT81X Registers

Table 5.1 shows the complete list of the FT81X registers. Refer to "**FT81X_Series_Programmers_Guide"** (FTDI Doc FT_00xxxx) Chapter 2 for details of the register function.

Table 5-2 Overview of FT81X Registers

Address	Register Name	Bits	Access	Reset value	Description
302000h	REG_ID	8	r/o	7Ch	Identification register, always reads as 7Ch
302004h	REG_FRAMES	32	r/o	00000000h	Frame counter, since reset
302008h	REG_CLOCK	32	r/o	00000000h	Clock cycles, since reset
30200Ch	REG_FREQUENCY	27	r/w	3938700h	Main clock frequency
302010h	REG_RENDERMODE	1	r/w	0h	Rendering mode: 1 = normal, 1 = single-line
302014h	REG_SNAPY	11	r/w	000h	Scanline select for RENDERMODE 1
302018h	REG_SNAPSHOT	1	r/w	0h	Trigger for RENDERMODE 1
30201Ch	REG_SNAPSHOT_FORMAT	6	r/w	20h	Pixel format for scanline readout
302020h	REG_CPURESET	1	r/w	0h	Graphics, audio and touch engines reset control
302024h	REG_TAP_CRC	32	r/o	-	Live video tap crc. Frame CRC is computed every DL SWAP.
302028h	REG_TAP_MASK	32	r/w	FFFFFFFFh	Live video tap mask
30202Ch	REG_HCYCLE	10	r/w	224h	Horizontal total cycle count
302030h	REG_HOFFSET	10	r/w	02Bh	Horizontal display start offset
302034h	REG_HSIZE	10	r/w	1E0h	Horizontal display pixel count
302038h	REG_HSYNC0	10	r/w	000h	Horizontal sync fall offset
30203Ch	REG_HSYNC1	10	r/w	029h	Horizontal sync rise offset
302040h	REG_VCYCLE	10	r/w	124h	Vertical total cycle count
302044h	REG_VOFFSET	10	r/w	00Ch	Vertical display start offset
302048h	REG_VSIZE	10	r/w	110h	Vertical display line count
30204Ch	REG_VSYNC0	10	r/w	000h	Vertical sync fall offset
302050h	REG_VSYNC1	10	r/w	00Ah	Vertical sync rise offset
302054h	REG_DLSWAP	2	r/w	0h	Display list swap control

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Address	Register Name	Bits	Access	Reset value	Description
302058h	REG_ROTATE	1	r/w	0h	Screen 180 degree rotate
30205Ch	REG_OUTBITS	9	r/w	1B6h	Output bit resolution, 3x3x3 bits
302060h	REG_DITHER	1	r/w	1h	Output dither enable
302064h	REG_SWIZZLE	4	r/w	00h	Output RGB signal swizzle
302068h	REG_CSPREAD	1	r/w	1h	Output clock spreading enable
30206Ch	REG_PCLK_POL	1	r/w	0h	PCLK polarity: 0 = output on PCLK rising edge, 1 = output on PCLK falling edge
302070h	REG_PCLK	8	r/w	00h	PCLK frequency divider, 0 = disable
302074h	REG_TAG_X	9	r/w	000h	Tag query X coordinate
302078h	REG_TAG_Y	9	r/w	000h	Tag query Y coordinate
30207Ch	REG_TAG	8	r/o	00h	Tag query result
302080h	REG_VOL_PB	8	r/w	FFh	Volume for playback
302084h	REG_VOL_SOUND	8	r/w	FFh	Volume for synthesizer sound
302088h	REG_SOUND	16	r/w	0000h	Sound effect select
30208Ch	REG_PLAY	1	r/w	0h	Start effect playback
302090h	REG_GPIO_DIR	8	r/w	00h	GPIO pin direction, 0 = input , 1 = output
302094h	REG_GPIO	8	r/w	00h	GPIO pin value (bit 0,1,7); output pin drive strength(bit 2-6)
302098h	REG_GPIOX_DIR	16	r/w	00h	Extended GPIO pin direction, 0 = input , 1 = output
30209Ch	REG_GPIOX	16	r/w	00h	Extended GPIO pin value (bit 0,1,7); output pin drive strength(bit 2-6)
3020A0h - 3020A4h	Reserved	-	-	-	Reserved
3020A8h	REG_INT_FLAGS	8	r/o	00h	Interrupt flags, clear by read
3020ACh	REG_INT_EN	1	r/w	0h	Global interrupt enable
3020B0h	REG_INT_MASK	8	r/w	FFh	Interrupt enable mask
3020B4h	REG_PLAYBACK_START	20	r/w	00000h	Audio playback RAM start address

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Address	Register Name	Bits	Access	Reset value	Description
3020B8h	REG_PLAYBACK_LENGTH	20	r/w	00000h	Audio playback sample length (bytes)
3020BCh	REG_PLAYBACK_READPTR	20	r/o	-	Audio playback current read pointer
3020C0h	REG_PLAYBACK_FREQ	16	r/w	1F40h	Audio playback sampling frequency (Hz)
3020C4h	REG_PLAYBACK_FORMAT	2	r/w	0h	Audio playback format
3020C8h	REG_PLAYBACK_LOOP	1	r/w	0h	Audio playback loop enable
3020CCh	REG_PLAYBACK_PLAY	1	r/o	0h	Start audio playback
3020D0h	REG_PWM_HZ	14	r/w	00FAh	BACKLIGHT PWM output frequency (Hz)
3020D4h	REG_PWM_DUTY	8	r/w	80h	BACKLIGHT PWM output duty cycle 0=0%, 128=100%
3020D8h	REG_MACRO_0	32	r/w	00000000h	Display list macro command 0
3020DCh	REG_MACRO_1	32	r/w	00000000h	Display list macro command 1
3020E0h – 3020F4h	Reserved	-	-	-	Reserved
3020F8h	REG_CMD_READ	12	r/w	000h	Command buffer read pointer
3020E8h	REG_CMD_WRITE	12	r/w	000h	Command buffer write pointer
302100h	REG_CMD_DL	13	r/w	0000h	Command display list offset
302104h	REG_TOUCH_MODE	2	r/w	3h	Touch-screen sampling mode
302108h	REG_TOUCH_ADC_MODE REG_CTOUCH_EXTENDED	1	r/w	1h	Set Touch ADC mode Set capacitive touch operation mode: 0: extended mode (multi-touch) 1: FT800 compatibility mode (single touch).
30210Ch	REG_TOUCH_CHARGE	16	r/w	1770h	Set touch charge timing
302110h	REG_TOUCH_SETTLE	4	r/w	3h	Set touch settling time
302114h	REG_TOUCH_OVERSAMPLE	4	r/w	7h	Set touch oversample
302118h	REG_TOUCH_RZTHRESH	16	r/w	FFFFh	Touch RX threshold
30211Ch	REG_TOUCH_ RAW_XY REG_CTOUCH_TOUCH1_XY	32	r/o	-	Compatibility mode: touch-screen raw (x-MSB16; y-LSB16) Extended mode: touch-screen screen data for touch 1 (x-MSB16; y-LSB16)

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Address	Register Name	Bits	Access	Reset value	Description
302120h	REG_CTOUCH_TOUCH4_Y	16	r/o	-	Extended mode: touch-screen screen Y data for touch 4
302124h	REG_TOUCH_SCREEN_XY REG_CTOUCH_TOUCH0_XY	32	r/o	-	Compatibility mode: touch-screen screen (x-MSB16; y-LSB16) Extended mode: touch-screen screen data for touch 0 (x-MSB16; y-LSB16)
302128h	REG_TOUCH_TAG_XY	32	r/o	-	Touch-screen screen (x-MSB16; y-LSB16) used for tag 0 lookup
30212Ch	REG_TOUCH_TAG	8	r/o	-	Touch-screen tag result 0
302130h	REG_TOUCH_TAG1_XY	32	r/o	-	Touch-screen screen (x-MSB16; y-LSB16) used for tag 1 lookup
302134h	REG_TOUCH_TAG1	8	r/o	-	Touch-screen tag result 1
302138h	REG_TOUCH_TAG2_XY	32	r/o	-	Touch-screen screen (x-MSB16; y-LSB16) used for tag 2 lookup
30213Ch	REG_TOUCH_TAG2	8	r/o	-	Touch-screen tag result 2
302140h	REG_TOUCH_TAG3_XY	32	r/o	-	Touch-screen screen (x-MSB16; y-LSB16) used for tag 3 lookup
302144h	REG_TOUCH_TAG3	8	r/o	-	Touch-screen tag result 3
302148h	REG_TOUCH_TAG4_XY	32	r/o	-	Touch-screen screen (x-MSB16; y-LSB16) used for tag 4 lookup
30214Ch	REG_TOUCH_TAG4	8	r/o	-	Touch-screen tag result 4
302150h	REG_CTOUCH_TRANSFORM_A	32	r/w	00010000h	Touch-screen transform coefficient (s15.16)
302154h	REG_CTOUCH_TRANSFORM_B	32	r/w	00000000h	Touch-screen transform coefficient (s15.16)
302158h	REG_CTOUCH_TRANSFORM_C	32	r/w	00000000h	Touch-screen transform coefficient (s15.16)
30215Ch	REG_CTOUCH_TRANSFORM_D	32	r/w	00000000h	Touch-screen transform coefficient (s15.16)
302160h	REG_CTOUCH_TRANSFORM_E	32	r/w	00010000h	Touch-screen transform coefficient (s15.16)
302164h	REG_CTOUCH_TRANSFORM_F	32	r/w	00000000h	Touch-screen transform coefficient (s15.16)
302168h	Reserved	-	-	-	Reserved
30216Ch	REG_ANALOG	16	r/o	-	Touch analog in

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Address	Register Name	Bits	Access	Reset value	Description
	REG_CTOUCH_TOUCH4_X REG_PATCHED_TOUCH_FAULT				Extended mode: touch-screen screen X data for touch 4
302170	REG_PATCHED_ANALOG REG_TOUCH_FAULT	16	-	-	Analogue input data on AIN pin Touch short-circuit fault
302174h	REG_BIST_EN	1	r/w	0h	BIST memory mapping enable
302178h	REG_CRC	32	r/o	-	CPU CRC
30217Ch	REG_SPI_EARLY_TX	1	r/w	0h	Enable early TX feature for high-speed
302180h	REG_TRIM	8	r/w	0h	Internal relaxation clock trimming
302184h	REG_ANA_COMP	8	r/w	0h	Analogue control register
302188h	REG_SPI_WIDTH	3	r/w	0h	QSPI bus width setting Bit [2]: extra dummy cycle on read Bit [1:0]: bus width (0=1-bit, 1=2-bit, 2=4-bit)
30218Ch	REG_TOUCH_DIRECT_XY REG_CTOUCH_TOUCH2_XY	32	r/o	-	Compatibility mode: Touch screen direct (x-MSB16; y-LSB16) conversions Extended mode: touch-screen screen data for touch 2 (x-MSB16; y-LSB16)
302190h	REG_TOUCH_DIRECT_Z1Z2 REG_CTOUCH_TOUCH3_XY	32	r/o	-	Compatibility mode: Touch screen direct (z1-MSB16; z2-LSB16) conversions Extended mode: touch-screen screen data for touch 3 (x-MSB16; y-LSB16)

Note: All register addresses are 4-byte aligned. The value in the “Bits” column refers to the number of valid bits from bit 0 unless otherwise specified; other bits are reserved.

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6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT81X device are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Table 6-1 Absolute Maximum Ratings

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40 to +85	°C
VCC Supply Voltage	0 to +4	V
VCCIO Supply Voltage	0 to +4	V
DC Input Voltage	-0.5 to + (VCCIO + 0.3)	V

* If the devices are stored out of the packaging, beyond this time limit, the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

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6.2 DC Characteristics

Table 6-2 Operating Voltage and Current
(Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCCIO1/ VCCIO2	VCCIO operating supply voltage	1.62	1.80	1.98	V	Normal Operation
		2.25	2.50	2.75	V	
		2.97	3.30	3.63	V	
VCC	VCC operating supply voltage	2.97	3.30	3.63	V	Normal Operation
Icc1	Power Down current	-		-	µA	Power down mode
Icc2	Sleep current	-		-	µA	Sleep Mode
Icc3	Standby current	-		-	mA	Standby Mode
Icc4	Operating current	-		-	mA	Normal Operation
VOUT1V2	Regulator Output voltage	-	1.20	-	V	Normal Operation

Table 6-3 Digital I/O Pin Characteristics (VCC/VCCIO = +3.3V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.4	-	-	V	
Vol	Output Voltage Low	-	-	0.4	V	
Vih	Input High Voltage	2.0	-	-	V	
Vil	Input Low Voltage	-	-	0.8	V	
Vth	Schmitt Hysteresis Voltage	0.3	0.45	0.5	V	
Iin	Input leakage current	-10	-	10	uA	Vin = VCCIO or 0
Ioz	Tri-state output leakage current	-10	-	10	uA	Vin = VCCIO or 0

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Table 6-4 Digital I/O Pin Characteristics (VCCIO = +2.5V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCCIO-0.4	-	-	V	Ioh=mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=mA
Vih	Input High Voltage	0.7 X VCCIO	-	-	V	-
Vil	Input Low Voltage	-	-	0.3 X VCCIO	V	-
Vth	Schmitt Hysteresis Voltage	0.28	0.39	0.5	V	-
Iin	Input leakage current	-10	-	10	uA	Vin = VCCIO or 0
Ioz	Tri-state output leakage current	-10	-	10	uA	Vin = VCCIO or 0

Table 6-5 Digital I/O Pin Characteristics (VCCIO = +1.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCCIO-0.4	-	-	V	Ioh=mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=mA
Vih	Input High Voltage	0.7 X VCCIO	-	-	V	-
Vil	Input Low Voltage	-	-	0.3 X VCCIO	V	-
Vth	Schmitt Hysteresis Voltage	0.25	0.35	0.5	V	-
Iin	Input leakage current	-10	-	10	uA	Vin = VCCIO or 0
Ioz	Tri-state output leakage current	-10	-	10	uA	Vin = VCCIO or 0

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6.3 AC Characteristics

6.3.1 System clock

Table 6-6 System clock characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Value			Units
	Minimum	Typical	Maximum	
Internal Relaxation Clock				
Trimmed frequency	-	12	-	MHz
Frequency tuning accuracy	-2.5	-	+2.5	%
Frequency variation over voltage and temperature	-3	-	+3	%
Crystal				
Frequency	-	12.000	-	MHz
X1/X2 Capacitance	-	5	10	pF
External clock input				
Frequency	-	12.000	-	MHz
Duty cycle	45	50	55	%
Input voltage on X1/CLKIN	-	3.3	-	Vp-p

6.3.2 Host Interface SPI Mode 0

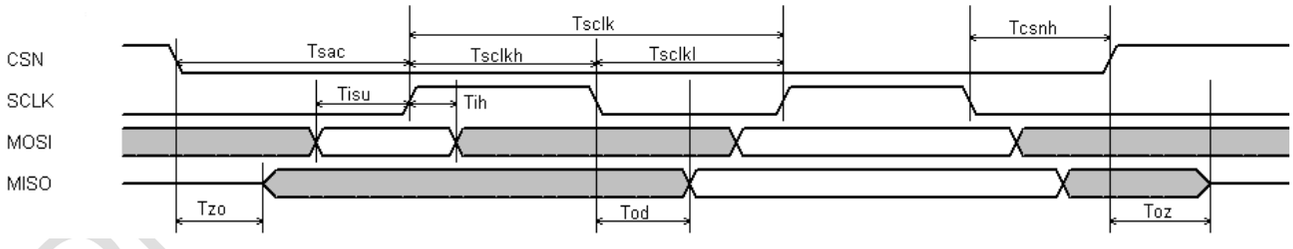


Figure 6-1 SPI Interface Timing

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Table 6-7 SPI Interface Timing Specification

Parameter	Description	VCC(I/O)=1.8V		VCC(I/O)=2.5V		VCC(I/O)=3.3V		Units
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
Tsclk	SPI clock period							ns
Tsclkl	SPI clock low duration							ns
Tsclkh	SPI clock high duration							ns
Tsac	SPI access time							ns
Tisu	Input Setup							ns
Tih	Input Hold							ns
Tzo	Output enable delay							ns
Toz	Output disable delay							ns
Tod	Output data delay							ns
Tcsnh	CSN hold time							ns

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6.3.3 RGB Video Timing

Table 6-8 RGB Video timing characteristics

Parameter	Description	VCC=3.3V			Units
		Min	**Typ**	**Max**	
Tpclk	Pixel Clock period				ns
Tpclkdc	Pixel Clock duty cycle				%
Thc	Hsync to Clock				ns
Thwh	HSYNC width (REG_HSYNC1-REG_HSYNC0)				Tpclk
Tvwh	VSYNC width (REG_VSYNC1-REG_VSYNC0)				Th
Th	HSYNC Cycle (REG_HCYCLE)				Tpclk
Tvsu	VSYNC setup				ns
Tvhd	VSYNC hold				ns
Thsu	HSYNC setup				ns
Thhd	HSYNC hold				ns
Tdsu	DATA setup				ns
Tdhd	DATA hold				ns
Tesu	DE setup				ns
Tehd	DE hold				ns

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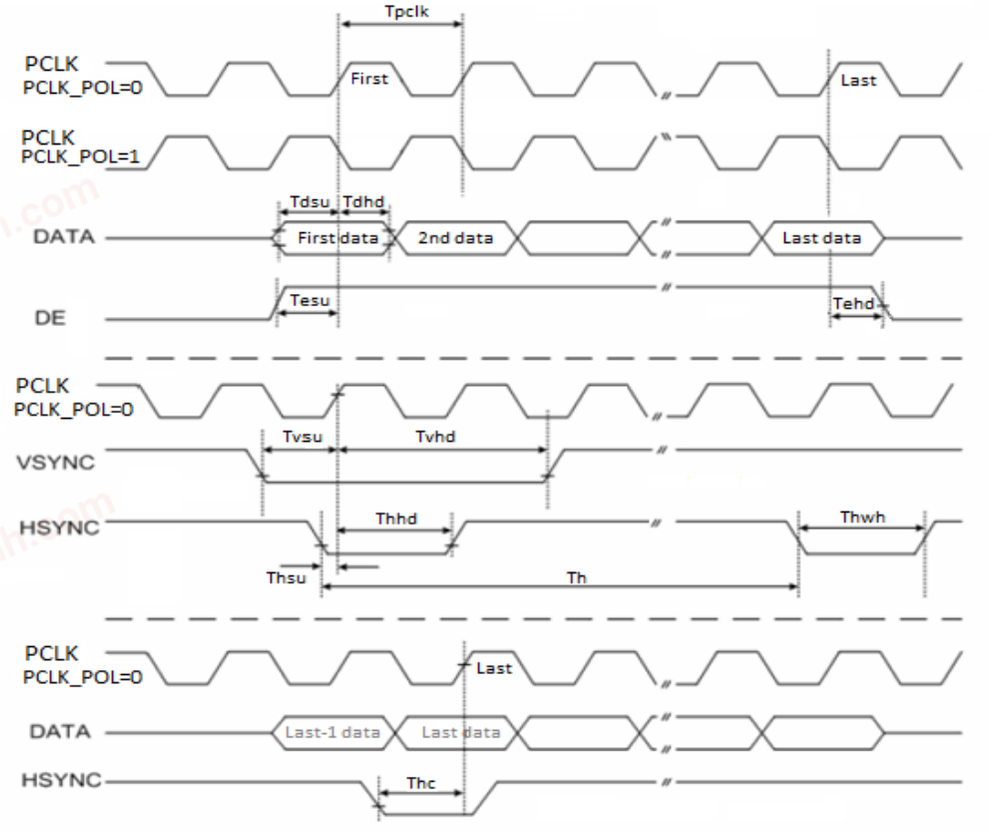


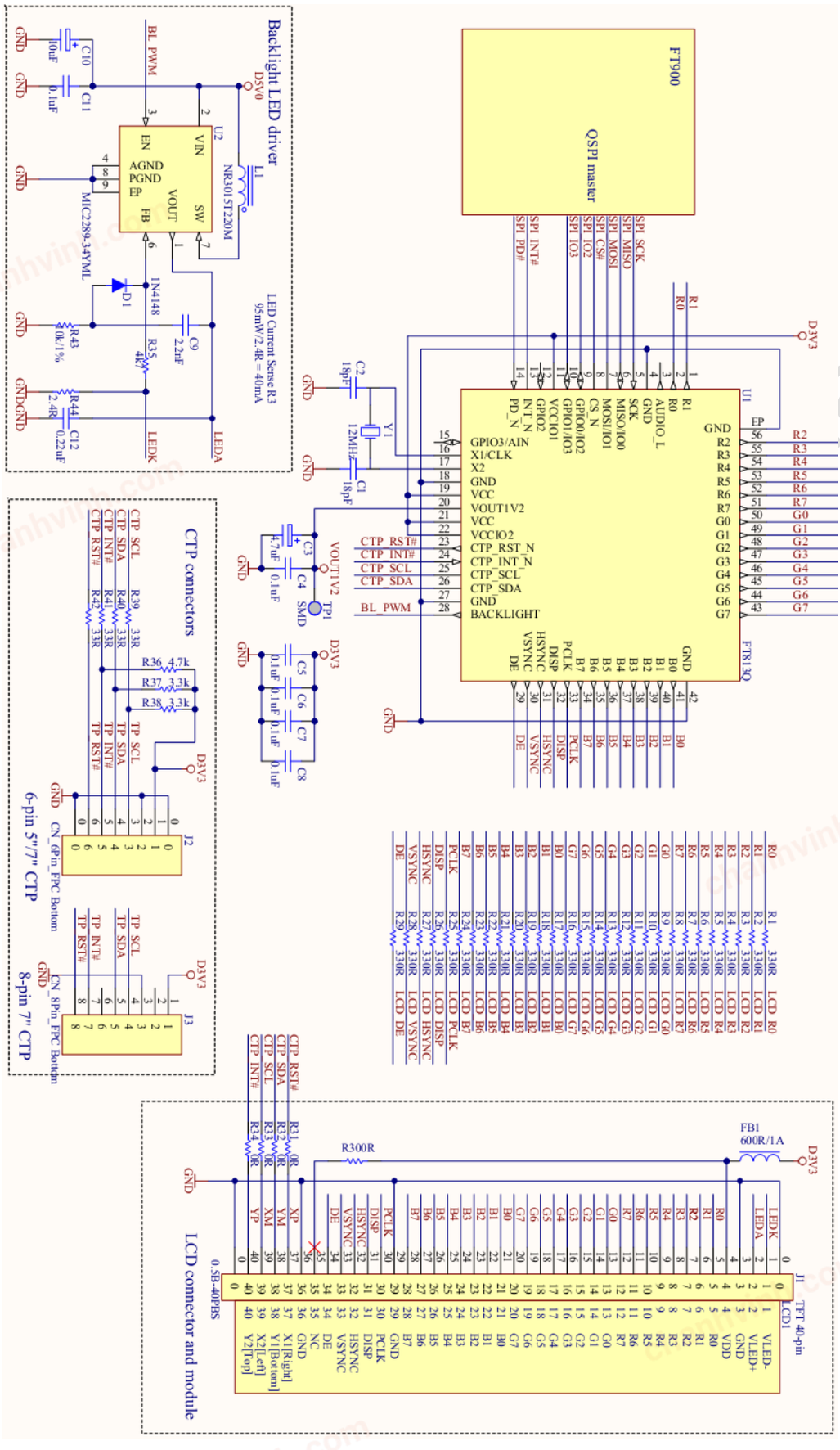
Figure 6-2 RGB Video Signal Timing

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7 Application Examples



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8 Package Parameters

The FT81X is available in VQFN-48 and VQFN-56 packages. The solder reflow profile for all packages is described in following sections.

8.1 VQFN-48 Package Dimensions

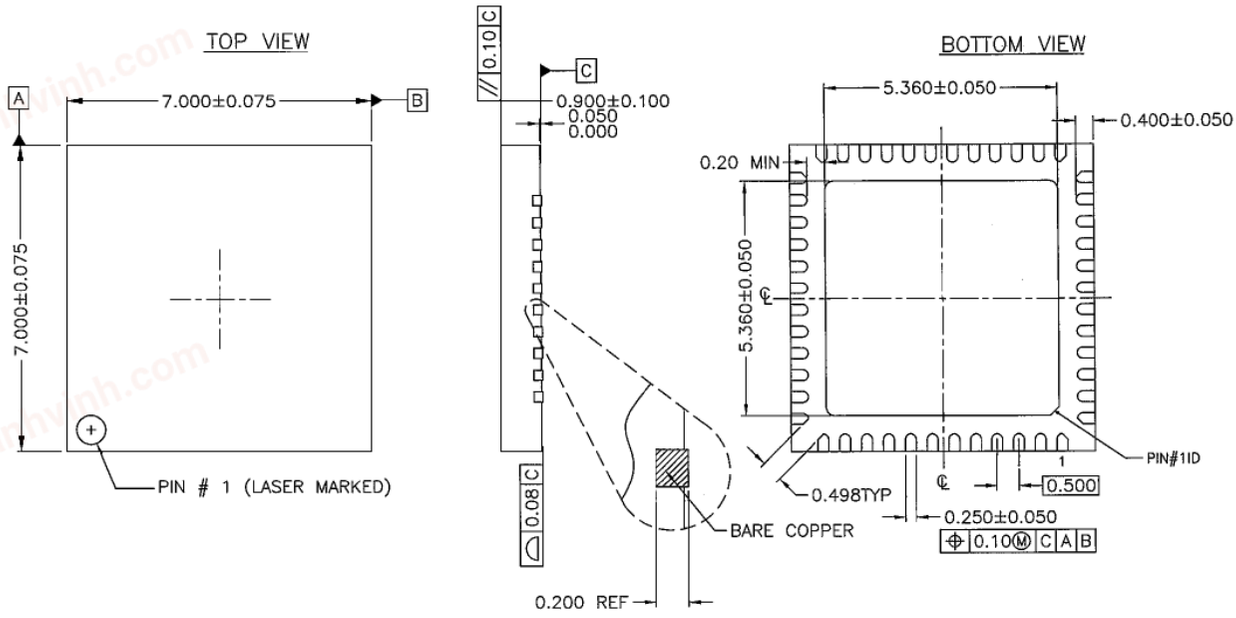


Figure 8-1 VQFN-48 Package Dimensions

8.2 VQFN-56 Package Dimensions

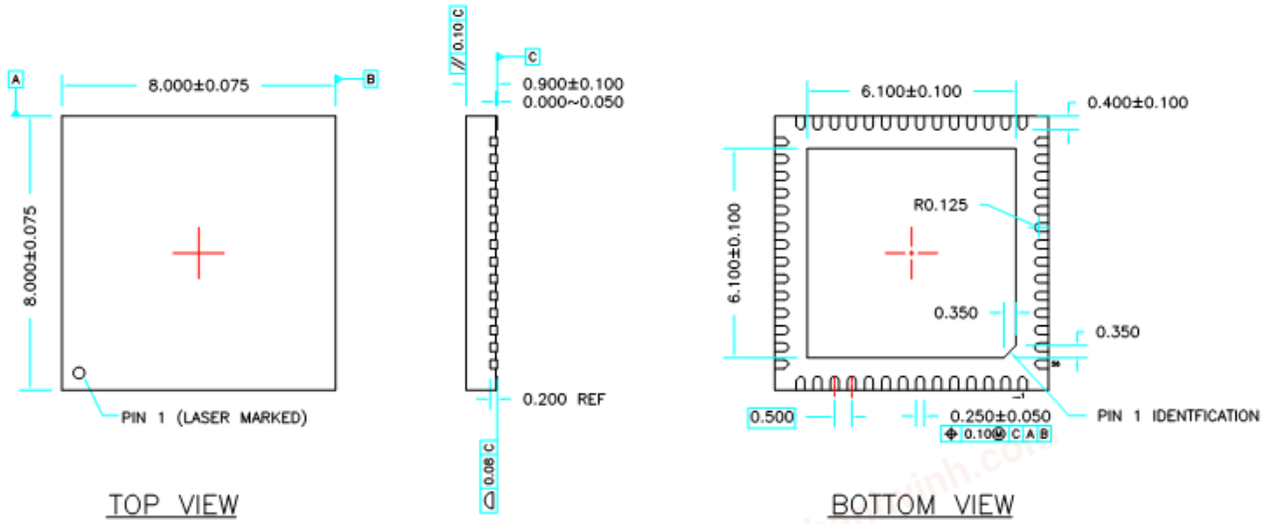


Figure 8-2 VQFN-56 Package Dimensions

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8.3 Solder Reflow Profile

The FT81X is supplied in a Pb free VQFN-48 or VQFN-56 package. The recommended solder reflow profile for the package is shown in Figure 8-3.

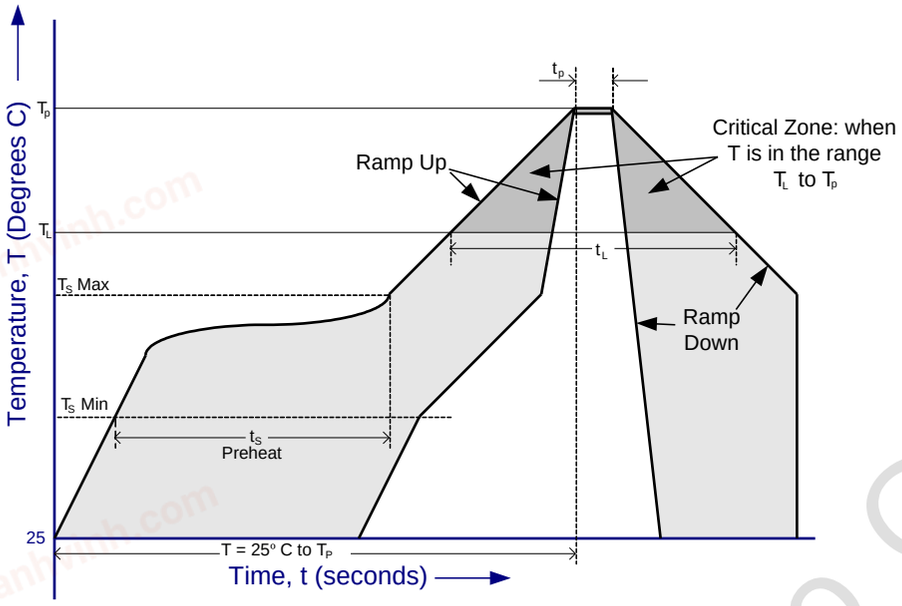


Figure 8-3 FT81X Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 8-1. Values are shown for both a completely Pb free solder process (i.e. the FT81X is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT81X is used with non-Pb free solder).

Table 8-1 Reflow Profile Parameter Values

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

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Appendix A – References

Useful Application Notes

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Appendix C - Revision History

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