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## BT817/8 Advanced Embedded Video Engine Datasheet




The BT817/8 are easy to use graphic controllers targeted at embedded applications to generate high-quality Human Machine Interfaces (HMIs). They have the following features:

- Advanced Embedded Video Engine (EVE) with high resolution graphics and video playback
- Graphic control, audio control, and touch control interface
- Supports multiple widgets for simplified design implementation
- Built-in graphics operations allow users with little expertise to create high-quality displays
- Supports Adaptive Scalable Texture Compression (ASTC) format to save considerable memory space for larger fonts and graphics images
- Supports external QSPI NOR flash up to 2Gbit to store and fetch graphic elements (image, font, widget etc.)
- Supports 4-wire resistive touch screen (BT818)
- Supports capacitive touch screen with up to 5 touch point detection (BT817)
- Hardware engine can recognize touch tags and track touch movement. Provides notification for up to 255 touch tags
- Enhanced sketch processing
- Built-in 12MHz crystal oscillator with PLL providing programmable system clock up to 72MHz
- Video RGB parallel output; configurable to support PCLK up to 96MHz with separate PLL(PLL2), and R/G/B output of 1 to 8 bits (including RGB565, RGB666 and RGB888)
- Programmable timing to adjust HSYNC and VSYNC timing, enabling interfacing to numerous displays
- Support for LCD displays with up to 1 Mega pixel in total, and up to 2048 pixels per line
- Supported LCD resolutions: 1920x480, 1440x540, 1280x800, 1024x600, 800x600, 800x480, 480x272, 320x240 and many others
- Supports landscape and portrait orientations
- High-quality cubic filter to output pixels to correct for panels with non-square pixels
- Adaptive framerate and Adaptive HSYNC modes
- Integrated 1MByte graphics RAM, no frame buffer RAM required
- Supports playback of motion-JPEG encoded AVI videos
- Mono audio channel output with Sigma-delta
- Built-in sound synthesizer
- PWM output for display backlight dimming control
- Advanced object oriented architecture enables low cost MPU/MCU as system host using SPI interfaces
- Supports SPI data lines in single, dual, or quad mode; SPI clock up to 30MHz
- Power mode control allows the chip to be put in power down, sleep, and standby states
- Supports I/O voltage from 1.8V to 3.3V (5V tolerant)
- Internal voltage regulator supplies 1.2V to the digital core
- Built-in Power-on-reset circuit
- -40°C to 85°C extended operating temperature range
- Available in a compact Pb-free, VQFN-64 package, RoHS compliant

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# 1 Typical Applications

- Point of Sales Machines
- Multi-function Printers
- Instrumentation
- Home Security Systems
- Graphic touch pad – remote, dial pad
- Tele / Video Conference Systems
- Phones and Switchboards
- Medical Appliances
- Blood Pressure displays
- Heart monitors
- Glucose level displays
- Breathalyzers
- Gas chromatographs
- Power meter
- Home appliance devices
- Set-top box
- Thermostats
- Sprinkler system displays
- GPS / Satnav
- Vending Machine Control Panels
- Elevator Controls
- ……and many more

## 1.1 Part Numbers

| Part Number | Description | Package |
|---|---|---|
| BT817Q-x | EVE4 with ASTC and external NOR flash, capacitive touch | 64 Pin VQFN, body 9 x 9 mm, pitch 0.5mm |
| BT818Q-x | EVE4 with ASTC and external NOR flash, resistive touch | 64 Pin VQFN, body 9 x 9 mm, pitch 0.5mm |

**Table 1- BT817/8 Embedded Video Engine Part Numbers**

**Note:** Packaging codes for x is:

-R: Taped and Reel (3000 pcs per reel)

-T: Tray packing (260 pcs per tray)

For example: BT817Q-R is 3000 VQFN pieces in taped and reel packaging

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# 2 Block Diagram

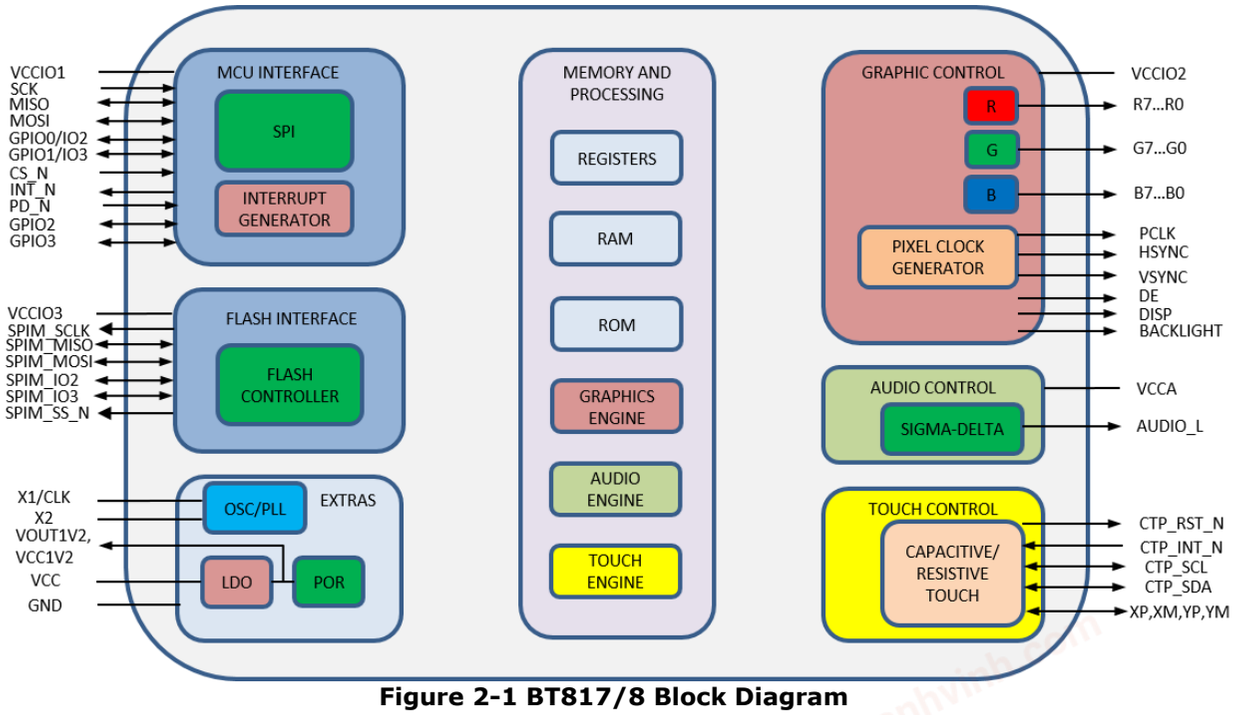



**Figure 2-1 BT817/8 Block Diagram**

For a description of each function please refer to Section 4.

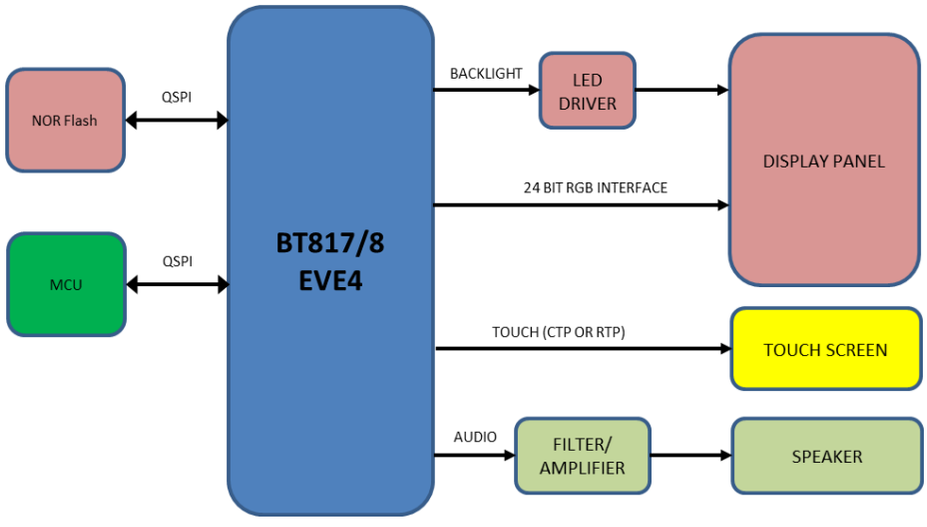



**Figure 2-2 BT817/8 System Design Diagram**

BT817/8 with EVE (Embedded Video Engine) technology simplifies the system architecture for advanced human machine interfaces (HMIs) by providing support for display, audio, and touch as well as an object oriented architecture approach that extends from display creation to the rendering of the graphics.

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# 3 Device Pin Out and Signal Description

## 3.1 BT817 VQFN-64 Package Pin Out

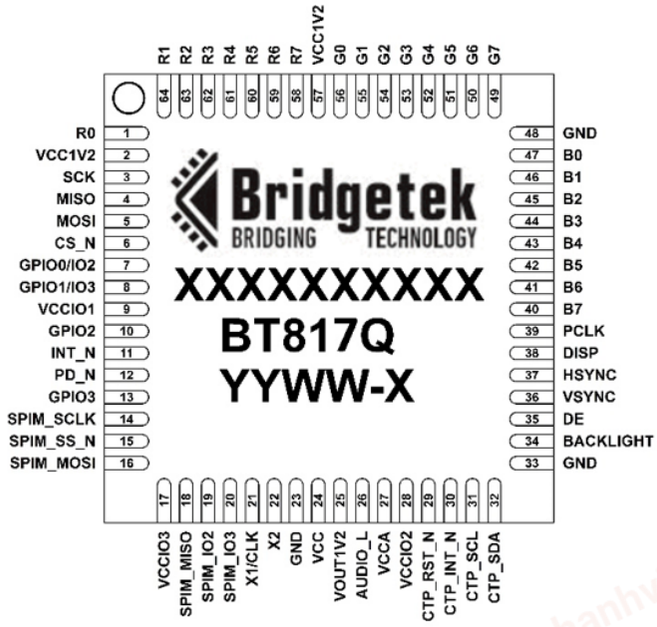



**Figure 3-1 Pin Configuration BT817 VQFN-64(Top View)**

## 3.2 BT818 VQFN-64 Package Pin Out

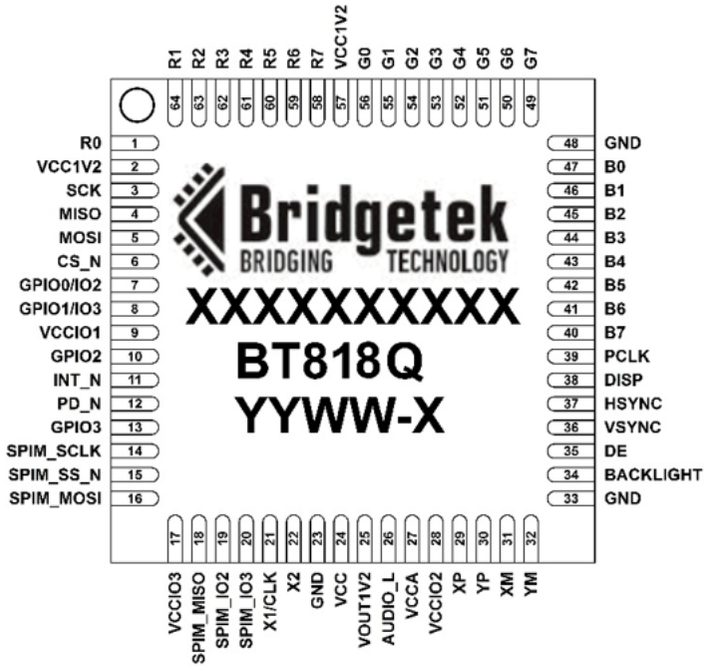



**Figure 3-2 Pin Configuration BT818 VQFN-64 (Top View)**

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## 3.3 Pin Description

| Pin Number | | Pin Name | Type | Description |
|---|---|---|---|---|
| BT817 | BT818 | | | |
| 1 | 1 | R0 | O | Bit 0 of Red RGB signals<br>Powered from pin VCCIO2 |
| 2 | 2 | VCC1V2 | P | 1.2V digital core supply. Connect to VOUT1V2 pin on PCB. A 0.1uF + 1uF decoupling capacitors are recommended |
| 3 | 3 | SCK | I | SPI clock input<br>Powered from pin VCCIO1 |
| 4 | 4 | MISO | I/O | SPI Single mode: SPI MISO output<br>SPI Dual/Quad mode: SPI data line 1<br>Powered from pin VCCIO1 |
| 5 | 5 | MOSI | I/O | SPI Single mode: SPI MOSI input<br>SPI Dual/Quad mode: SPI data line 0<br>Powered from pin VCCIO1 |
| 6 | 6 | CS_N | I | SPI slave select input<br>Powered from pin VCCIO1 |
| 7 | 7 | GPIO0/IO2 | I/O | SPI Single/Dual mode: General purpose IO 0<br>SPI Quad mode: SPI data line 2<br>Powered from pin VCCIO1 |
| 8 | 8 | GPIO1/IO3 | I/O | SPI Single/Dual mode: General purpose IO 1<br>SPI Quad mode: SPI data line 3<br>Powered from pin VCCIO1 |
| 9 | 9 | VCCIO1 | P | I/O power supply for host interface pins. Support 1.8V, 2.5V or 3.3V. |
| 10 | 10 | GPIO2 | I/O | General purpose IO 2<br>Powered from pin VCCIO1 |
| 11 | 11 | INT_N | OD/O | Interrupt to host, open drain output (default) or push-pull output, active low |
| 12 | 12 | PD_N | I | Chip power down mode control input, active low. Connect to MCU GPIO for power management or hardware reset function or pulled up to VCCIO1 if not used.<br>Powered from pin VCCIO1 |
| 13 | 13 | GPIO3 | I/O | General purpose IO 3<br>Powered from pin VCCIO1 |
| 14 | 14 | SPIM_SCLK | O | SPI flash clock output line. Leave floating if not used.<br>Powered from pin VCCIO3 |
| 15 | 15 | SPIM_SS_N | O | SPI flash chip select output line. Leave floating if not used.<br>Powered from pin VCCIO3 |
| 16 | 16 | SPIM_MOSI | I/O | SPI flash MOSI line. Leave floating if not used.<br>Powered from pin VCCIO3 |
| 17 | 17 | VCCIO3 | P | I/O power supply for SPIM pins. Support 1.8V, 2.5V or 3.3V.<br>VCCIO3 can be connected to different voltage with VCCIO1 or VCCIO2. |
| 18 | 18 | SPIM_MISO | I/O | SPI flash MISO line. Connect to GND if not used.<br>Powered from pin VCCIO3 |
| 19 | 19 | SPIM_IO2 | I/O | SPI flash IO2 line. Leave floating if not used.<br>Powered from pin VCCIO3 |
| 20 | 20 | SPIM_IO3 | I/O | SPI flash IO3 line. Leave floating if not used.<br>Powered from pin VCCIO3 |
| 21 | 21 | X1/CLK | I | Crystal oscillator input |

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| Pin Number | | Pin Name | Type | Description |
|---|---|---|---|---|
| BT817 | BT818 | | | |
| | | | | 3.3V peak input allowed.<br>Powered from pin VCC. |
| 22 | 22 | X2 | O | Crystal oscillator output<br>Powered from pin VCC. |
| 23 | 23 | GND | P | Ground |
| 24 | 24 | VCC | P | 3.3V power supply input. |
| 25 | 25 | VOUT1V2 | P | 1.2V regulator output pin. Connect a minimum 3.3uF decoupling capacitor to GND. |
| 26 | 26 | AUDIO_L | O | Audio Sigma-delta output<br>Powered from pin VCCA |
| 27 | 27 | VCCA | P | 3.3V power supply input. |
| 28 | 28 | VCCIO2 | P | I/O power supply for RGB and touch pins. Supports 1.8V, 2.5V or 3.3V. VCCIO2 can be connected to different voltage with VCCIO1 or VCCIO3. |
| - | 29 | XP | AI/O | Connect to X right electrode of 4-wire resistive touch-screen panel.<br>Powered from pin VCCIO2. |
| - | 30 | YP | AI/O | Connect to Y top electrode of 4-wire resistive touch-screen panel.<br>Powered from pin VCCIO2. |
| - | 31 | XM | AI/O | Connect to X left electrode of 4-wire resistive touch-screen panel.<br>Powered from pin VCCIO2. |
| - | 32 | YM | AI/O | Connect to Y bottom electrode of 4-wire resistive touch-screen panel.<br>Powered from pin VCCIO2. |
| 29 | - | CTP_RST_N | O | Connect to reset pin of the CTPM.<br>Powered from pin VCCIO2. |
| 30 | - | CTP_INT_N | I/O | Connect to interrupt pin of the CTPM.<br>Powered from pin VCCIO2. |
| 31 | - | CTP_SCL | I/OD | Connect to I2C SCL pin of the CTPM.<br>Powered from pin VCCIO2. |
| 32 | - | CTP_SDA | I/OD | Connect to I2C SDA pin of the CTPM.<br>Powered from pin VCCIO2. |
| 33 | 33 | GND | P | Ground |
| 34 | 34 | BACKLIGHT | O | LED Backlight brightness PWM control signal.<br>Powered from pin VCCIO2. |
| 35 | 35 | DE | O | LCD Data Enable.<br>Powered from pin VCCIO2. |
| 36 | 36 | VSYNC | O | LCD Vertical Sync.<br>Powered from pin VCCIO2. |
| 37 | 37 | HSYNC | O | LCD Horizontal Sync.<br>Powered from pin VCCIO2. |
| 38 | 38 | DISP | O | LCD Display Enable.<br>Powered from pin VCCIO2. |
| 39 | 39 | PCLK | O | LCD Pixel Clock.<br>Powered from pin VCCIO2. |
| 40 | 40 | B7 | O | Bit 7 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 41 | 41 | B6 | O | Bit 6 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 42 | 42 | B5 | O | Bit 5 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 43 | 43 | B4 | O | Bit 4 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 44 | 44 | B3 | O | Bit 3 of Blue RGB signals. |

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| Pin Number | | Pin Name | Type | Description |
|---|---|---|---|---|
| BT817 | BT818 | | | |
| | | | | Powered from pin VCCIO2. |
| 45 | 45 | B2 | O | Bit 2 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 46 | 46 | B1 | O | Bit 1 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 47 | 47 | B0 | O | Bit 0 of Blue RGB signals.<br>Powered from pin VCCIO2. |
| 48 | 48 | GND | P | Ground |
| 49 | 49 | G7 | O | Bit 7 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 50 | 50 | G6 | O | Bit 6 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 51 | 51 | G5 | O | Bit 5 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 52 | 52 | G4 | O | Bit 4 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 53 | 53 | G3 | O | Bit 3 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 54 | 54 | G2 | O | Bit 2 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 55 | 55 | G1 | O | Bit 1 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 56 | 56 | G0 | O | Bit 0 of Green RGB signals.<br>Powered from pin VCCIO2. |
| 57 | 57 | VCC1V2 | P | 1.2V digital core supply. Connect to VOUT1V2 pin on PCB. A 0.1uF decoupling capacitor is recommended. |
| 58 | 58 | R7 | O | Bit 7 of Red RGB signals.<br>Powered from pin VCCIO2. |
| 59 | 59 | R6 | O | Bit 6 of Red RGB signals.<br>Powered from pin VCCIO2. |
| 60 | 60 | R5 | O | Bit 5 of Red RGB signals.<br>Powered from pin VCCIO2. |
| 61 | 61 | R4 | O | Bit 4 of Red RGB signals.<br>Powered from pin VCCIO2. |
| 62 | 62 | R3 | O | Bit 3 of Red RGB signals.<br>Powered from pin VCCIO2. |
| 63 | 63 | R2 | O | Bit 2 of Red RGB signals.<br>Powered from pin VCCIO2. |
| 64 | 64 | R1 | O | Bit 1 of Red RGB signals<br>Powered from pin VCCIO2 |
| EP | EP | GND | P | Ground. Exposed thermal pad.<br>Connect to ground plane on PCB. |

**Table 3-1 BT817/8 Pin Description**

**Note:**

P : Power or ground
I : Input
O : Output
OD : Open drain output
I/O : Bi-direction Input and Output
AI/O: Analog Input and Output

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# 4 Functional Description

The BT817/8 is a single chip, embedded video controller with the following functional blocks:

- Quad SPI Host Interface
- Quad SPI Flash Interface
- System Clock
- Graphics Engine
- Parallel RGB video interface
- Audio Engine
- Touch-screen support and interface (Capacitive – BT817 / Resistive – BT818)
- Power Management

The functions for each block are briefly described in the following subsections.

## 4.1 Quad SPI Host Interface

The BT817/8 uses a quad serial peripheral interface (QSPI) to communicate with host microcontrollers and microprocessors.

### 4.1.1 QSPI Interface

The QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported. Refer to section 6.4.2 for detailed timing specification. The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default, the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH. The table below depicts the setting.

| REG_SPI_WIDTH [1:0] | Channel Mode | Data pins | Max bus speed |
|---|---|---|---|
| 00 | SINGLE – default mode | MISO, MOSI | 30 MHz |
| 01 | DUAL | MOSI, MISO | 30 MHz (not exceeding system clock frequency) |
| 10 | QUAD | MOSI, MISO, IO2, IO3 | 30 MHz (not exceeding half of the system clock frequency) |
| 11 | Reserved | - | - |

**Table 4-1 QSPI Channel Selection**

With DUAL/QUAD channel modes, the SPI data ports are now unidirectional. In these modes, each SPI transaction (signified by CS_N going active low) will begin with the data ports set as inputs.

Hence, for writing to the BT817/8, the protocol will operate as in previous EVE revisions such as the FT800, with "WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ …" The write operation is considered complete when CS_N goes inactive high.

For reading from the BT817/8, the protocol will still operate as in FT800, with "RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ". However, as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the BT817/8. Therefore, it is important that the firmware controlling the SPI master changes the SPI master data port direction to "input" after transmitting Addr0. The BT817/8 will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the BT817/8 will reset all its data ports' direction to input once CS_N goes inactive high (i.e. at the end of the current SPI master transaction).

Figure 4-1 depicts the behaviour of both the SPI master and slave in the master read case.

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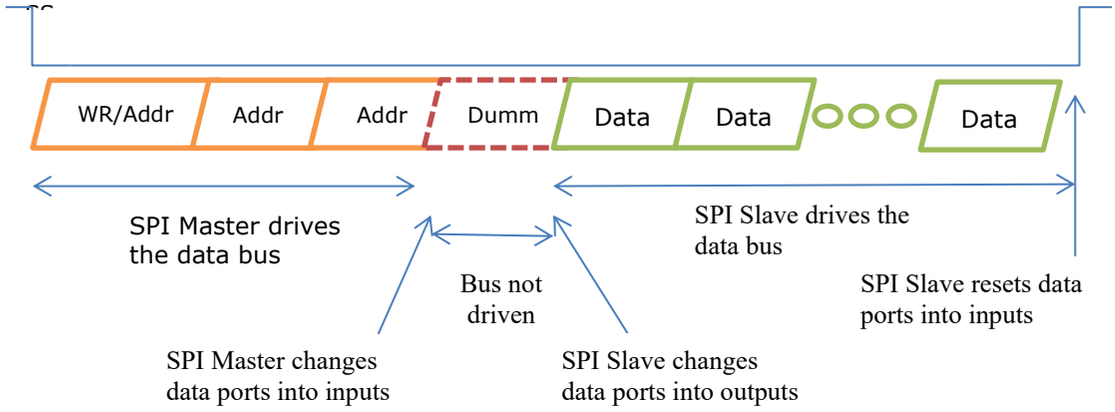



**Figure 4-1 SPI Master and Slave in the Master Read Case**

In the DUAL channel mode, MISO (MSB) and MOSI are used while in the QUAD channel mode. IO3 (MSB), IO2, MISO and MOSI are used.

Figure 4-2 illustrates a direct connection to a 1.8-3.3V IO MPU/MCU with single or dual SPI interface.

Figure 4-3 illustrates a direct connection to a 1.8-3.3V IO MPU/MCU with Quad SPI interface.

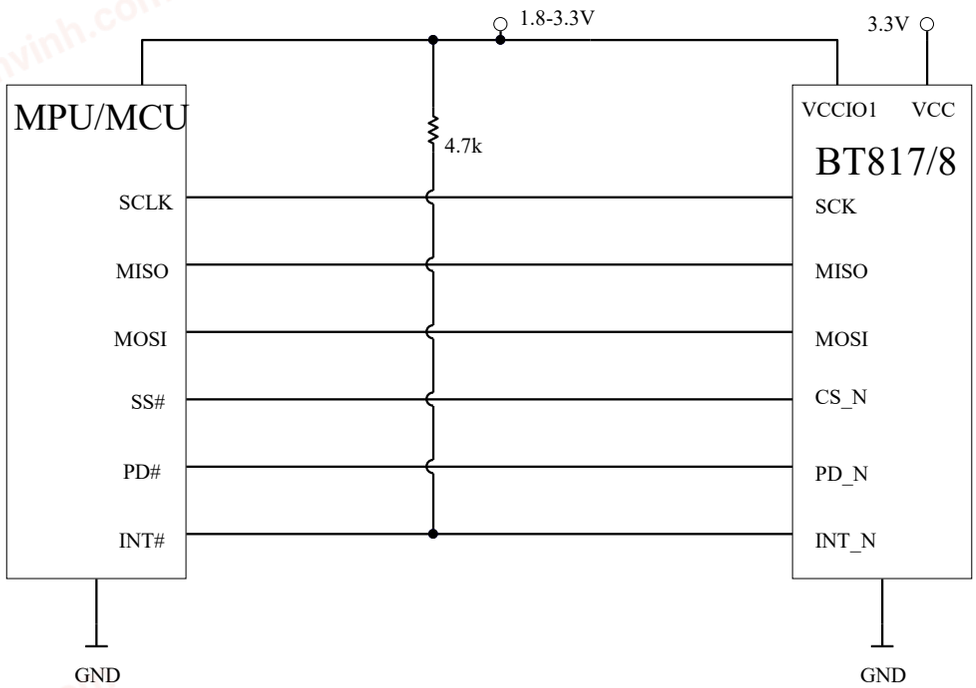



**Figure 4-2 Single/Dual SPI Interface connection**

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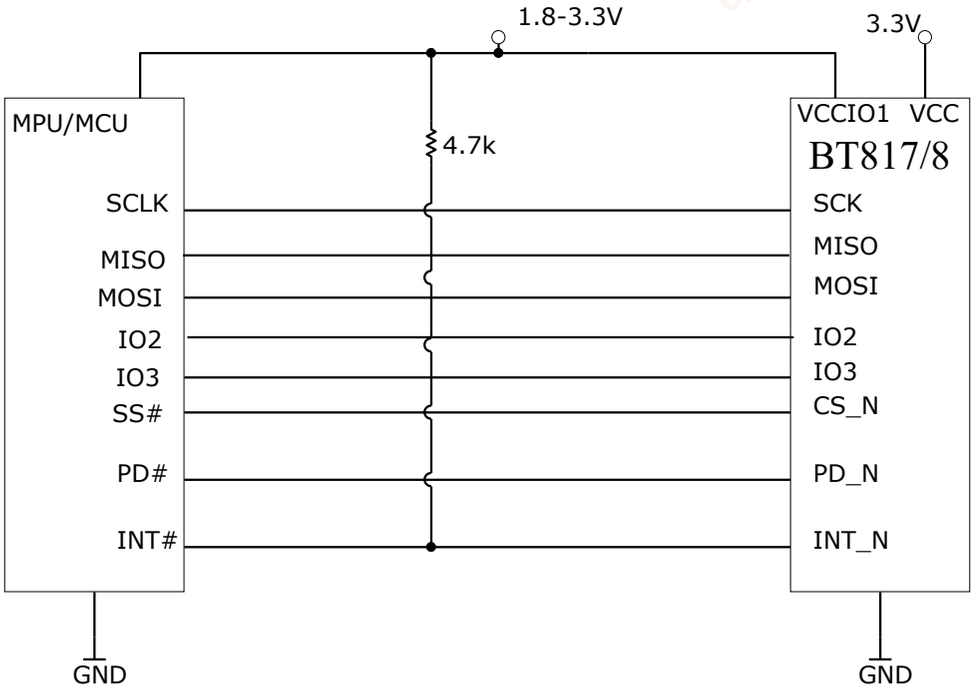



**Figure 4-3 Quad SPI Interface connection**

### 4.1.2 Serial Data Protocol

The BT817/8 appears to the host MPU/MCU as a memory-mapped SPI device. The host communicates with the BT817/8 using reads and writes to a large (4 megabyte) address space. Within this address space are dedicated areas for graphics, audio, and touch control. Refer to section 5 for the detailed memory map. The host reads and writes the BT817/8 address space using SPI transactions. These transactions are memory read, memory write and command write. Serial data is sent by the most significant bit first. Each transaction starts with CS_N goes low and ends when CS_N goes high. There is no limit on data length within one transaction, as long as the memory address is continuous.

### 4.1.3 Host Memory Read

For SPI memory read transactions, the host sends two zero bits, followed by the 22-bit address. This is followed by a dummy byte. After the dummy byte, the BT817/8 responds to each host byte with read data bytes.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | Address [21:16] | | | | | | Write Address |
| Address [15:8] | | | | | | | | |
| Address [7:0] | | | | | | | | |
| Dummy byte | | | | | | | | Read Data |
| Byte 0 | | | | | | | | |
| Byte *n* | | | | | | | | |

**Table 4-2 Host Memory Read Transaction**

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### 4.1.4 Host Memory Write

For SPI memory write transactions, the host sends a '1' bit and '0' bit, followed by the 22-bit address. This is followed by the write data.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | Address [21:16] | | | | | | Write Address |
| Address [15:8] | | | | | | | | |
| Address [7:0] | | | | | | | | |
| Byte 0 | | | | | | | | Write Data |
| Byte *n* | | | | | | | | |

**Table 4-3 Host Memory Write Transaction**

### 4.1.5 Host Command

When sending a command, the host transmits a 3 byte command. Table 4-5 lists all the host command functions.

For SPI command transactions, the host sends a '0' bit and '1' bit, followed by the 6-bit command code. The 2nd byte can be either 00h, or the parameter of that command. The 3rd byte is fixed at 00h.

All SPI commands except the system reset can only be executed when the SPI is in the Single channel mode. They will be ignored when the SPI is in either Dual or Quad channel mode.

Some commands are used to configure the device and these configurations will be reset upon receiving the SPI PWRDOWN command, except those that configure the pin state during power down. These commands will be sticky unless reconfigured or power-on-reset (POR) occurs.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | Command [5:0] | | | | | | 1st Byte |
| Parameter for the command | | | | | | | | 2nd Byte |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3rd Byte |

**Table 4-4 Host Command Transaction**

| 1st Byte | 2nd byte | 3rd byte | Command | Description |
|---|---|---|---|---|
| **Power Modes** | | | | |
| 00000000b | 00000000b | 00000000b | 00h<br>ACTIVE | Switch from Standby/Sleep/PWRDOWN modes to active mode. Dummy memory read from address 0(read twice) generates ACTIVE command. |
| 01000001b | 00000000b | 00000000b | 41h<br>STANDBY | Put BT817/8 core to standby mode. Clock gate off, PLL and Oscillator remain on. ACTIVE command to wake up. |
| 01000010b | 00000000b | 00000000b | 42h<br>SLEEP | Put BT817/8 core to sleep mode. Clock gate off, PLL and Oscillator off. ACTIVE command to wake up. |

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| 1st Byte | 2nd byte | 3rd byte | Command | Description |
|---|---|---|---|---|
| 01000011b<br>01010000b | 00000000b | 00000000b | 43h/50h<br>PWRDOWN | Switch off 1.2V core voltage to the digital core circuits. Clock, PLL and Oscillator off. SPI is alive. ACTIVE command to wake up. |
| **Clock and Reset** | | | | |
| 01000100b | 00000000b | 00000000b | 44h<br>CLKEXT | Select PLL input from external crystal oscillator. No effect if external clock is already selected, otherwise a system reset will be generated |
| 01100001b<br>01100010b | xx | 00000000b | 61h/62h<br>CLKSEL | Select the system clock frequency. Note that software shall also update the register value for REG_FREQUENCY to align with system clock selected.<br>This command will only be effective when the PLL is stopped (SLEEP mode).<br>For compatibility to FT800/FT801, set Byte2 to 0x00. This will set the PLL clock back to default (60 MHz).<br>Byte2 [5:0] — sets the clock frequency<br>0 — Set to default clock speed<br>1 — Reserved<br>2 to 6 — 2 to 6 times the osc frequency (i.e. 24 to 72MHz with 12MHz oscillator)<br>Byte2 [7:6] — sets the PLL range<br>0 — When Byte2[5:0] = 0, 2, 3<br>1 — When Byte2[5:0] = 4, 5, 6 |
| 01101000b | 00000000b | 00000000b | 68h<br>RST_PULSE | Send reset pulse to BT817/8 core. The behaviour is the same as POR except that settings done through SPI commands will not be affected |
| **Configuration** | | | | |
| 01110000b | xx | 00000000b | 70h<br>PINDRIVE | This will set the drive strength for various pins. For FT800/FT801 compatibility, by default those settings are from the GPIO registers. BT817/8 supports setting the drive strength via SPI command instead.<br>When PINDRIVE for a pin from the SPI command is not updated, the drive strength will be determined by its corresponding GPIO register bits if they exist. If they do not exist, a hard coded setting is used. Please refer to Table 4-23 for default values.<br>When PINDRIVE for a pin from the SPI command is updated, it will override the corresponding setting in the GPIO register bits.<br>Byte2 determines which pin and the |

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<table>
<tr><th>1st Byte</th><th>2nd byte</th><th>3rd byte</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>setting are to be updated.<br>Byte2[1:0] determine the drive strength. Refer to Table 6-4 for pin group and drive strength currents.<br><br>
<table>
<tr><td>Byte2[1:0]</td><td colspan="2">Drive Strength Degree</td></tr>
<tr><td>0h</td><td>DSD1</td><td>Low</td></tr>
<tr><td>1h</td><td>DSD2</td><td>Medium</td></tr>
<tr><td>2h</td><td>DSD3</td><td>High</td></tr>
<tr><td>3h</td><td>DSD4</td><td>Maximum</td></tr>
</table>
<br>Byte2[7:2] determine which pin/pin group to set:
<table>
<tr><td>Byte2 [7:2]</td><td>Pin / Pin Group</td></tr>
<tr><td>00h</td><td>GPIO 0</td></tr>
<tr><td>01h</td><td>GPIO 1</td></tr>
<tr><td>02h</td><td>GPIO 2</td></tr>
<tr><td>03h</td><td>GPIO 3</td></tr>
<tr><td>04-07h</td><td>Reserved</td></tr>
<tr><td>08h</td><td>DISP</td></tr>
<tr><td>09h</td><td>DE</td></tr>
<tr><td>0Ah</td><td>VSYNC / HSYNC</td></tr>
<tr><td>0Bh</td><td>PCLK</td></tr>
<tr><td>0Ch</td><td>BACKLIGHT</td></tr>
<tr><td>0Dh</td><td>R[7:0], G[7:0], B[7:0]</td></tr>
<tr><td>0Eh</td><td>AUDIO_L</td></tr>
<tr><td>0Fh</td><td>INT_N</td></tr>
<tr><td>10h</td><td>CTP_RST_N</td></tr>
<tr><td>11h</td><td>CTP_SCL</td></tr>
<tr><td>12h</td><td>CTP_SDA</td></tr>
<tr><td>13h</td><td>SPI MISO/MOSI/IO2/IO3</td></tr>
<tr><td>14h</td><td>SPIM_SCLK</td></tr>
<tr><td>15h</td><td>SPIM_SS_N</td></tr>
<tr><td>16h</td><td>SPIM_MISO</td></tr>
<tr><td>17h</td><td>SPIM_MOSI</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>1st Byte</th><th>2nd byte</th><th>3rd byte</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>
<table>
<tr><td>18h</td><td>SPIM_IO2</td></tr>
<tr><td>19h</td><td>SPIM_IO3</td></tr>
<tr><td>Others</td><td>Reserved</td></tr>
</table>
Note: GPIO0 shares the same pin as SPI IO2 and GPIO1 with SPI IO3. When SPI is set in Quad mode, IO2 and IO3 will inherit the drive strength set in GROUP 13h; otherwise GPIO0 and GPIO1 will inherit the drive strength from GROUP 00h and 01h respectively.
</td></tr>
<tr><td>01110001b</td><td>xx</td><td>00000000b</td><td>71h<br>PIN_PD_STATE</td><td>
During power down, I/O pins will have different state as compared to normal operating mode. Please refer to Table 4-23 for their default power down state.<br>
These settings will only be effective during power down and will not affect normal operations. Also note that these configuration bits are sticky and, unlike other configuration bits, will not reset to default values upon exiting power down. Only POR will reset them.<br>
Byte2 determines which pin and the setting are to be updated.<br>
Byte2[1:0] determine the pin state.
<table>
<tr><td>Byte2 [1:0]</td><td>Pin Setting</td></tr>
<tr><td>0h</td><td>Float</td></tr>
<tr><td>1h</td><td>Pull-Down</td></tr>
<tr><td>2h</td><td>Pull-Up</td></tr>
<tr><td>3h</td><td>Reserved</td></tr>
</table>
Byte2[7:2] determine which pin/pin group to set.<br>
Please refer to the table in command PINDRIVE entry.
</td></tr>
</table>

**Table 4-5 Host Command List**

**Note:** Any command code not specified is reserved and should not be used by the software

### 4.1.6 Interrupts

The interrupt output pin is enabled by REG_INT_EN. When REG_INT_EN is 0, INT_N is tri-state (pulled to high by external pull-up resistor). When REG_INT_EN is 1, INT_N is driven low when any of the interrupt flags in REG_INT_FLAGS are high, after masking with REG_INT_MASK. Writing a '1' in any bit of REG_INT_MASK will enable the corresponding interrupt. Each bit in REG_INT_FLAGS is set by a corresponding interrupt source. REG_INT_FLAGS is readable by the host at any time and clears when read.

The INT_N pin is open-drain (OD) output by default. It can be configured to push-pull output by register REG_GPIOX.

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| Bit | Interrupt Source | Conditions |
|---|---|---|
| 0 | INT_SWAP | Display list swap occurred |
| 1 | INT_TOUCH | touch detected |
| 2 | INT_TAG | Touch-screen tag value change |
| 3 | INT_SOUND | Sound effect ended |
| 4 | INT_PLAYBACK | Audio playback ended |
| 5 | INT_CMDEMPTY | Command FIFO empty |
| 6 | INT_CMDFLAG | Command FIFO flag |
| 7 | INT_CONV_COMPLETE | Touch-screen conversions completed |
| 8 | INT_UNDERRUN | Graphics pipeline underrun |

**Table 4-6 Interrupt Flags bit assignment**

## 4.2 System Clock

### 4.2.1 Clock Source

The BT817/8 supports external 12MHz crystal as clock source for system clock and RGB interface pixel clock.

Figure 4-4 shows the pin connections for the crystal.

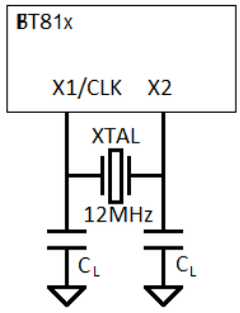



**Figure 4-4 Crystal Oscillator Connection**

### 4.2.2 Phase Locked Loop

There are 2 PLLs inside the chip, system PLL(PLL1) and PCLK PLL(PLL2).

The system PLL takes an input clock from the oscillator, and generates clocks to all internal circuits, including the graphics engine, audio engine and touch engine.

The PCLK PLL (PLL2) takes an input clock from the oscillator and generates clocks for RGB interface when configured in Exsync mode.

### 4.2.3 Clock Enable

At power-on the BT817/8 is in sleep mode. The system clock will be enabled when the following step is executed:

- Host sends a “CLKEXT” command
- Host sends an “ACTIVE” command

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### 4.2.4 Clock Frequency

By default, the system clock is running at 60MHz when the input clock is 12MHz. The host is allowed to switch the system clock to other frequencies by the host command "CLKSEL." The clock switching command shall be sent in SLEEP mode only.

After the chip is put into Active mode, software shall update the REG_FREQUENCY value to align with the chosen system clock frequency by CLKSEL command, if the default 60MHz is changed.

## 4.3 Graphics Engine

### 4.3.1 Introduction

The graphics engine executes the display list once for every horizontal line. It executes the primitive objects in the display list and constructs the display line buffer. The horizontal pixel content in the line buffer is updated if the object is visible at the horizontal line.

Key features of the graphics engine are:

- The primitive objects supported by the graphics processor are: lines, points, rectangles, bitmaps (comprehensive set of formats), text display, plotting bar graph, edge strips, and line strips, etc.
- Operations such as stencil test, alpha blending and masking are useful for creating a rich set of effects such as shadows, transitions, reveals, fades, and wipes.
- Anti-aliasing of the primitive objects (except bitmaps) gives a smoothing effect to the viewer.
- Bitmap transformations enable operations such as translate, scale, and rotate.
- Display pixels are plotted with 1/16$^{th}$ pixel precision.
- Four levels of graphics states
- Tag buffer detection

The graphics engine also supports customized built-in widgets and functionalities such as ASTC decode, jpeg decode, screen saver, calibration etc. The graphics engine interprets commands from the MPU host via a 4 Kbyte FIFO in the BT817/8 memory at RAM_CMD. The MPU/MCU writes commands into the FIFO, and the graphics engine reads and executes the commands. The MPU/MCU updates the register REG_CMD_WRITE to indicate that there are new commands in the FIFO, and the graphics engine updates REG_CMD_READ after commands have been executed.

Key features supported are:

- Drawing of widgets such as buttons, clock, keys, gauges, text displays, progress bars, sliders, toggle switches, dials, gradients, etc.
- JPEG and motion-JPEG decode
- Inflate functionality (zlib inflate is supported)
- Timed interrupt (generate an interrupt to the host processor after a specified number of milliseconds)
- In-built animated functionalities such as displaying logo, calibration, spinner, screen saver and sketch
- Snapshot feature to capture the current graphics display

For a complete list of graphics engine display commands and widgets refer to BT81X Series Programming Guide, Chapter 4.

### 4.3.2 ASTC

ASTC stands for **A**daptive **S**calable **T**exture **C**ompression, an open standard developed by ARM for use in mobile GPUs.

ASTC is a block-based lossy compression format. The compressed image is divided into a number of blocks of uniform size, which makes it possible to quickly determine which block a given texel (unit of a texture map) resides in. Each block has a fixed memory footprint of 128 bits, but these bits can represent varying numbers of texels (the block footprint).

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Block footprint sizes are not confined to powers-of-two and are also not confined to be square. For 2D formats the block dimensions range from 4 to 12 texels.

Using ASTC for the large ROM fonts can save considerable space. Encoding the four largest fonts in ASTC 8x8 formats gives no noticeable loss in quality and reduces the ROM size from 1 Mbytes to about 640 Kbytes.

### 4.3.3 ROM and RAM Fonts

The BT817/8 has built in ROM character bitmaps as font metrics. The graphics engine can use these metrics when drawing text fonts. There are a total of 19 ROM fonts, numbered with font handle 16-34. Fonts 31-34 are large ROM fonts encoded in ASTC 8x8 format. The user can define and load customized font metrics into RAM_G or external flash, making it possible to support a full range of Unicode characters with UTF-8 coding points.

Each ROM font metric block has a 148 byte font table which defines the parameters of the font and the pointer of font image. The font table format is shown in Table 4-7.

| Address Offset | Size(byte) | Parameter Description |
|---|---|---|
| 0 | 128 | width of each font character, in pixels |
| 128 | 4 | font bitmap format, for example L1, L4 or L8 |
| 132 | 4 | font line stride, in bytes |
| 136 | 4 | font width, in pixels |
| 140 | 4 | font height, in pixels |
| 144 | 4 | pointer to font image data in memory |

**Table 4-7 Font Table Format**

The ROM fonts are stored in the memory space ROM_FONT. The ROM font table is also stored in the ROM. The starting address of the ROM font table for font index 16 is stored at ROM_FONT_ADDR, with other font tables following. The ROM font table and individual character width (in pixel) are listed in Table 4-8, Table 4-9 and Table 4-10. Font index 16, 18 and 20-31 are for basic ASCII characters (code 0-127), while font index 17 and 19 are for Extended ASCII characters (code 128-255). The character width for font index 16 through 19 is fixed at 8 pixels for any of the ASCII characters.

| Font Index | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Font format | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L4 | L4 | L4 | L4 | L4 | L4 | L4 | L4 | L4 |
| Line stride | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 3 | 3 | 4 | 7 | 8 | 9 | 11 | 14 | 18 | 23 | 30 | 39 |
| Font width (max) | 8 | 8 | 8 | 8 | 11 | 13 | 17 | 18 | 25 | 34 | 13 | 15 | 19 | 21 | 28 | 37 | 49 | 63 | 82 |
| Font height | 8 | 8 | 16 | 16 | 13 | 17 | 20 | 22 | 29 | 38 | 16 | 20 | 25 | 28 | 36 | 49 | 63 | 83 | 108 |

**Table 4-8 ROM Font Table**

| Font Index => | | | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ASCII Character width in pixels | 0 | NULL | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | SOH | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 2 | STX | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 3 | ETX | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 4 | EOT | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 5 | ENQ | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 6 | ACK | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 7 | BEL | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 8 | BS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 9 | HT | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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| Font Index => | | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | LF | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | VT | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | FF | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13 | CR | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | SO | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | SI | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | DLE | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 | DC1 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18 | DC2 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19 | DC3 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 | DC4 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21 | NAK | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22 | SYN | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 23 | ETB | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24 | CAN | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 25 | EM | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26 | SUB | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 27 | ESC | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28 | FS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 29 | GS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30 | RS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31 | US | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32 | Space | 8 | 3 | 4 | 5 | 5 | 6 | 9 | 3 | 4 | 5 | 6 | 8 | 10 | 13 | 18 | 23 |
| 33 | ! | 8 | 3 | 4 | 5 | 6 | 6 | 9 | 3 | 4 | 6 | 6 | 9 | 11 | 15 | 19 | 25 |
| 34 | " | 8 | 4 | 5 | 6 | 5 | 8 | 12 | 5 | 6 | 7 | 8 | 12 | 15 | 19 | 25 | 33 |
| 35 | # | 8 | 6 | 8 | 9 | 10 | 14 | 19 | 10 | 11 | 14 | 15 | 19 | 26 | 33 | 44 | 57 |
| 36 | $ | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 11 | 15 | 18 | 25 | 31 | 41 | 54 |
| 37 | % | 8 | 9 | 12 | 14 | 16 | 22 | 29 | 11 | 13 | 16 | 17 | 23 | 31 | 40 | 52 | 68 |
| 38 | & | 8 | 8 | 10 | 11 | 13 | 17 | 22 | 9 | 11 | 14 | 15 | 19 | 26 | 34 | 44 | 57 |
| 39 | ' | 8 | 2 | 3 | 3 | 3 | 6 | 6 | 3 | 4 | 4 | 5 | 7 | 10 | 11 | 15 | 20 |
| 40 | ( | 8 | 4 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 7 | 9 | 11 | 15 | 18 | 24 | 31 |
| 41 | ) | 8 | 4 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 8 | 8 | 10 | 14 | 18 | 24 | 31 |
| 42 | * | 8 | 4 | 7 | 6 | 7 | 10 | 13 | 7 | 8 | 10 | 11 | 14 | 18 | 24 | 31 | 40 |
| 43 | + | 8 | 6 | 9 | 10 | 10 | 14 | 19 | 9 | 10 | 12 | 14 | 17 | 24 | 30 | 41 | 52 |
| 44 | , | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 4 | 5 | 7 | 9 | 12 | 16 | 20 |
| 45 | - | 8 | 4 | 4 | 5 | 6 | 8 | 11 | 6 | 7 | 10 | 11 | 15 | 18 | 24 | 32 | 41 |
| 46 | . | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 6 | 7 | 8 | 11 | 14 | 19 | 24 |
| 47 | / | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 6 | 7 | 9 | 10 | 13 | 17 | 22 | 29 | 38 |
| 48 | 0 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 49 | 1 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 50 | 2 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 51 | 3 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 52 | 4 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 53 | 5 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 54 | 6 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 55 | 7 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 56 | 8 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 57 | 9 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 58 | : | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 6 | 6 | 7 | 10 | 13 | 18 | 23 |
| 59 | ; | 8 | 3 | 4 | 4 | 5 | 6 | 9 | 3 | 4 | 6 | 6 | 8 | 10 | 14 | 18 | 23 |
| 60 | < | 8 | 6 | 8 | 10 | 10 | 15 | 19 | 8 | 9 | 11 | 12 | 16 | 21 | 28 | 36 | 46 |
| 61 | = | 8 | 5 | 9 | 10 | 11 | 15 | 19 | 8 | 9 | 13 | 14 | 18 | 23 | 30 | 40 | 52 |
| 62 | > | 8 | 6 | 8 | 10 | 10 | 15 | 19 | 8 | 9 | 11 | 13 | 16 | 22 | 29 | 37 | 48 |

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| Font Index => | | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 63 | ? | 8 | 6 | 8 | 9 | 10 | 12 | 18 | 7 | 9 | 10 | 12 | 15 | 20 | 26 | 34 | 44 |
| 64 | @ | 8 | 11 | 13 | 17 | 18 | 25 | 34 | 13 | 15 | 19 | 21 | 28 | 37 | 49 | 63 | 82 |
| 65 | A | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 11 | 13 | 15 | 20 | 27 | 34 | 45 | 58 |
| 66 | B | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 10 | 14 | 15 | 19 | 27 | 34 | 45 | 58 |
| 67 | C | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 13 | 15 | 20 | 26 | 34 | 45 | 58 |
| 68 | D | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 14 | 17 | 22 | 28 | 36 | 48 | 63 |
| 69 | E | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 7 | 9 | 12 | 13 | 16 | 23 | 29 | 39 | 50 |
| 70 | F | 8 | 6 | 8 | 10 | 12 | 14 | 20 | 7 | 9 | 12 | 13 | 17 | 22 | 29 | 39 | 50 |
| 71 | G | 8 | 8 | 11 | 13 | 15 | 19 | 25 | 9 | 11 | 14 | 16 | 22 | 28 | 37 | 48 | 62 |
| 72 | H | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 15 | 17 | 23 | 29 | 37 | 50 | 65 |
| 73 | I | 8 | 3 | 4 | 4 | 6 | 8 | 9 | 4 | 5 | 6 | 7 | 9 | 12 | 15 | 20 | 26 |
| 74 | J | 8 | 5 | 7 | 8 | 10 | 13 | 16 | 8 | 9 | 12 | 13 | 17 | 23 | 30 | 40 | 50 |
| 75 | K | 8 | 7 | 9 | 11 | 13 | 18 | 22 | 9 | 11 | 14 | 16 | 19 | 26 | 34 | 45 | 58 |
| 76 | L | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 7 | 9 | 12 | 13 | 17 | 22 | 29 | 39 | 51 |
| 77 | M | 8 | 9 | 12 | 13 | 16 | 21 | 27 | 11 | 14 | 19 | 21 | 26 | 35 | 46 | 62 | 79 |
| 78 | N | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 15 | 17 | 23 | 29 | 37 | 50 | 65 |
| 79 | O | 8 | 8 | 11 | 13 | 15 | 18 | 25 | 10 | 12 | 14 | 16 | 22 | 28 | 37 | 49 | 63 |
| 80 | P | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 9 | 10 | 14 | 15 | 19 | 26 | 34 | 45 | 58 |
| 81 | Q | 8 | 8 | 11 | 13 | 15 | 18 | 26 | 10 | 12 | 14 | 17 | 22 | 29 | 38 | 50 | 64 |
| 82 | R | 8 | 7 | 10 | 12 | 14 | 17 | 24 | 9 | 11 | 13 | 15 | 19 | 27 | 33 | 45 | 58 |
| 83 | S | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 9 | 11 | 12 | 14 | 20 | 26 | 33 | 43 | 56 |
| 84 | T | 8 | 5 | 9 | 10 | 12 | 16 | 20 | 10 | 12 | 14 | 15 | 19 | 26 | 32 | 42 | 56 |
| 85 | U | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 13 | 17 | 21 | 28 | 37 | 48 | 62 |
| 86 | V | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 11 | 14 | 15 | 20 | 27 | 34 | 45 | 58 |
| 87 | W | 8 | 9 | 13 | 15 | 18 | 22 | 31 | 12 | 15 | 18 | 21 | 27 | 36 | 46 | 61 | 79 |
| 88 | X | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 11 | 13 | 15 | 20 | 27 | 34 | 45 | 58 |
| 89 | Y | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 9 | 10 | 14 | 15 | 19 | 26 | 34 | 45 | 58 |
| 90 | Z | 8 | 7 | 9 | 10 | 12 | 15 | 20 | 9 | 11 | 13 | 14 | 18 | 25 | 32 | 42 | 55 |
| 91 | [ | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 4 | 5 | 6 | 7 | 9 | 12 | 15 | 19 | 25 |
| 92 | \ | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 6 | 7 | 9 | 10 | 13 | 18 | 22 | 29 | 38 |
| 93 | ] | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 4 | 5 | 7 | 7 | 9 | 12 | 15 | 19 | 25 |
| 94 | ^ | 8 | 6 | 7 | 8 | 9 | 12 | 16 | 6 | 7 | 9 | 10 | 13 | 18 | 23 | 30 | 38 |
| 95 | _ | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 11 | 13 | 16 | 21 | 26 | 34 | 43 |
| 96 | ` | 8 | 3 | 5 | 6 | 4 | 7 | 11 | 4 | 5 | 7 | 8 | 10 | 13 | 17 | 22 | 29 |
| 97 | A | 8 | 5 | 8 | 9 | 11 | 13 | 18 | 8 | 9 | 11 | 13 | 17 | 23 | 30 | 39 | 50 |
| 98 | B | 8 | 6 | 7 | 9 | 11 | 14 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 40 | 52 |
| 99 | C | 8 | 5 | 7 | 8 | 10 | 12 | 16 | 8 | 9 | 11 | 12 | 16 | 22 | 28 | 37 | 48 |
| 100 | D | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 31 | 40 | 52 |
| 101 | E | 8 | 5 | 8 | 9 | 10 | 13 | 18 | 8 | 9 | 11 | 12 | 16 | 22 | 29 | 37 | 48 |
| 102 | F | 8 | 4 | 4 | 5 | 6 | 8 | 9 | 6 | 7 | 8 | 10 | 12 | 15 | 19 | 25 | 31 |
| 103 | G | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 11 | 14 | 18 | 24 | 31 | 41 | 52 |
| 104 | H | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 41 | 52 |
| 105 | I | 8 | 2 | 3 | 3 | 4 | 6 | 7 | 3 | 4 | 6 | 6 | 7 | 10 | 13 | 18 | 23 |
| 106 | J | 8 | 2 | 3 | 4 | 4 | 6 | 7 | 3 | 4 | 6 | 6 | 8 | 11 | 14 | 18 | 23 |
| 107 | K | 8 | 5 | 7 | 8 | 9 | 12 | 16 | 7 | 9 | 11 | 13 | 16 | 22 | 28 | 36 | 47 |
| 108 | L | 8 | 2 | 3 | 3 | 4 | 6 | 7 | 3 | 4 | 6 | 6 | 7 | 10 | 13 | 18 | 23 |
| 109 | M | 8 | 8 | 11 | 14 | 16 | 20 | 27 | 11 | 15 | 18 | 21 | 27 | 36 | 47 | 63 | 80 |
| 110 | N | 8 | 6 | 8 | 9 | 10 | 14 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 41 | 52 |
| 111 | O | 8 | 6 | 8 | 9 | 11 | 13 | 18 | 8 | 10 | 12 | 13 | 17 | 24 | 31 | 40 | 52 |
| 112 | P | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 40 | 51 |
| 113 | Q | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 12 | 13 | 17 | 24 | 31 | 40 | 52 |
| 114 | R | 8 | 4 | 5 | 5 | 6 | 9 | 11 | 5 | 6 | 7 | 9 | 11 | 15 | 19 | 25 | 32 |
| 115 | S | 8 | 5 | 7 | 8 | 9 | 12 | 16 | 7 | 9 | 11 | 12 | 17 | 22 | 29 | 38 | 48 |
| 116 | T | 8 | 4 | 4 | 5 | 6 | 8 | 9 | 6 | 7 | 8 | 9 | 11 | 14 | 17 | 23 | 29 |

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| Font Index => | | | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 117 | U | 8 | 5 | 7 | 9 | 10 | 14 | 18 | 8 | 9 | 12 | 14 | 17 | 24 | 31 | 41 | 52 |
| | 118 | V | 8 | 6 | 7 | 8 | 10 | 13 | 16 | 7 | 9 | 11 | 12 | 16 | 21 | 27 | 36 | 46 |
| | 119 | W | 8 | 8 | 10 | 12 | 14 | 18 | 23 | 11 | 13 | 16 | 18 | 23 | 32 | 41 | 54 | 70 |
| | 120 | X | 8 | 6 | 7 | 8 | 10 | 12 | 16 | 7 | 9 | 11 | 12 | 16 | 21 | 27 | 36 | 46 |
| | 121 | Y | 8 | 5 | 7 | 8 | 10 | 13 | 16 | 7 | 9 | 11 | 12 | 16 | 21 | 27 | 36 | 46 |
| | 122 | Z | 8 | 5 | 7 | 8 | 9 | 12 | 16 | 8 | 9 | 11 | 12 | 15 | 22 | 27 | 36 | 46 |
| | 123 | { | 8 | 3 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 8 | 8 | 11 | 15 | 18 | 24 | 31 |
| | 124 | \| | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 5 | 6 | 7 | 10 | 14 | 18 | 23 |
| | 125 | } | 8 | 3 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 7 | 9 | 10 | 15 | 18 | 24 | 31 |
| | 126 | ~ | 8 | 7 | 8 | 10 | 10 | 14 | 19 | 10 | 11 | 14 | 15 | 21 | 29 | 36 | 47 | 63 |
| | 127 | DEL | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 4 | 5 | 6 | 5 | 10 | 13 | 18 | 23 |

**Table 4-9 ROM font ASCII character width in pixels**

| Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 128 | Ç | 144 | É | 160 | á | 176 | ░ | 192 | └ | 208 | ╨ | 224 | α | 240 | Ξ |
| 129 | ü | 145 | æ | 161 | í | 177 | ▒ | 193 | ┴ | 209 | ╤ | 225 | ß | 241 | ± |
| 130 | é | 146 | Æ | 162 | ó | 178 | ▓ | 194 | ┬ | 210 | ╥ | 226 | Γ | 242 | ≥ |
| 131 | â | 147 | ô | 163 | ú | 179 | │ | 195 | ├ | 211 | ╙ | 227 | π | 243 | ≤ |
| 132 | ä | 148 | ö | 164 | ñ | 180 | ┤ | 196 | ─ | 212 | ╘ | 228 | Σ | 244 | ⌠ |
| 133 | à | 149 | ò | 165 | Ñ | 181 | ╡ | 197 | ┼ | 213 | ╒ | 229 | σ | 245 | ⌡ |
| 134 | å | 150 | û | 166 | ª | 182 | ╢ | 198 | ╞ | 214 | ╓ | 230 | µ | 246 | ÷ |
| 135 | ç | 151 | ù | 167 | º | 183 | ╖ | 199 | ╟ | 215 | ╫ | 231 | τ | 247 | ≈ |
| 136 | ê | 152 | ÿ | 168 | ¿ | 184 | ╕ | 200 | ╚ | 216 | ╪ | 232 | Φ | 248 | ° |
| 137 | ë | 153 | Ö | 169 | ⌐ | 185 | ╣ | 201 | ╔ | 217 | ┘ | 233 | θ | 249 | • |
| 138 | è | 154 | Ü | 170 | ¬ | 186 | ║ | 202 | ╩ | 218 | ┌ | 234 | Ω | 250 | · |
| 139 | ï | 155 | ¢ | 171 | ½ | 187 | ╗ | 203 | ╦ | 219 | ▉ | 235 | δ | 251 | √ |
| 140 | î | 156 | £ | 172 | ¼ | 188 | ╝ | 204 | ╠ | 220 | ▄ | 236 | ω | 252 | ⁿ |
| 141 | ì | 157 | ¥ | 173 | ¡ | 189 | ╜ | 205 | ═ | 221 | ▌ | 237 | φ | 253 | ² |
| 142 | Ä | 158 | ₧ | 174 | « | 190 | ╛ | 206 | ╬ | 222 | ▐ | 238 | ε | 254 | ■ |
| 143 | Å | 159 | ƒ | 175 | » | 191 | ┐ | 207 | ╧ | 223 | ▀ | 239 | ∩ | 255 | nbsp |

**Table 4-10 ROM Font Extended ASCII Characters**

**Note 1:** Font 17 and 19 are extended ASCII characters, with width fixed at 8 pixels for all characters.

**Note 2:** All fonts included in the BT817/8 ROM are widely available to the market-place for general usage.

## 4.4 SPI NOR Flash Interface

The BT817/8 implements a SPI master to connect to external SPI NOR Flash. Graphics assets such as Unicode fonts and images can be stored in the flash memory. The BT817/8 graphics engine can fetch these graphics assets directly without going through external host MCU, thus significantly offloading the host MCU from feeding display contents.

The BT817/8 supports various NOR flash memory device from different vendors such as Cypress, Macronix, Winbond, Micron, ISSI and Gigadevice. The flash shall support XIP operation. The interface will work at system clock speed at 4 bit mode, providing the maximum data read throughput of 288 Mbit/s.

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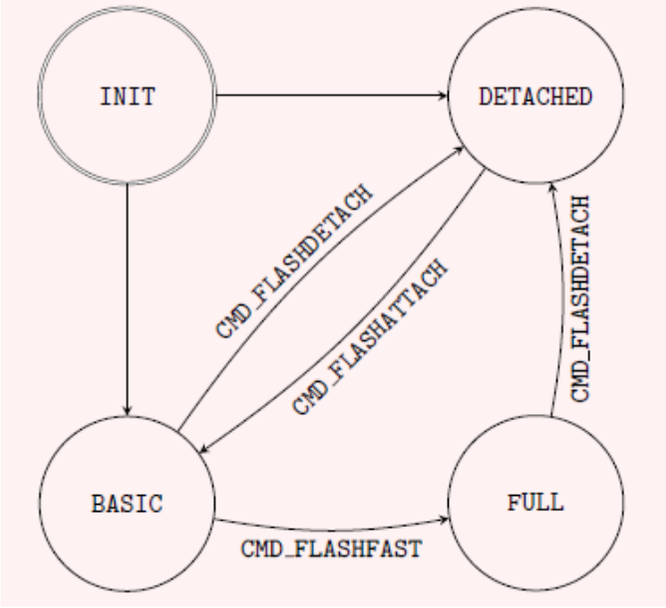



**Figure 4-5 Flash Interface States**

The register REG_FLASH_STATE indicates the state of the flash subsystem. At boot the flash state is FLASH_STATE_INIT. After detection has completed flash is in state FLASH_STATE_DETACHED or FLASH_STATE_BASIC, depending on whether an attached flash device was detected.

If no device is detected, then all SPIM signals are driven to low or high, except SPIM_MISO which is Hi-Z.

When the host MCU calls CMD_FLASHFAST, the flash system attempts to go to full-speed mode, setting state to FLASH_STATE_FULL (Note: the 4K byte flash blob file needs to program to the flash before the flash can enter full-speed mode).

At any time, the user can call CMD_FLASHDETACH in order to disable flash communications. In the detached state, commands CMD_FLASHSPIDESEL, CMD_FLASHSPITX and CMD_FLASHSPIRX can be used to control the SPI bus.

If detached, the host MCU can call CMD_FLASHATTACH to re-establish communication with the flash device.

Direct rendering of bitmaps from flash is only possible in FLASH_STATE_FULL. After modifying the contents of flash, the MCU should clear the on-chip bitmap cache by calling CMD_CLEARCACHE.

If the flash is blank (or erased using the CMD_FLASHERASE), it is recommended to use CMD_FLASHPROGRAM to program the flash in order to achieve fastest programming speed. For Micron MT25QL and Cypress S25FL-L series NOR flash, typical programming speed is about 900 kByte/s (assume SPI clock 10MHz or higher in Single SPI mode).

## 4.5 Parallel RGB Interface

The RGB parallel interface consists of 29 signals - DISP, PCLK, VSYNC, HSYNC, DE, 8 signals each for R, G and B.

A set of RGB registers configure the LCD operation and timing parameters.

REG_PCLK is used to select the display mode and clock divisor. The default value is 0, which means the display scanout is disabled and all RGB signals output Low.

When REG_PCLK is set to 1, the display output will be in EXTSYNC mode, where the PCLK frequency is controlled by REG_PCLK_FREQ from PLL2. The maximum PLL2 frequency is 228MHz. The PCLK frequency can be set up to 96MHz to align with the optimized PCLK frequency of the selected LCD

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panel. If PCLK frequency is equal to or higher than system clock frequency (up to double the system clock frequency), the REG_PCLK_2X needs to be 1 so that the graphics engine can send two pixels per system clock to the EXTSYNC block. Note that in this 2X mode, the values loaded in the following registers must be even: REG_HSIZE, REG_HOFFSET, REG_HCYCLE, REG_HSYNC0, REG_HSYNC1.

The PCLK frequency in EXTSYNC mode can be calculated as:

PLL2 frequency = 12MHz * REG_PCLK_FREQ[8:4]
PCLK frequency = PLL2 frequency / REG_PCLK_FREQ[3:0] / 2

REG_PCLK_FREQ[10:9] is determined by PLL2 frequency range:

00: 20 – 40 MHz
01: 40 – 80 MHz
10: 80 – 160 MHz
11: 160 – 228 MHz

Table 4-11 lists some of the valid PCLK frequency and REG_PCLK_FREQ values in EXTSYNC mode.

| fpclk (MHz) | REG_PCLK_ FREQ (hex) | fpclk (MHz) | REG_PCLK_ FREQ (hex) | fpclk (MHz) | REG_PCLK_ FREQ (hex) | fpclk (MHz) | REG_PCLK_ FREQ (hex) | fpclk (MHz) | REG_PCLK_ FREQ (hex) |
|---|---|---|---|---|---|---|---|---|---|
| 96 | D01 | 51 | D12 | 32 | D03 | 22 | 8B3 | 10.5 | 874 |
| 90 | CF1 | 48 | 881 | 30 | 451 | 21 | 872 | 10 | 453 |
| 84 | CE1 | 45 | CF2 | 28.5 | D34 | 19.5 | 8D4 | 9 | 32 |
| 78 | 8D1 | 42 | 871 | 28 | CE3 | 18 | 31 | 8 | 443 |
| 72 | 8C1 | 39 | 8D2 | 27 | 892 | 16.5 | 8B4 | 7.5 | 454 |
| 66 | 8B1 | 38 | D33 | 26 | 8D3 | 16 | 883 | 6 | 22 |
| 60 | 8A1 | 36 | 461 | 25.5 | D14 | 15 | 452 | 4.5 | 34 |
| 57 | D32 | 34 | D13 | 24 | 441 | 13.5 | 894 | 4 | 23 |
| 54 | 891 | 33 | 8B2 | 22.5 | CF4 | 12 | 21 | 3 | 24 |

**Table 4-11 RGB PCLK Frequency in EXTSYNC mode**

When REG_PCLK is set to 2 to 255, the display out is in pass-through mode, where the PCLK frequency can be calculated as:

PCLK frequency = System Clock frequency / REG_PCLK

The BT817/8 system clock frequency is programmable. Some of the possible PCLK frequencies that BT817/8 supports in pass-through mode are listed in Table 4-12.

| REG_PCLK | System Clock Frequency (MHz) | | | | |
|---|---|---|---|---|---|
| | 72 | 60(default) | 48 | 36 | 24 |
| 2 | 36 | 30 | 24 | 18 | 12 |
| 3 | 24 | 20 | 16 | 12 | 8.0 |
| 4 | 18 | 15 | 12 | 9.0 | 6.0 |
| 5 | 14.5 | 12 | 9.6 | 7.2 | 4.8 |
| 6 | 12 | 10 | 8.0 | 6.0 | 4.0 |
| 7 | 10.3 | 8.6 | 6.9 | 5.1 | 3.4 |
| 8 | 9 | 7.5 | 6.0 | 4.5 | 3.0 |
| 9 | 8 | 6.7 | 5.3 | 4.0 | 2.7 |
| 10 | 7.2 | 6.0 | 4.8 | 3.6 | 2.4 |

**Table 4-12 RGB PCLK Frequency in Pass-Through mode**

REG_PCLK_POL defines the clock polarity, with 0 for positive active clock edge, and 1 for negative clock edge.

REG_CSPREAD controls the transition of RGB signals with respect to the PCLK active clock edge. When REG_CSPREAD=0, R[7:0], G[7:0] and B[7:0] signals change following the active edge of PCLK. When REG_CSPREAD=1, R[7:0] changes a PCLK clock early and B[7:0] a PCLK clock later, which helps reduce the switching noise.

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REG_DITHER enables colour dither. To improve image quality, the graphics engine applies a 2x2 color dither matrix to output pixels. This option improves the half-tone appearance on displays, even on 1-bit displays. Note that the dither function is not applicable to 2X mode (REG_PCLK_2X=1).

REG_OUTBITS gives the bit width of each colour channel. The default is 8/8/8 bits for each R/G/B colour, giving total colour depth of 16,777,216 colours. A lower value means fewer bits are output for that colour channel, allowing dithering on lower precision LCD displays. A typical lower precision LCD has 6/6/6 bits for each R/G/B colour, giving total colour depth of 262,144 colours. For 6/6/6 bits configuration, pins R2-R7, G2-G7 and B2-B7 will be used, while pins R0,R1,G0,G1,B0,B1 can be left un-connected.

REG_SWIZZLE controls the arrangement of the output colour pins, to help PCB routing with different LCD panel arrangements. Bit 0 of the register causes the order of bits in each colour channel to be reversed. Bits 1-3 control the RGB order. Setting Bit 1 causes R and B channels to be swapped. Setting Bit 3 allows rotation to be enabled. If Bit 3 is set, then (R, G, B) is rotated right if bit 2 is one, or left if bit 2 is zero.

| REG_SWIZZLE | | | | RGB PINS | | |
|---|---|---|---|---|---|---|
| b3 | b2 | b1 | b0 | R7, R6, R5, R4, R3, R2, R1, R0 | G7, G6, G5, G4, G3, G2, G1, G0 | B7, B6, B5, B4, B3, B2, B1, B0 |
| 0 | X | 0 | 0 | R[7:0] | G[7:0] | B[7:0] |
| 0 | X | 0 | 1 | R[0:7] | G[0:7] | B[0:7] |
| 0 | X | 1 | 0 | B[7:0] | G[7:0] | R[7:0] |
| 0 | X | 1 | 1 | B[0:7] | G[0:7] | R[0:7] |
| 1 | 0 | 0 | 0 | B[7:0] | R[7:0] | G[7:0] |
| 1 | 0 | 0 | 1 | B[0:7] | R[0:7] | G[0:7] |
| 1 | 0 | 1 | 0 | G[7:0] | R[7:0] | B[7:0] |
| 1 | 0 | 1 | 1 | G[0:7] | R[0:7] | B[0:7] |
| 1 | 1 | 0 | 0 | G[7:0] | B[7:0] | R[7:0] |
| 1 | 1 | 0 | 1 | G[0:7] | B[0:7] | R[0:7] |
| 1 | 1 | 1 | 0 | R[7:0] | B[7:0] | G[7:0] |
| 1 | 1 | 1 | 1 | R[0:7] | B[0:7] | G[0:7] |

**Table 4-13 REG_SWIZZLE RGB Pins Mapping**

REG_HCYCLE, REG_HSIZE, REG_HOFFSET, REG_HSYNC0 and REG_HSYNC1 define the LCD horizontal timings. Each register has 12 bits to allow programmable range of 0-4095 PCLK cycles. REG_VCYCLE, REG_VSIZE, REG_VOFFSET, REG_VSYNC0 and REG_VSYNC1 define the LCD vertical timings. Each register has 12 bits to allow a programmable range of 0-4095 lines.

| | Register | Display Parameter | Description |
|---|---|---|---|
| Horizontal | REG_HCYCLE | $T_H$ | **Total** length of line (visible and non-visible) (in PCLKs) |
| | REG_HSIZE | $T_{HD}$ | Length of **visible** part of line (in PCLKs) |
| | REG_HOFFSET | $T_{HF} + T_{HP} + T_{HB}$ | Length of **non-visible** part of line. Must be < $T_H$ - $T_{HD}$ (in PCLK cycles) |
| | REG_HSYNC0 | $T_{HF}$ | Horizontal Front Porch (in PCLK cycles) |
| | REG_HSYNC1 | $T_{HF} + T_{HP}$ | Horizontal Front Porch plus Hsync Pulse width (in PCLK cycles) |
| Vertical | REG_VCYCLE | $T_V$ | **Total** number of lines (visible and non-visible) (in lines) |
| | REG_VSIZE | $T_{VD}$ | Number of **visible** lines (in lines) |
| | REG_VOFFSET | $T_{VF} + T_{VP} + T_{VB}$ | Number of **non-visible** lines. Must be < $T_V$ - $T_{VD}$ (in lines) |
| | REG_VSYNC0 | $T_{VF}$ | Vertical Front Porch (in lines) |
| | REG_VSYNC1 | $T_{VF} + T_{VP}$ | Vertical Front Porch plus Vsync Pulse width (in lines) |

**Table 4-14 Registers for RGB Horizontal and Vertical Timings**

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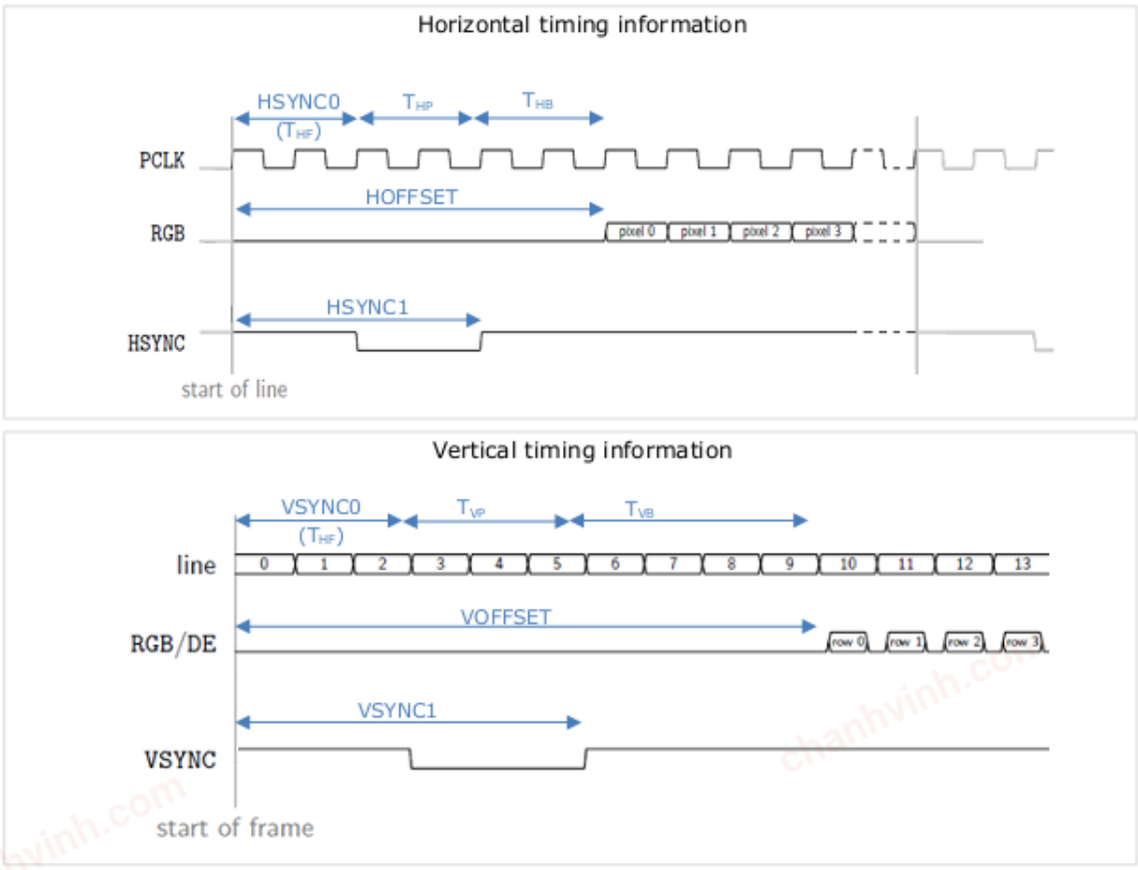



**Figure 4-6 RGB Timing Waveforms**

BT817/8 supports adaptive HSYNC and adaptive framerate operations. In adaptive HSYNC mode the graphics engine may delay the start of the scanout line up to the cycle count given in REG_AH_HCYCLE_MAX, while keeping PCLK running. Adaptive HSYNC is enabled when REG_AH_HCYCLE_MAX is set to a non-zero value between REG_HCYCLE and 4095. In adaptive framerate mode the graphics engine may suspend PLCK if the next scanout line is not ready.

BT817/8 supports Horizontal Scanout Filter (HSF) operation. The HSF applies a high-quality filter to output pixels, correcting for LCD panels with non-square pixels (the physical size of the LCD pixel is not square). HSF is enabled and disabled with CMD_HSF. Note that HSF and 2X are not supported together.

Table 4-15 lists all the supported display modes for the RGB interface.

| EXTSYNC | 2X | adaptive | HSF | Description |
|---|---|---|---|---|
| No | No | No | No | passthrough mode |
| No | No | framerate | No | passthrough, adaptive framerate |
| No | No | hsync | No | passthrough, adaptive hsync |
| No | No | * | Yes | not supported |
| Yes | No | No | No | extsync mode |
| Yes | No | No | Yes | extsync, HSF |
| Yes | No | framerate | No | extsync, adaptive framerate |
| Yes | No | framerate | Yes | extsync, adaptive framerate, HSF |
| Yes | No | hsync | No | extsync, adaptive hsync |
| Yes | No | hsync | Yes | extsync, adaptive hsync, HSF |

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| | | | | |
|---|---|---|---|---|
| Yes | Yes | No | No | extsync mode, 2X pixels |
| Yes | Yes | framerate | No | extsync, 2X, adaptive framerate |
| Yes | Yes | hsync | No | extsync, 2X, adaptive hsync |
| Yes | Yes | * | Yes | not supported |

**Table 4-15 Display mode**

## 4.6 Miscellaneous Control

### 4.6.1 Backlight Control Pin

The backlight dimming control pin (BACKLIGHT) is a Pulse-width Modulation (PWM) signal controlled by two registers: *REG_PWM_HZ* and *REG_PWM_DUTY*. REG_PWM_HZ specifies the PWM output frequency, the range is 250-10000 Hz. REG_PWM_DUTY specifies the duty cycle; the range is 0-128. A value of 0 means that the PWM is completely off and 128 means completely on.

The BACKLIGHT pin will output low when the DISP pin is not enabled (i.e. logic 0).

### 4.6.2 DISP Control Pin

The DISP pin is a general purpose output that can be used to enable or reset the LCD display panel. The pin is controlled by writing to Bit 7 of the REG_GPIO register, or bit 15 of REG_GPIOX.

### 4.6.3 General Purpose IO pins

The BT817/8 can be configured to use up to 4 GPIO pins. These GPIO pins are controlled by the REG_GPIOX_DIR and REG_GPIOX registers. Alternatively, the GPIO0 and GPIO1 pins can also be controlled by REG_GPIO_DIR and REG_GPIO to maintain backward compatibility with the FT800/FT801.

When the QSPI is enabled in Quad mode, GPIO0/IO2 and GPIO1/IO3 pins are used as data lines of the QSPI.

### 4.6.4 Pins Drive Current Control

The output drive current of output pins can be changed as per the following table by writing to bit[6:2] of REG_GPIO register or bit[14:10] of REG_GPIOX register. Alternatively, use the SPI command PINDRIVE to change the individual pin drive strength.

| REG_GPIO | Bit[6:5] | | | | Bit[4] | | Bit[3:2] | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| REG_GPIOX | Bit[14:13] | | | | Bit[12] | | Bit[11:10] | | | |
| Value | 00b# | 01b | 10b | 11b | 0b# | 1b | 00b# | 01b | 10b | 11b |
| Drive Strength Degree | DSD1 | DSD2 | DSD3 | DSD4 | DSD1 | DSD2 | DSD1 | DSD2 | DSD3 | DSD4 |
| Pins | GPIO0<br>GPIO1<br>GPIO2<br>GPIO3<br>CTP_RST_N | | | | PCLK<br>DISP<br>VSYNC<br>HSYNC<br>DE<br>R7..R0<br>G7..G0<br>B7..B0<br>BACKLIGHT | | MISO<br>MOSI<br>IO2<br>IO3<br>INT_N<br>SPIM_SCLK<br>SPIM_SS_N<br>SPIM_MOSI<br>SPIM_MISO<br>SPIM_IO2<br>SPIM_IO3 | | | |

**Table 4-16 Output Drive Current Selection**

**Note:** #Default value

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## 4.7 Audio Engine

BT817/8 provides mono audio output with sigma-delta modulation through a digital output pin, AUDIO_L. It outputs two audio sources, the sound synthesizer and audio file playback.

### 4.7.1 Sound Synthesizer

A sound processor, AUDIO ENGINE, generates the sound effects from a small ROM library of waves table. To play a sound effect listed in Table 4.3, load the REG_SOUND register with a code value and write 1 to the REG_PLAY register. The REG_PLAY register reads 1 while the effect is playing and returns a '0' when the effect ends. Some sound effects play continuously until interrupted or instructed to play the next sound effect. To interrupt an effect, write a new value to REG_SOUND and REG_PLAY registers; e.g. write 0 (Silence) to REG_SOUND and 1 to PEG_PLAY to stop the sound effect.

The sound volume is controlled by register REG_VOL_SOUND. The 16-bit REG_SOUND register takes an 8-bit sound in the low byte. For some sounds, marked "pitch adjust" in the table below, the high 8 bits contain a MIDI note value. For these sounds, a note value of zero indicates middle C. For other sounds, the high byte of REG_SOUND is ignored.

| Value | Effect | Continuous | Pitch adjust |
|---|---|---|---|
| 00h | Silence | Y | N |
| 01h | square wave | Y | Y |
| 02h | sine wave | Y | Y |
| 03h | sawtooth wave | Y | Y |
| 04h | triangle wave | Y | Y |
| 05h | Beeping | Y | Y |
| 06h | Alarm | Y | Y |
| 07h | Warble | Y | Y |
| 08h | Carousel | Y | Y |
| 10h | 1 short pip | N | Y |
| 11h | 2 short pips | N | Y |
| 12h | 3 short pips | N | Y |
| 13h | 4 short pips | N | Y |
| 14h | 5 short pips | N | Y |
| 15h | 6 short pips | N | Y |
| 16h | 7 short pips | N | Y |
| 17h | 8 short pips | N | Y |
| 18h | 9 short pips | N | Y |
| 19h | 10 short pips | N | Y |
| 1Ah | 11 short pips | N | Y |
| 1Bh | 12 short pips | N | Y |
| 1Ch | 13 short pips | N | Y |
| 1Dh | 14 short pips | N | Y |

| Value | Effect | Continuous | Pitch adjust |
|---|---|---|---|
| 32h | DTMF 2 | Y | N |
| 33h | DTMF 3 | Y | N |
| 34h | DTMF 4 | Y | N |
| 35h | DTMF 5 | Y | N |
| 36h | DTMF 6 | Y | N |
| 37h | DTMF 7 | Y | N |
| 38h | DTMF 8 | Y | N |
| 39h | DTMF 9 | Y | N |
| 40h | harp | N | Y |
| 41h | xylophone | N | Y |
| 42h | tuba | N | Y |
| 43h | glockenspiel | N | Y |
| 44h | organ | N | Y |
| 45h | trumpet | N | Y |
| 46h | piano | N | Y |
| 47h | chimes | N | Y |
| 48h | music box | N | Y |
| 49h | bell | N | Y |
| 50h | click | N | N |
| 51h | switch | N | N |
| 52h | cowbell | N | N |
| 53h | notch | N | N |
| 54h | hihat | N | N |

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| | | | |
|---|---|---|---|
| 1Eh | 15 short pips | N | Y |
| 1Fh | 16 short pips | N | Y |
| 23h | DTMF # | Y | N |
| 2Ch | DTMF * | Y | N |
| 30h | DTMF 0 | Y | N |
| 31h | DTMF 1 | Y | N |

| | | | |
|---|---|---|---|
| 55h | kickdrum | N | N |
| 56h | pop | N | N |
| 57h | clack | N | N |
| 58h | chack | N | N |
| 60h | mute | N | N |
| 61h | unmute | N | N |

**Table 4-17 Sound Effect**

| MIDI note | ANSI note | Freq (Hz) |
|---|---|---|
| 21 | A0 | 27.5 |
| 22 | A#0 | 29.1 |
| 23 | B0 | 30.9 |
| 24 | C1 | 32.7 |
| 25 | C#1 | 34.6 |
| 26 | D1 | 36.7 |
| 27 | D#1 | 38.9 |
| 28 | E1 | 41.2 |
| 29 | F1 | 43.7 |
| 30 | F#1 | 46.2 |
| 31 | G1 | 49.0 |
| 32 | G#1 | 51.9 |
| 33 | A1 | 55.0 |
| 34 | A#1 | 58.3 |
| 35 | B1 | 61.7 |
| 36 | C2 | 65.4 |
| 37 | C#2 | 69.3 |
| 38 | D2 | 73.4 |
| 39 | D#2 | 77.8 |
| 40 | E2 | 82.4 |
| 41 | F2 | 87.3 |
| 42 | F#2 | 92.5 |
| 43 | G2 | 98.0 |
| 44 | G#2 | 103.8 |
| 45 | A2 | 110.0 |
| 46 | A#2 | 116.5 |
| 47 | B2 | 123.5 |
| 48 | C3 | 130.8 |
| 49 | C#3 | 138.6 |

| MIDI note | ANSI note | Freq (Hz) |
|---|---|---|
| 65 | F4 | 349.2 |
| 66 | F#4 | 370.0 |
| 67 | G4 | 392.0 |
| 68 | G#4 | 415.3 |
| 69 | A4 | 440.0 |
| 70 | A#4 | 466.2 |
| 71 | B4 | 493.9 |
| 72 | C5 | 523.3 |
| 73 | C#5 | 554.4 |
| 74 | D5 | 587.3 |
| 75 | D#5 | 622.3 |
| 76 | E5 | 659.3 |
| 77 | F5 | 698.5 |
| 78 | F#5 | 740.0 |
| 79 | G5 | 784.0 |
| 80 | G#5 | 830.6 |
| 81 | A5 | 880.0 |
| 82 | A#5 | 932.3 |
| 83 | B5 | 987.8 |
| 84 | C6 | 1046.5 |
| 85 | C#6 | 1108.7 |
| 86 | D6 | 1174.7 |
| 87 | D#6 | 1244.5 |
| 88 | E6 | 1318.5 |
| 89 | F6 | 1396.9 |
| 90 | F#6 | 1480.0 |
| 91 | G6 | 1568.0 |
| 92 | G#6 | 1661.2 |
| 93 | A6 | 1760.0 |

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| | | | | | |
|---|---|---|---|---|---|
| 50 | D3 | 146.8 | 94 | A#6 | 1864.7 |
| 51 | D#3 | 155.6 | 95 | B6 | 1975.5 |
| 52 | E3 | 164.8 | 96 | C7 | 2093.0 |
| 53 | F3 | 174.6 | 97 | C#7 | 2217.5 |
| 54 | F#3 | 185.0 | 98 | D7 | 2349.3 |
| 55 | G3 | 196.0 | 99 | D#7 | 2489.0 |
| 56 | G#3 | 207.7 | 100 | E7 | 2637.0 |
| 57 | A3 | 220.0 | 101 | F7 | 2793.8 |
| 58 | A#3 | 233.1 | 102 | F#7 | 2960.0 |
| 59 | B3 | 246.9 | 103 | G7 | 3136.0 |
| 60 | C4 | 261.6 | 104 | G#7 | 3322.4 |
| 61 | C#4 | 277.2 | 105 | A7 | 3520.0 |
| 62 | D4 | 293.7 | 106 | A#7 | 3729.3 |
| 63 | D#4 | 311.1 | 107 | B7 | 3951.1 |
| 64 | E4 | 329.6 | 108 | C8 | 4186.0 |

**Table 4-18 MIDI Note Effect**

### 4.7.2 Audio Playback

The BT817/8 can play back recorded sound through its audio output. To do this, load the original sound data into the BT817/8's RAM, and set registers to start the playback.

The registers controlling audio playback are:

REG_PLAYBACK_START: the start address of the audio data
REG_PLAYBACK_LENGTH: the length of the audio data, in bytes
REG_PLAYBACK_FREQ: the playback sampling frequency, in Hz
REG_PLAYBACK_FORMAT: the playback format, one of LINEAR SAMPLES, uLAW SAMPLES, or ADPCM SAMPLES
REG_PLAYBACK_LOOP: if zero, the sample is played once. If one, the sample is repeated indefinitely
REG_PLAYBACK_PLAY: a write to this location triggers the start of audio playback, regardless of writing '0' or '1'. Read back '1' when playback is ongoing, and '0' when playback finishes
REG_VOL_PB: playback volume, 0-255

The mono audio formats supported are 8-bits PCM, 8-bits uLAW and 4-bits IMA-ADPCM. For ADPCM_SAMPLES, each sample is 4 bits, so two samples are packed per byte, the first sample is in bits 0-3 and the second is in bits 4-7.

The current audio playback read pointer can be queried by reading the REG_PLAYBACK_READPTR. Using a large sample buffer, looping, and this read pointer, the host MPU/MCU can supply a continuous stream of audio.

## 4.8 Touch-Screen Engine

The BT817/8 touch-screen engine supports both resistive and capacitive touch panels. BT818 supports resistive touch, while BT817 supports capacitive touch.

### 4.8.1 Resistive Touch Control

The resistive touch-screen consists of a touch screen engine, ADC, Axis-switches, and ADC input multiplexer. The touch screen engine reads commands from the memory map register and generates

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the required control signals to the axis-switches and inputs mux and ADC. The ADC data is acquired, processed, and updated in the respective register for the MPU/MCU to read.

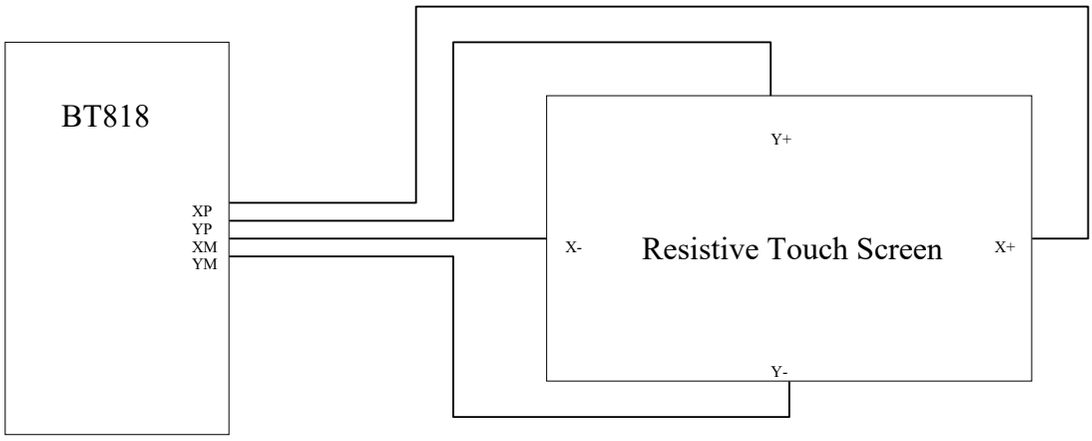



**Figure 4-7 Resistive Touch Screen Connection**

The host controls the TOUCH SCREEN ENGINE operation mode by writing the REG_TOUCH_MODE.

| REG_TOUCH_MODE | Mode | Description |
|---|---|---|
| 0 | OFF | Acquisition stopped, only touch detection interrupt is still valid. |
| 1 | ONE-SHOT | Perform acquisition once every time the MPU writes '1' to REG_TOUCH_MODE. |
| 2 | FRAME-SYNC | Perform acquisition for every frame sync (~60 data acquisition/second. |
| 3 | CONTINUOUS | Perform acquisition continuously at approximately 1000 data acquisition / second. |

**Table 4-19 Resistive Touch Controller Operating Mode**

The Touch Screen Engine captures the raw X and Y coordinate and writes to register REG_TOUCH_RAW XY. The range of these values is 0-1023. If the touch screen is not being pressed, both registers read 65535 (FFFFh).

These touch values are transformed into screen coordinates using the matrix in registers REG_TOUCH_TRANSFORM_A-F. The post-transform coordinates are available in register REG_TOUCH_SCREEN_XY. If the touch screen is not being pressed, both registers read -32768 (8000h).

The values for REG TOUCH TRANSFORM A-F may be computed using an on-screen calibration process.

If the screen is being touched, the screen coordinates are looked up in the screen's tag buffer, delivering a final 8-bit tag value, in REG TOUCH TAG. Because the tag lookup takes a full frame, and touch coordinates change continuously, the original (x; y) used for the tag lookup is also available in REG_TOUCH_TAG_XY.

Screen touch pressure is available in REG_TOUCH_RZ. The value is relative to the resistance of the touch contact, a lower value indicates more pressure. The register defaults to 32767 when touch is not detected. The REG_TOUCH_RZTHRESH (valid in touch continuous mode, frame mode and one-shot mode) can be set to accept a touch only when the force threshold is exceeded.

### 4.8.2 Capacitive Touch Control

The Capacitive Touch Screen Engine (CTSE) of the BT817 communicates with the external capacitive touch panel module (CTPM) through an $I^2C$ interface. The CTPM will assert its interrupt line when there is a touch detected. Upon detecting CTP_INT_N line active, the BT817/8 will read the touch data through $I^2C$. Up to 5 touches can be reported and stored in BT817 registers. The BT817 built-in ROM code supports Focaltech, Hycontek and Goodix touch controllers, as well as touch host mode (refer to

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section 4.8.7). For a supported CTPM list please refer to AN_336 FT8xx - Selecting an LCD Display. For other touch controller IC, consult Bridgetek.

The BT817 uses the I2C address value in the REG_TOUCH_CONFIG register to differentiate Focaltech/Hycontek and Goodix touch controllers. For Focaltech/Hycontek IC the I2C address must be set as 0x38-0x3F (example: REG_TOUCH_CONFIG = 0x0380), while for Goodix IC the I2C address must be set as 0x5D (example: REG_TOUCH_CONFIG = 0x05D0). The touch engine requires a reset if changing I2C address from default value, as shown below:

```
Write REG_CPURESET = 2
Write REG_TOUCH_CONFIG = 0x05D0          //For Goodix touch controller
Write REG_CPURESET = 0
```

The BT817 supports I2C clock stretch. This is particularly useful for supporting Hycontek touch IC.

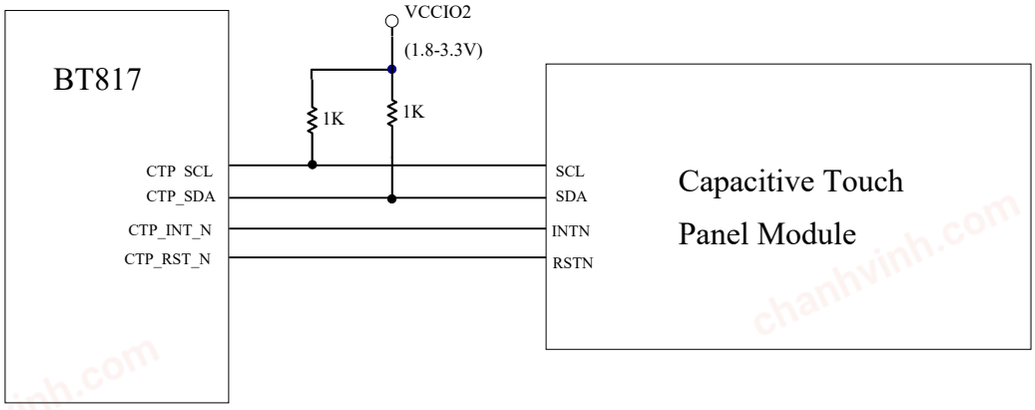



**Figure 4-8 Touch Screen Connection**

The host controls the CTSE operation mode by writing the REG_CTOUCH_MODE.

| REG_CTOUCH_MODE | Mode | Description |
|---|---|---|
| 0 | OFF | Acquisition stopped |
| 1-2 | Reserved | Reserved |
| 3 | CONTINUOUS | Perform acquisition continuously at the reporting rate of the connected CTPM. |

**Table 4-20 Capacitive Touch Controller Operating Mode**

The BT817 CTSE supports compatibility mode and extended mode. By default, the CTSE runs in compatibility mode where the touch system provides an interface similar to the resistive touch engine. In extended mode, the touch register meanings are modified, and a second set of registers are exposed. These allow multi-touch detection (up to 5 touches).

### 4.8.3 Compatibility Mode

The CTSE reads the X and Y coordinates from the CTPM and writes to register REG_CTOUCH_RAW_XY. If the touch screen is not being pressed, both registers read 65535 (FFFFh). These touch values are transformed into screen coordinates using the matrix in registers REG_CTOUCH_TRANSFORM_A-F. The post-transform coordinates are available in register REG_CTOUCH_SCREEN_XY. If the touch screen is not being pressed, both registers read -32768 (8000h). The values for REG_CTOUCH_TRANSFORM_A-F may be computed using an on-screen calibration process.

If the screen is being touched, the screen coordinates are looked up in the screen's tag buffer, delivering a final 8-bit tag value, in REG_TOUCH_TAG. Because the tag lookup takes a full frame, and touch coordinates change continuously, the original (x; y) used for the tag lookup is also available in REG_TOUCH_TAG_XY.

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### 4.8.4 Extended Mode

Setting REG_CTOUCH_EXTENDED to 1b'0 enables extended mode. In extended mode a new set of readout registers are available, allowing gestures and up to five touches to be read. There are two classes of registers: control registers and status registers. Control registers are written by the MCU. Status registers can be read out by the MCU and the BT817/8's hardware tag system.

The five touch coordinates are packed in REG_CTOUCH_TOUCH0_XY, REG_CTOUCH_TOUCH1_XY, REG_CTOUCH_TOUCH2_XY, REG_CTOUCH_TOUCH3_XY, REG_CTOUCH4_X and REG_CTOUCH4_Y.

Coordinates stored in these registers are signed 16-bit values, so have a range of -32768 to 32767. The no-touch condition is indicated by x=y= -32768. These coordinates are already transformed into screen coordinates based on the raw data read from the CTPM, using the matrix in registers REG_CTOUCH_TRANSFORM_A-F. To obtain raw (x,y) coordinates read from CTPM, the user sets the REG_CTOUCH_TRANSFORM_A-F registers to the identity matrix.

The BT817/8 tag mechanism is implemented by hardware, where up to 5 tags can be looked up.

In touch extended mode, the INT_TOUCH bit in REG_INT_FLAG register will not be set upon touch down event. It is recommended to use INT_CONV_COMPLETE bit instead.

### 4.8.5 Short-Circuit Protection

For resistive touch it is useful to protect the chip from permanent damage due to potential short-circuits on the 4 XY lines. When a short circuit on the touch screen happens, the BT818 can detect it and stop the touch detection operation, leaving the 4 XY pins in the high impedance state.

The short-circuit protection can be enabled/disabled by the REG_TOUCH_CONFIG.

### 4.8.6 Capacitive Touch Configuration

On a capacitive touch system some users may need to adjust the CTPM default values, such as the registers affecting touch sensitivity. To do this the following sequence shall be executed once after chip reset:

- Hold the touch engine in reset (set REG_CPURESET = 2)
- Write the CTPM configure register address and value to the BT817 designated memory location
- Up to 10 register address/value can be added
- Release the touch engine reset (set REG_CPURESET = 0)

Sample codes are listed below for configuring Focaltech touch controller:

```
#define FW_RD(a)    VC.rd16(RAM_JTBOOT + 2 * (a))
#define FW_WR(a, v) VC.wr16(RAM_JTBOOT + 2 * (a), (v))

void init_custom_touch(size_t num_regs, uint8_t *reg_value)
{
  while (VC.rd(REG_CPURESET) != 0)
    ;
  VC.wr(REG_CPURESET, 2);

  uint16_t main = FW_RD(0) & 0xfff;
  uint16_t i_set = 0x4000 | (main - 4);
  uint16_t patch = main + 1;
  uint16_t i_eol = FW_RD(patch);

  while (num_regs--) {
    uint8_t reg = *reg_value++;
    uint8_t val = *reg_value++;
    FW_WR(patch++, 0x8000 | val);
    FW_WR(patch++, 0x8000 | reg);
```

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```
        FW_WR(patch++, i_set);
      }
      FW_WR(patch, i_eol);

      VC.wr(REG_CPURESET, 0);
    }
```

The CTPM can be enabled in low power state when the touch function is not required by the application. Setting the low-power bit in REG_TOUCH_CONFIG will enable the low power mode of the CTPM. When the low-power bit is cleared, the BT817 touch engine will send a reset to the CTPM, thus re-enabling the touch detection function.

### 4.8.7 Host Driven Multi-Touch

If the host MCU can provide touch inputs, it can supply them directly to the BT817 using touch host mode. By using touch host mode, an application can choose to select a touch controller that is not in the BT817 direct support list. For example, Touch Host mode would allow controllers to be used from other manufacturers beyond Focaltech and Goodix.

To use the touch host mode, the host MCU shall be connected to the touch panel directly. The four touch related pins of the BT817 can be left unconnected on the PCB. The host MCU is responsible for communicating with the touch controller, fetching the touch data when reported, and writing the touch data to the BT817 for touch TAG lookup and reporting.

The touch host mode can be entered by setting bit 14 in register REG_TOUCH_CONFIG and resetting the touch engine:

- Hold the touch engine in reset (set REG_CPURESET = 2)
- Write 1 to bit 14 in REG_TOUCH_CONFIG (set REG_TOUCH_CONFIG = 0x4000)
- Release the touch engine reset (set REG_CPURESET = 0)

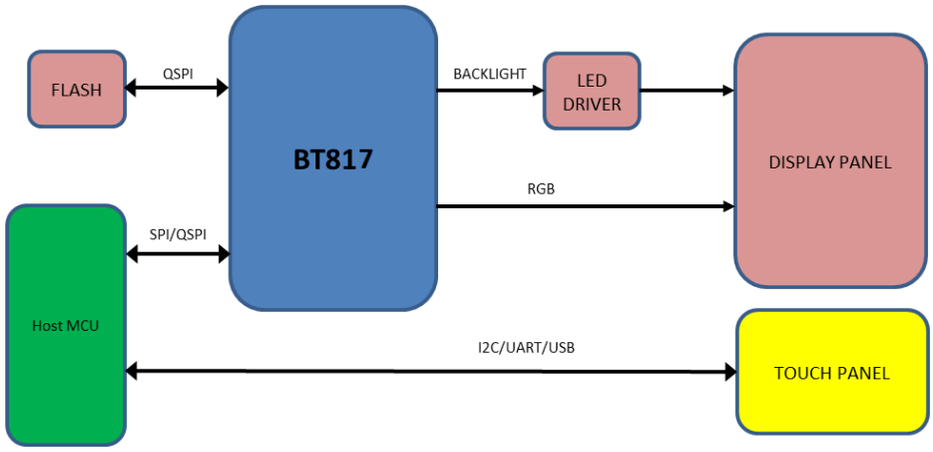



**Figure 4-9 Touch Host Mode Connections**

In touch host mode, the host supplies touch information via four registers:

| BT817 address | Register Name | Bits | Description |
|---|---|---|---|
| 0x30210c | REG_EHOST_TOUCH_X | Unsigned 16-bit | Touch x coordinate |
| 0x302118 | REG_EHOST_TOUCH_Y | Unsigned 16-bit | Touch y coordinate |
| 0x302114 | REG_EHOST_TOUCH_ID | 4-bit | Touch ID / phase |
| 0x302170 | REG_EHOST_TOUCH_ACK | 4-bit | Acknowledgement |

**Table 4-21 Registers for Touch Host Mode**

The host writes raw (x; y) coordinates and IDs to the above registers. Up to 5 touches can be set, using touch IDs 0-4. The host indicates no touch by supplying coordinates (0x8000; 0x8000). When

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the host writes 0xf to the ID register, BT817 sets the ACK register to 0, transforms all the raw coordinates, and writes the results to the regular touch registers.

Pseudocode:

```
wait until REG_EHOST_TOUCH_ACK is 1
for each touch:

    write x coordinate to REG_EHOST_TOUCH_X
    write y coordinate to REG_EHOST_TOUCH_Y
    write id to REG_EHOST_TOUCH_ID
    write 0xf to REG_EHOST_TOUCH_ID
```

As soon as BT817 has converted the coordinates, it writes 1 to the ACK register and sets the INT_CONV_COMPLETE interrupt flag.

The ID should be zero in touch compatibility mode. The host should indicate no touch at all by writing (0x8000; 0x8000) with ID 0.

In extended mode, the multiple touches may be sent in any order. Any IDs not assigned are assumed to be not pressed. Again, the host should indicate no touch at all by writing (0x8000; 0x8000) with ID 0.

The host can use three methods to ensure that BT817 is ready to accept touch inputs:

1. poll the ACK register until it is 1
2. use the INT_CONV_COMPLETE interrupt flag
3. supply touches slower than 1000 Hz, since BT817 guarantees to process the touches in under 1 ms. Note that report rates from capacitive touch panels are about 100 Hz

Like the direct capacitive driver, this touch host mode works when REG_CTOUCH_EXTENDED is both CTOUCH_MODE_EXTENDED and CTOUCH_MODE_COMPATIBILITY. CTOUCH_MODE_COMPATIBILITY should be used for the calibration procedure, just as when using native capacitive support. After changing mode, the BT817 touch engine must be reset.

### 4.8.8 Touch Detection in none-ACTIVE State

When the BT817/8 is in non-ACTIVE state, a touch event can still be detected and reported to the host through the INT_N pin. In other words, a touch event can wake-up the host if needed.

For resistive touch, the INT_N pin will be asserted low when the screen is touched, regardless of the setting of the interrupt registers. This will happen when the BT818 is in STANDBY or SLEEP state, but not in POWERDOWN state.

For capacitive touch, the INT_N pin will follow CTP_INT_N pin when the BT817 is in STANDBY, SLEEP or POWERDOWN state.

## 4.9 Power Management

### 4.9.1 Power Supply

The BT817/8 may be operated with a single supply of 3.3V applied to VCC and VCCIO pins. For operation with a host MPU/MCU at a lower supply, connect the VCCIO1 to the MPU IO supply to match the interface voltage. For operation with LCD/touch panels at lower voltages, connect the VCCIO2 to the LCD/touch IO supply.

| Symbol | Typical | Description |
|---|---|---|
| VCCIO1 | 1.8V, or 2.5V, or 3.3V | Supply for Host interface digital I/O pins |
| VCCIO2 | 1.8V, or 2.5V, or 3.3V | Supply for RGB and touch interface I/O pins |

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| | | |
|---|---|---|
| VCCIO3 | 1.8V, or 2.5V, or 3.3V | Supply for NOR Flash interface I/O pins |
| VCCA | 3.3V | Supply for AUDIO_L pin and ADC circuit |
| VCC | 3.3V | Supply for 3.3V circuits and internal 1.2V regulator |
| VOUT1V2, VCC1V2 | 1.2V | Supply for digital core. Generated by internal regulator |

**Table 4-22 Power Supply**

### 4.9.2 Internal Regulator and POR

The internal regulator outputs 1.2V to supply power to the core circuit.

The internal regulator requires a compensation capacitor (minimum 3.3uF) to be stable. A typical design uses a 4.7uF or 10uF capacitor between the VOUT1V2 and GND pins. Do not connect any other load to the VOUT1V2 pin.

The internal regulator will generate a Power-On-Reset (POR) pulse when the output voltage rises above the POR threshold. The POR will reset all the core digital circuits.

### 4.9.3 Power Modes

When the supply to VCCIO and VCC is applied, the internal regulator is powered by VCC. An internal POR pulse will be generated during the regulator power up until it is stable. After the initial power up, the BT817/8 will stay in the SLEEP state. When needed, the host can set the BT817/8 to the ACTIVE state by performing a SPI ACTIVE command. The graphics engine, the audio engine and the touch engine are only functional in the ACTIVE state. To save power the host can send a command to put the BT817/8 into any of the low power modes: STANDBY, SLEEP and POWERDOWN. In addition, the host is allowed to put the BT817/8 in POWERDOWN mode from ACTIVE mode by driving the PD_N pin to low. Refer to Figure 4-10 for the power state transitions.

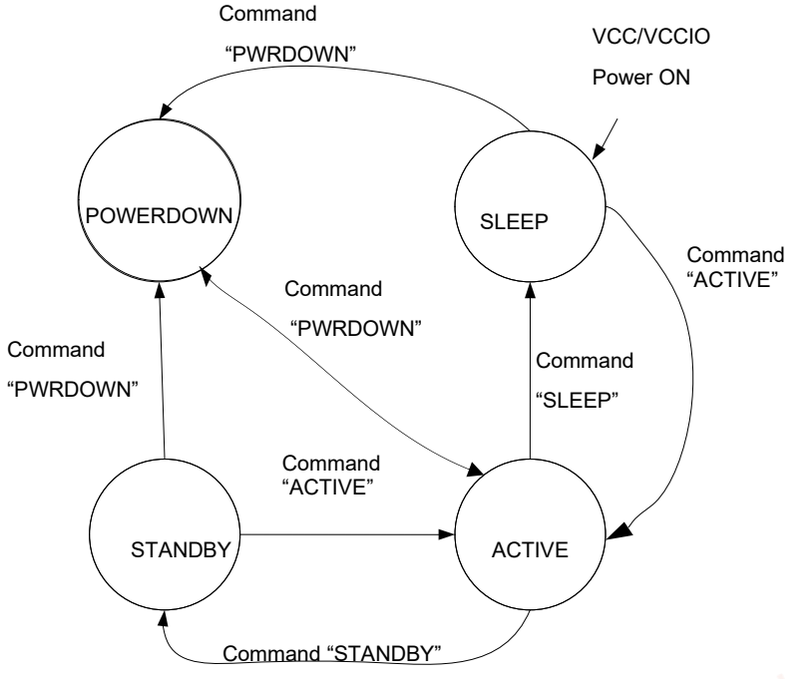



**Figure 4-10 Power State Transition**

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#### 4.9.3.1 ACTIVE state

In ACTIVE state, the BT817/8 is in normal operation. The clock oscillator and PLL are functioning. The system clock applied to the BT817/8 core engines is enabled.

#### 4.9.3.2 STANDBY state

In STANDBY state, the clock oscillator and PLL remain functioning; the system clock applied to the BT817/8 core engines is disabled. All register contents are retained.

#### 4.9.3.3 SLEEP state

In SLEEP state, the clock oscillator, PLL and system clock applied to the BT817/8 core engines are disabled. All register contents are retained.

#### 4.9.3.4 POWERDOWN state

In POWERDOWN state, the clock oscillator, the PLL and the system clock applied to the BT817/8 core is disabled. The core engines are powered down while the SPI interface for host commands remains functional. All register contents are lost and reset to default when the chip is next switched on. The internal regulator remains on.

#### 4.9.3.5 Wake up to ACTIVE from other power states

When in the POWERDOWN state, if the device enters this state via an SPI command, then only the SPI ACTIVE command will bring the device back to the ACTIVE state, provided PD_N pin is also high. However, if PD_N is used instead, then making PD_N high followed by a SPI ACTIVE command will wake up the device. Upon exiting this state, the device will perform a global reset and will go through the same power up sequence. All settings from SPI commands will be reset except those that pertain to pin states during power down. The clock enable sequence mentioned in section 4.2.3 shall be executed to select and enable the system clock.

From the SLEEP state, the host MPU sends an SPI ACTIVE command to wake the BT817/8 into the ACTIVE state. The host needs to wait for at least 20ms before accessing any registers or commands. This is to guarantee the clock oscillator and PLL are up and stable.
From the STANDBY state, the host MPU sends SPI ACTIVE command to wake the BT817/8 into the ACTIVE state. The host can immediately access any register or command.

### 4.9.4 Reset and Boot-up Sequence

There are a few hardware and software reset events which can be triggered to reset the BT817/8.
Hardware reset events:

- Power-on-Reset(POR)
- A low pulse of 5ms on PD_N pin (applicable when chip is in ACTIVE or STANDBY state)

Software reset events:

- SPI command RST_PULSE
- SPI command to enter POWERDOWN then wakeup

After reset, the BT817/8 will be in the SLEEP state. Upon receiving the SPI ACTIVE command (or CLKEXT followed by SPI ACTIVE command if external clock source is used), the clock oscillator and PLL will start up. Once the clock is stable, the chip will check and repair its internal RAM, running the configuration and then entering into normal operations. The boot-up may take up to 300ms to complete. During boot up process, software should not access BT817/8 register or RAM except reading REG_ID and REG_CPURESET.

### 4.9.5 Pin Status at Different Power States

The BT817/8 pin status depends on the power state of the chip. See the following table for more details. At the power transition from ACTIVE to STANDBY or ACTIVE to SLEEP, all pins retain their

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previous status. The software needs to set AUDIO_L, BACKLIGHT to a known state before issuing power transition commands.

The pin status in the power down state can be changed by SPI command PIN_PD_STATE.

| Pin Name | Default Drive Strength Degree | Reset | Normal | Power Down (Default) |
|---|---|---|---|---|
| AUDIO_L | DSD4 | Out, Float | Out | Retain |
| SCK | - | In | In | In |
| MISO | DSD1 | Out, Float (CS_N = 1) | IO | Out, Float |
| MOSI | DSD1 | In | IO | In |
| CS_N | - | In | In | In |
| IO2<br>GPIO0 | DSD1 | In<br>In | IO<br>IO | Float<br>Float |
| IO3<br>GPIO1 | DSD1 | In<br>In | IO<br>IO | Float<br>Float |
| GPIO2 | DSD1 | In | IO | Float |
| INT_N | DSD1 | OD, Float | OD / Out | Float |
| PD_N | - | In | In | In |
| GPIO3 | DSD1 | In | IO | Float |
| SPIM_SCLK | DSD1 | Float | Out | Float |
| SPIM_MISO | DSD1 | Float | IO | Float |
| SPIM_MOSI | DSD1 | Float | IO | Float |
| SPIM_SS_N | DSD1 | Float | Out | Float |
| SPIM_IO2 | DSD1 | Float | IO | Float |
| SPIM_IO3 | DSD1 | Float | IO | Float |
| X1/CLK | - | In | In | In |
| X2 | | Out | Out | High |
| XP | - | IO, Float | IO | High |
| YP | - | IO, Float | IO | High |
| XM | - | IO, Float | IO | Retain |
| YM | - | IO, Float | IO | Retain |
| CTP_RST_N | DSD1 | Low | Out | Pull Low |
| CTP_INT_N | DSD1 | In | IO | In |
| CTP_SCL | DSD4 | OD | I/OD | Float |
| CTP_SDA | DSD4 | OD | I/OD | Float |
| BACKLIGHT | DSD1 | Low | Out | Pull Low |
| DE | DSD1 | Low | Out | Pull Low |
| VSYNC | DSD1 | Low | Out | Pull Low |
| HSYNC | DSD1 | Low | Out | Pull Low |
| DISP | DSD1 | Low | Out | Pull Low |
| PCLK | DSD1 | Low | Out | Pull Low |
| R/G/B | DSD1 | Low | Out | Pull Low |

**Table 4-23 Pin Status**

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# 5 Memory Map

All memory and registers in the BT817/8 core are memory mapped in 22-bit address space with a 2-bit SPI command prefix. Prefix 0'b00 for read and 0'b10 for write to the address space, 0'b01 is reserved for Host Commands and 0'b11 undefined. The following are the memory space definition.

| Start Address | End Address | Size | NAME | Description |
|---|---|---|---|---|
| 00 0000h | 0F FFFFh | 1024 kB | RAM_G | General purpose graphics RAM |
| 20 0000h | 2F FFFFh | 1024 kB | ROM | ROM codes, font table and bitmap |
| 30 0000h | 30 1FFFh | 8 kB | RAM_DL | Display List RAM |
| 30 2000h | 30 2FFFh | 4 kB | RAM_REG | Registers |
| 30 8000h | 30 8FFFh | 4 kB | RAM_CMD | Command buffer |
| 30 9800h | 30 98FFh | 128 B | RAM_ERR_REPORT | Coprocessor fault report RAM |
| 30 B000h | 30 B7FFh | 2 kB | RAM_JTBOOT | Touch control codes |
| 80 0000h | 107F FFFFh | 256 MB | FLASH | External NOR flash memory. Maximum 256MB. The address is used by internal command only. |

**Table 5-1 BT817/8 Memory Map**

**Note 1:** The addresses beyond this table are reserved and shall not be read or written unless otherwise specified.

## 5.1 Registers

Table 5-2 shows the complete list of the BT817/8 registers. Refer to BT81X Series Programming Guide, Chapter 3 for details of the register function.

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---|---|---|---|---|---|
| 302000h | REG_ID | 8 | r/o | 7Ch | Identification register, always reads as 7Ch |
| 302004h | REG_FRAMES | 32 | r/o | 0 | Frame counter, since reset |
| 302008h | REG_CLOCK | 32 | r/o | 0 | Clock cycles, since reset |
| 30200Ch | REG_FREQUENCY | 28 | r/w | 48000000 | Main clock frequency (Hz). Firmware sets to 60000000 at boot. |
| 302010h | REG_RENDERMODE | 1 | r/w | 0 | Rendering mode: 0 = normal, 1 = single-line |
| 302014h | REG_SNAPY | 11 | r/w | 0 | Scanline select for RENDERMODE 1 |
| 302018h | REG_SNAPSHOT | 1 | r/w | - | Trigger for RENDERMODE 1 |
| 30201Ch | REG_SNAPFORMAT | 6 | r/w | 20h | Pixel format for scanline readout |
| 302020h | REG_CPURESET | 3 | r/w | 2 | Graphics, audio, and touch engines reset control. Bit2: audio, bit1: touch, bit0: graphics |
| 302024h | REG_TAP_CRC | 32 | r/o | - | Live video tap crc. Frame CRC is computed every DL SWAP. |
| 302028h | REG_TAP_MASK | 32 | r/w | FFFFFFFFh | Live video tap mask |
| 30202Ch | REG_HCYCLE | 12 | r/w | 224h | Horizontal total cycle count |
| 302030h | REG_HOFFSET | 12 | r/w | 02Bh | Horizontal display start offset |
| 302034h | REG_HSIZE | 12 | r/w | 1E0h | Horizontal display pixel count |
| 302038h | REG_HSYNC0 | 12 | r/w | 000h | Horizontal sync fall offset |
| 30203Ch | REG_HSYNC1 | 12 | r/w | 029h | Horizontal sync rise offset |
| 302040h | REG_VCYCLE | 12 | r/w | 124h | Vertical total cycle count |
| 302044h | REG_VOFFSET | 12 | r/w | 00Ch | Vertical display start offset |
| 302048h | REG_VSIZE | 12 | r/w | 110h | Vertical display line count |
| 30204Ch | REG_VSYNC0 | 10 | r/w | 000h | Vertical sync fall offset |
| 302050h | REG_VSYNC1 | 10 | r/w | 00Ah | Vertical sync rise offset |

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| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---|---|---|---|---|---|
| 302054h | REG_DLSWAP | 2 | r/w | 0 | Display list swap control |
| 302058h | REG_ROTATE | 3 | r/w | 0 | Screen rotation control. Allow normal/mirrored/inverted for landscape or portrait orientation. |
| 30205Ch | REG_OUTBITS | 9 | r/w | 0 | Output bit resolution, 3 register bits each for R/G/B data pins. 0 indicates 8 bits, 1-7 indicates 1-7 bits, respectively. |
| 302060h | REG_DITHER | 1 | r/w | 1 | Output dither enable |
| 302064h | REG_SWIZZLE | 4 | r/w | 0 | Output RGB signal swizzle |
| 302068h | REG_CSPREAD | 1 | r/w | 1 | Output clock spreading enable |
| 30206Ch | REG_PCLK_POL | 1 | r/w | 0 | PCLK polarity:<br>0: output on PCLK rising edge,<br>1: output on PCLK falling edge |
| 302070h | REG_PCLK | 8 | r/w | 0 | PCLK frequency divider<br>0: disable<br>1: EXTSYNC mode<br>2-255: divider from system clock |
| 302074h | REG_TAG_X | 11 | r/w | 0 | Tag query X coordinate |
| 302078h | REG_TAG_Y | 11 | r/w | 0 | Tag query Y coordinate |
| 30207Ch | REG_TAG | 8 | r/o | 0 | Tag query result |
| 302080h | REG_VOL_PB | 8 | r/w | FFh | Volume for playback |
| 302084h | REG_VOL_SOUND | 8 | r/w | FFh | Volume for synthesizer sound |
| 302088h | REG_SOUND | 16 | r/w | 0 | Sound effect select |
| 30208Ch | REG_PLAY | 1 | r/w | 0h | Start effect playback |
| 302090h | REG_GPIO_DIR | 8 | r/w | 80h | Legacy GPIO pin direction,<br>0 = input , 1 = output |
| 302094h | REG_GPIO | 8 | r/w | 00h | Legacy GPIO read/write |
| 302098h | REG_GPIOX_DIR | 16 | r/w | 8000h | Extended GPIO pin direction,<br>0 = input , 1 = output |
| 30209Ch | REG_GPIOX | 16 | r/w | 0080h | Extended GPIO read/write |
| 3020A0h - 3020A4h | Reserved | - | - | - | Reserved |
| 3020A8h | REG_INT_FLAGS | 9 | r/o | 000h | Interrupt flags, clear by read |
| 3020Ach | REG_INT_EN | 1 | r/w | 0 | Global interrupt enable, 1=enable |
| 3020B0h | REG_INT_MASK | 9 | r/w | 1FFh | Individual interrupt enable, 1=enable. Firmware sets to ffh at boot. |
| 3020B4h | REG_PLAYBACK_START | 20 | r/w | 0 | Audio playback RAM start address |
| 3020B8h | REG_PLAYBACK_LENGTH | 20 | r/w | 0 | Audio playback sample length (bytes) |
| 3020BCh | REG_PLAYBACK_READPTR | 20 | r/o | - | Audio playback current read pointer |
| 3020C0h | REG_PLAYBACK_FREQ | 16 | r/w | 8000 | Audio playback sampling frequency (Hz) |
| 3020C4h | REG_PLAYBACK_FORMAT | 2 | r/w | 0 | Audio playback format |
| 3020C8h | REG_PLAYBACK_LOOP | 1 | r/w | 0 | Audio playback loop enable |
| 3020CCh | REG_PLAYBACK_PLAY | 1 | r/w | 0 | Start audio playback |
| 3020D0h | REG_PWM_HZ | 14 | r/w | 250 | BACKLIGHT PWM output frequency (Hz) |
| 3020D4h | REG_PWM_DUTY | 8 | r/w | 128 | BACKLIGHT PWM output duty cycle 0=0%, 128=100% |
| 3020D8h | REG_MACRO_0 | 32 | r/w | 0 | Display list macro command 0 |
| 3020DCh | REG_MACRO_1 | 32 | r/w | 0 | Display list macro command 1 |
| 3020E0h – 3020F4h | Reserved | - | - | - | Reserved |
| 3020F8h | REG_CMD_READ | 12 | r/w | 0 | Command buffer read pointer |

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| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---|---|---|---|---|---|
| 3020FCh | REG_CMD_WRITE | 12 | r/o | 0 | Command buffer write pointer |
| 302100h | REG_CMD_DL | 13 | r/w | 0 | Command display list offset |
| 302104h | REG_TOUCH_MODE | 2 | r/w | 3 | Touch-screen sampling mode |
| 302108h | REG_TOUCH_ADC_MODE<br>REG_CTOUCH_EXTENDED | 1 | r/w | 1 | Set Touch ADC mode<br>Set capacitive touch operation mode:<br>0: extended mode (multi-touch)<br>1: FT800 compatibility mode (single touch). |
| 30210Ch | REG_TOUCH_CHARGE<br>REG_EHOST_TOUCH_X | 16 | r/w | 9000 | Touch charge time, units of 6 clocks<br>Touch host mode: touch x value updated by host |
| 302110h | REG_TOUCH_SETTLE | 4 | r/w | 3 | Touch settle time, units of 6 clocks |
| 302114h | REG_TOUCH_OVERSAMPLE<br>REG_EHOST_TOUCH_ID | 4 | r/w | 7 | Touch oversample factor<br>Touch host mode: touch ID, 0-4 |
| 302118h | REG_TOUCH_RZTHRESH<br>REG_EHOST_TOUCH_Y | 16 | r/w | FFFFh | Touch resistance threshold<br>Touch host mode: touch x value updated by host |
| 30211Ch | REG_TOUCH_<br>RAW_XY<br>REG_CTOUCH_TOUCH1_XY | 32 | r/o | - | Compatibility mode: touch-screen raw (x-MSB16; y-LSB16)<br>Extended mode: touch-screen screen data for touch 1 (x-MSB16; y-LSB16) |
| 302120h | REG_TOUCH_RZ<br>REG_CTOUCH_TOUCH4_Y | 16 | r/o | - | Compatibility mode: touch-screen resistance<br>Extended mode: touch-screen screen Y data for touch 4 |
| 302124h | REG_TOUCH_<br>SCREEN_XY<br>REG_CTOUCH_TOUCH0_XY | 32 | r/o | - | Compatibility mode: touch-screen screen (x-MSB16; y-LSB16)<br>Extended mode: touch-screen screen data for touch 0 (x-MSB16; y-LSB16) |
| 302128h | REG_TOUCH_<br>TAG_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 0 lookup |
| 30212Ch | REG_TOUCH_TAG | 8 | r/o | - | Touch-screen tag result 0 |
| 302130h | REG_TOUCH_<br>TAG1_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 1 lookup |
| 302134h | REG_TOUCH_TAG1 | 8 | r/o | - | Touch-screen tag result 1 |
| 302138h | REG_TOUCH_<br>TAG2_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 2 lookup |
| 30213Ch | REG_TOUCH_TAG2 | 8 | r/o | - | Touch-screen tag result 2 |
| 302140h | REG_TOUCH_<br>TAG3_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 3 lookup |
| 302144h | REG_TOUCH_TAG3 | 8 | r/o | - | Touch-screen tag result 3 |
| 302148h | REG_TOUCH_<br>TAG4_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 4 lookup |
| 30214Ch | REG_TOUCH_TAG4 | 8 | r/o | - | Touch-screen tag result 4 |
| 302150h | REG_TOUCH_TRANSFORM_A | 32 | r/w | 00010000h | Touch-screen transform coefficient (s15.16) |
| 302154h | REG_TOUCH_TRANSFORM_B | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 302158h | REG_TOUCH_TRANSFORM_C | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 30215Ch | REG_TOUCH_TRANSFORM_D | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |

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| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---|---|---|---|---|---|
| 302160h | REG_TOUCH_TRANSFORM_E | 32 | r/w | 00010000h | Touch-screen transform coefficient (s15.16) |
| 302164h | REG_TOUCH_TRANSFORM_F | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 302168h | REG_TOUCH_CONFIG | 16 | r/w | 8381h (BT818)<br>0381h (BT817) | Touch configuration.<br>RTP/CTP select<br>RTP: short-circuit, sample clocks<br>CTP: I2C address, CTPM type, low-power mode, touch host mode |
| 30216Ch | REG_CTOUCH_TOUCH4_X | 16 | r/o | - | Extended mode: touch-screen screen X data for touch 4 |
| 302170h | REG_EHOST_TOUCH_ACK | 4 | r/w | 0 | Touch host mode: acknowledgement |
| 302174h | REG_BIST_EN | 1 | r/w | 0 | BIST memory mapping enable |
| 302178h - 302187Ch | Reserved | - | - | - | Reserved |
| 302184h | REG_ANA_COMP | 8 | r/w | 0 | Analogue control register |
| 302188h | REG_SPI_WIDTH | 3 | r/w | 0 | QSPI bus width setting<br>Bit [2]: extra dummy cycle on read<br>Bit [1:0]: bus width (0=1-bit, 1=2-bit, 2=4-bit) |
| 30218Ch | REG_TOUCH_DIRECT_XY<br><br>REG_CTOUCH_TOUCH2_XY | 32 | r/o | - | Compatibility mode: Touch screen direct (x-MSB16; y-LSB16) conversions<br>Extended mode: touch-screen screen data for touch 2 (x-MSB16; y-LSB16) |
| 302190h | REG_TOUCH_DIRECT_Z1Z2<br><br>REG_CTOUCH_TOUCH3_XY | 32 | r/o | - | Compatibility mode: Touch screen direct (z1-MSB16; z2-LSB16) conversions<br>Extended mode: touch-screen screen data for touch 3 (x-MSB16; y-LSB16) |
| 302194h - 302560h | Reserved | - | - | - | Reserved |
| 302564h | REG_DATESTAMP | 128 | r/o | - | Stamp date code |
| 302574h | REG_CMDB_SPACE | 12 | r/w | FFCh | Command DL (bulk) space available |
| 302578h | REG_CMDB_WRITE | 32 | w/o | 0 | Command DL (bulk) write |
| 30257Ch | REG_ADAPTIVE_FRAMERATE | 1 | r/w | 1 | Reduce frame rate during complex drawing |
| 3025ECh | REG_PLAYBACK_PAUSE | 1 | r/w | 0 | Audio playback control. 0: play, 1: pause |
| 3025F0h | REG_FLASH_STATUS | 2 | r/w | 0 | Flash status. 0: INIT, 1: DETACHED, 2: BASIC, 3: FULL |
| 3025F4h-302608h | Reserved | - | - | - | Reserved |
| 30260Ch | REG_UNDERRUN | 32 | r/o | - | Line underrun counter |
| 302610h | REG_AH_HCYCLE_MAX | 12 | r/w | 0 | Adaptive Hsync: maximum horizontal total PCLK cycles. 0 means Adaptive Hsync is disabled. |
| 302614h | REG_PCLK_FREQ | 16 | r/w | 0 | Fractional PCLK frequency/enable. Firmware sets to 08A1h at boot. |

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| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---|---|---|---|---|---|
| 302618h | REG_PCLK_2X | 1 | r/w | 0 | Core scan out 2 pixel data per system clock |
| 309000h | REG_TRACKER | 32 | r/w | 0 | Tracker register 0 |
| 309004h | REG_TRACKER_1 | 32 | r/w | 0 | Tracker register 1 |
| 309008h | REG_TRACKER_2 | 32 | r/w | 0 | Tracker register 2 |
| 30900Ch | REG_TRACKER_3 | 32 | r/w | 0 | Tracker register 3 |
| 309010h | REG_TRACKER_4 | 32 | r/w | 0 | Tracker register 4 |
| 309014h | REG_MEDIAFIFO_READ | 32 | r/o | - | Media FIFO read offset |
| 309018h | REG_MEDIAFIFO_WRITE | 32 | r/w | 0 | Media FIFO write offset |
| 309024h | REG_FLASH_SIZE | 32 | r/o | - | Detected flash capacity, in Mbytes |
| 30902Ch | REG_ANIM_ACTIVE | 32 | r/o | - | 32-bit mask of currently playing animations |
| 30914Eh | REG_PLAY_CONTROL | 8 | r/w | 0 | Video playback control. 0: pause, 1: play, ffh: exit |

**Table 5-2 Overview of BT817/8 Registers**

**Note:** All register addresses are 4-byte aligned. The value in the "Bits" column refers to the number of valid bits from bit 0 unless otherwise specified; other bits are reserved.

## 5.2 Chip ID

The BT817/8 Chip ID can be read at memory location 0C0000h – 0C0003h. The reset values of these bytes are:

- 0C0000h: 08h
- 0C0001h: 17h (BT817), 18h(BT818)
- 0C0002h: 01h
- 0C0003h: 00h

Note that the Chip ID memory location is part of RAM_G, which can be over-written by the user software. A reset event defined in section 4.9.4 will bring back the Chip ID information in these memory locations.

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# 6 Devices Characteristics and Ratings

## 6.1 Absolute Maximum Ratings

The absolute maximum ratings for the BT817/8 devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

| Parameter | Value | Unit |
|---|---|---|
| Storage Temperature | -65 to +150 | °C |
| Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity) | 168 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)* | Hours |
| Ambient Temperature (Power Applied) | -40 to +85 | °C |
| VCC Supply Voltage | 0 to +4 | V |
| VCCIO Supply Voltage | 0 to +4 | V |
| DC Input Voltage | -0.5 to + 5.5V | V |

**Table 6-1 Absolute Maximum Ratings**

* If the devices are stored out of the packaging, beyond this time limit, the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

## 6.2 ESD and Latch-up Specifications

| Description | Specification |
|---|---|
| **Human Body Mode (HBM)** | **> ± 2kV** |
| **Machine mode (MM)** | **> ± 200V** |
| **Latch-up** | **> ± 200mA** |

**Table 6-2 ESD and Latch-Up Specifications**

## 6.3 DC Characteristics

Typical condition refers to: VCC=3.3V, VCCIO=3.3V, Ta=25 °C, unless otherwise stated

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| VCCIO1/ VCCIO2/ VCCIO3 | VCCIO operating supply voltage | 1.62 | 1.8 | 1.98 | V | Normal Operation |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 3.0 | 3.3 | 3.6 | V | |
| VCC/ VCCA | VCC operating supply voltage | 3.0 | 3.3 | 3.6 | V | Normal Operation |
| Icc1 | Power Down current | - | 0.2 | - | mA | Power down mode |
| Icc2 | Sleep current | - | 0.6 | - | mA | Sleep Mode |
| Icc3 | Standby current | - | 3.6 | - | mA | Standby Mode |
| Icc4 | Operating current | - | 30 | - | mA | Normal Operation |

**Table 6-3 Operating Voltage and Current**

| Pin Group | drive strength | 1.8V | 2.5V | 3.3V | Unit |
|---|---|---|---|---|---|
| Pin group A: R[7:0], G[7:0], B[7:0], PCLK, HSYNC, VSYNC, DE, DISP, BACKLIGHT, CTP_RST_N, CTP_INT_N, CTP_SCL, CTP_SDA | DSD1 | 1.2 | 2 | 2.5 | mA |
| | DSD2 | 2.4 | 4 | 5 | mA |
| | DSD3 | 3.6 | 6 | 7.5 | mA |
| | DSD4 | 4.8 | 8 | 10 | mA |
| Pin group B: MOSI, MISO, GPIO0/IO2, GPIO1/IO3, INT_N, GPIO2, GPIO3, AUDIO_L, SPIM_SCK, SPIM_MOSI, SPIM_MISO, SPIM_CS_N, SPIM_IO2, SPIM_IO3 | DSD1 | 2.4 | 3.8 | 5 | mA |
| | DSD2 | 4.8 | 7.6 | 10 | mA |
| | DSD3 | 7.2 | 11.4 | 15 | mA |
| | DSD4 | 9.6 | 15.2 | 20 | mA |

**Table 6-4 Digital Output Pin Drive Strength**

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| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | VCCIO-0.5 | - | - | V | Ioh: refer to Table 6-4 |
| Vol | Output Voltage Low | - | - | 0.4 | V | Iol: refer to Table 6-4 |
| Vih | Input High Voltage | 2.0 | - | 5.5 | V | |
| Vil | Input Low Voltage | - | - | 0.8 | V | |
| Vth | Schmitt Hysteresis Voltage | 0.22 | - | 0.3 | V | |
| Iin | Input leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Ioz | Tri-state output leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Rpu | Pull-up resistor | - | 42 | - | kΩ | |
| Rpd | Pull-down resistor | - | 44 | - | kΩ | |

**Table 6-5 Digital I/O Pin Characteristics (VCCIO = +3.3V)**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | VCCIO-0.4 | - | - | V | Ioh: refer to Table 6-4 |
| Vol | Output Voltage Low | - | - | 0.4 | V | Iol: refer to Table 6-4 |
| Vih | Input High Voltage | 1.7 | - | 3.6 | V | |
| Vil | Input Low Voltage | - | - | 0.7 | V | |
| Vth | Schmitt Hysteresis Voltage | 0.2 | - | 0.3 | V | |
| Iin | Input leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Ioz | Tri-state output leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Rpu | Pull-up resistor | - | 57 | - | kΩ | |
| Rpd | Pull-down resistor | - | 59 | - | kΩ | |

**Table 6-6 Digital I/O Pin Characteristics (VCCIO = +2.5V)**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | VCCIO-0.4 | - | - | V | Ioh: refer to Table 6-4 |
| Vol | Output Voltage Low | - | - | 0.4 | V | Iol: refer to Table 6-4 |
| Vih | Input High Voltage | 1.2 | - | 2.75 | V | - |
| Vil | Input Low Voltage | - | - | 0.6 | V | - |
| Vth | Schmitt Hysteresis Voltage | 0.17 | - | 0.3 | V | - |
| Iin | Input leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Ioz | Tri-state output leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Rpu | Pull-up resistor | - | 90 | - | kΩ | |
| Rpd | Pull-down resistor | - | 97 | - | kΩ | |

**Table 6-7 Digital I/O Pin Characteristics (VCCIO = +1.8V)**

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| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Rsw-on | X-,X+,Y- and Y+ Drive On resistance | - | 6 | 10 | Ω | VCCIO=3.3V |
| | | - | 9 | 16 | Ω | VCCIO=1.8V |
| Rsw-off | X-,X+,Y- and Y+ Drive Off resistance | 10 | - | - | MΩ | |
| Rpu | Touch sense pull up resistance | 78 | 100 | 125 | kΩ | |
| Vth+ | Touch Detection rising-edge threshold on XP pin | 1.59 | - | 2.04 | V | VCCIO=3.3V |
| | | 0.58 | - | 0.68 | V | VCCIO=1.8V |
| Vth- | Touch Detection falling-edge threshold on XP pin | 1.23 | - | 1.55 | V | VCCIO=3.3V |
| | | 0.51 | - | 0.56 | V | VCCIO=1.8V |
| Rl | X-axis and Y-axis drive load resistance | 200 | - | - | Ω | |

**Table 6-8 Touch Sense Characteristics**

## 6.4 AC Characteristics

### 6.4.1 System Clock and Reset

| Parameter | Value | | | Units |
|---|---|---|---|---|
| | Minimum | Typical | Maximum | |
| Crystal | | | | |
| Frequency | - | 12.000 | - | MHz |
| X1/X2 Capacitance | - | - | 10 | pF |
| Reset | | | | |
| Reset pulse on PD_N (active state) | 5 | | | ms |

**Table 6-9 System Clock Characteristics**

### 6.4.2 SPI Interface Timing

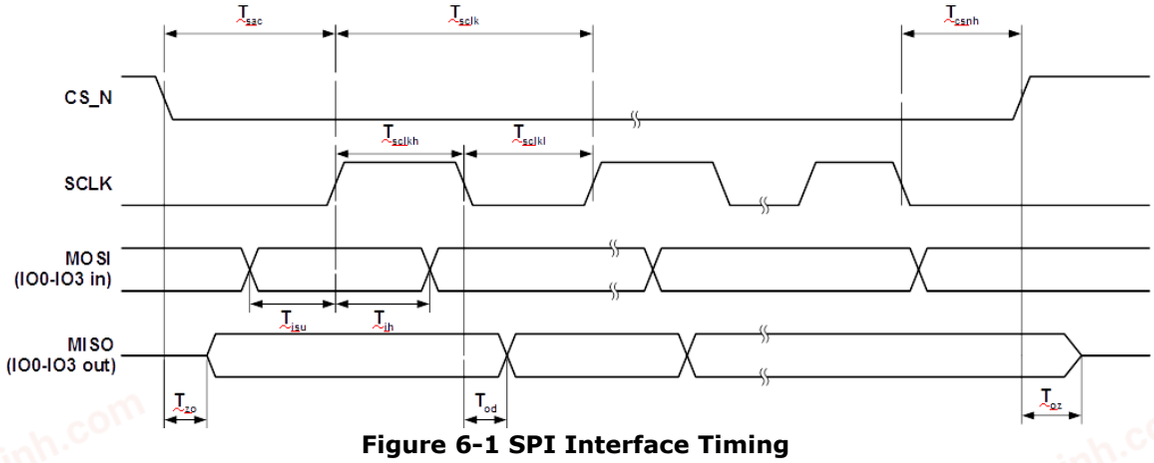



**Figure 6-1 SPI Interface Timing**

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| Parameter | Description | VCCIO=1.8V | | VCCIO=2.5V | | VCCIO=3.3V | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Tsclk | SPI clock period | 33.3 | | 33.3 | | 33.3 | | Ns |
| Tsclkl | SPI clock low duration | 13 | | 13 | | 13 | | Ns |
| Tsclkh | SPI clock high duration | 13 | | 13 | | 13 | | Ns |
| Tsac | SPI access time | 4 | | 3.5 | | 3 | | ns |
| Tisu | Input Setup | 4 | | 3.5 | | 3 | | Ns |
| Tih | Input Hold | 0 | | 0 | | 0 | | Ns |
| Tzo | Output enable delay | | 16 | | 13 | | 11 | Ns |
| Toz | Output disable delay | | 13 | | 11 | | 10 | Ns |
| Tod | Output data delay | | 15 | | 12 | | 11 | Ns |
| Tcsnh | CSN hold time | 0 | | 0 | | 0 | | Ns |

**Table 6-10 SPI Interface Timing Specifications**

### 6.4.3 RGB Interface Timing

| Parameter | Description | Value | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Tpclk | Pixel Clock period | 10.4 | | | ns |
| Td | Output delay relative to PCLK rising edge (REG_PCLK_POL=0) or falling edge (REG_PCLK_POL=1). Applied for all the RGB output pins. | | | 4 | Ns |
| Th | Output hold time relative to PCLK rising edge (REG_PCLK_POL=0) or falling edge (REG_PCLK_POL=1). Applied for all the RGB output pins. | 0.5 | | | Ns |

**Table 6-11 RGB Interface Timing Characteristics**

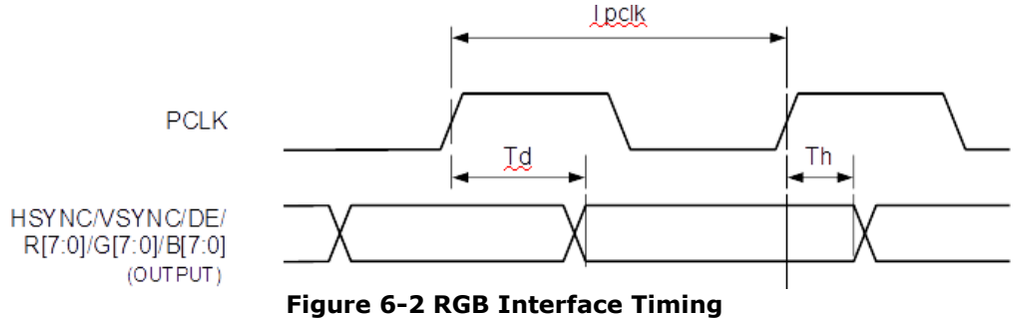



**Figure 6-2 RGB Interface Timing**

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# 7 Application Examples

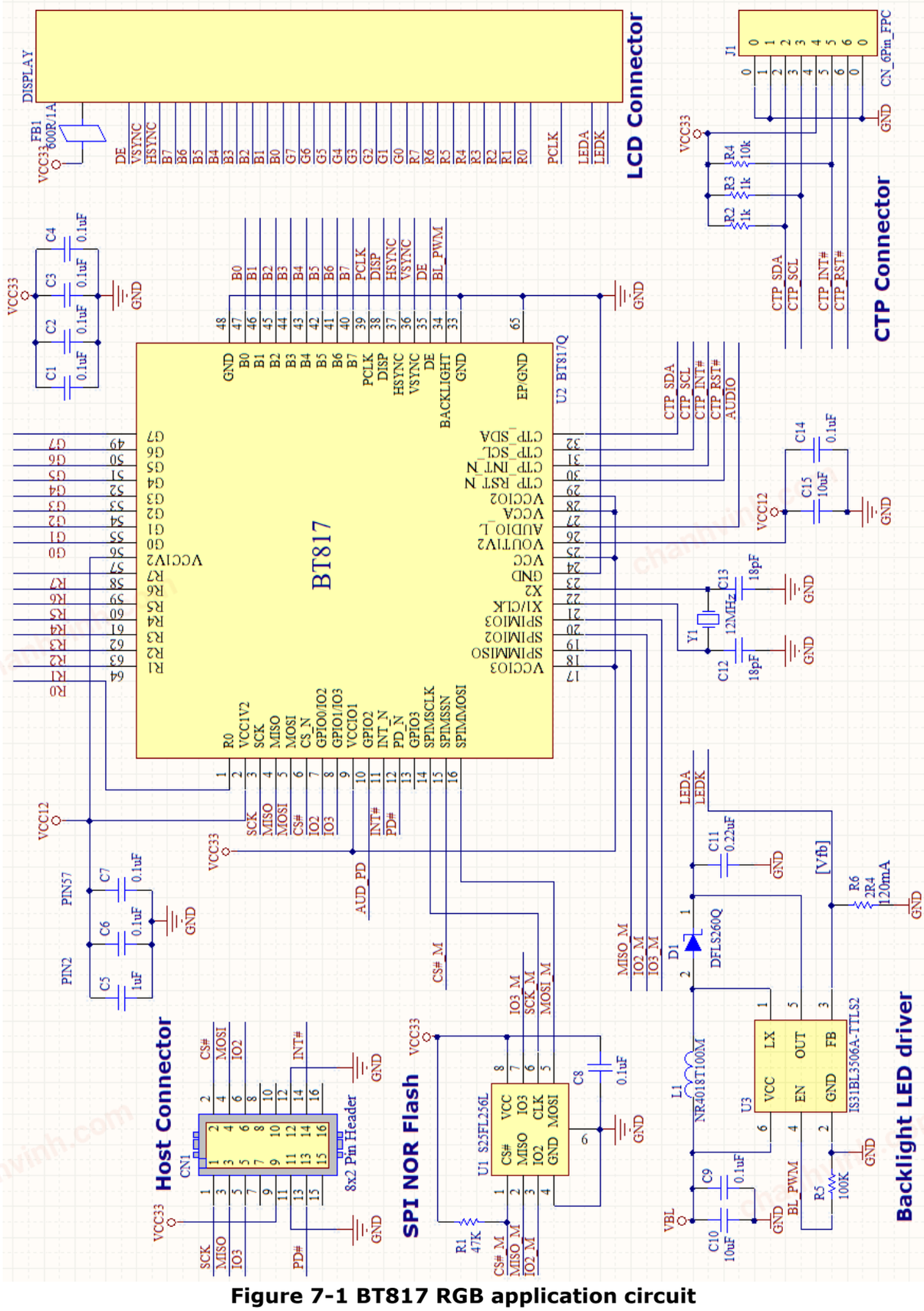



Figure 7-1 BT817 RGB application circuit

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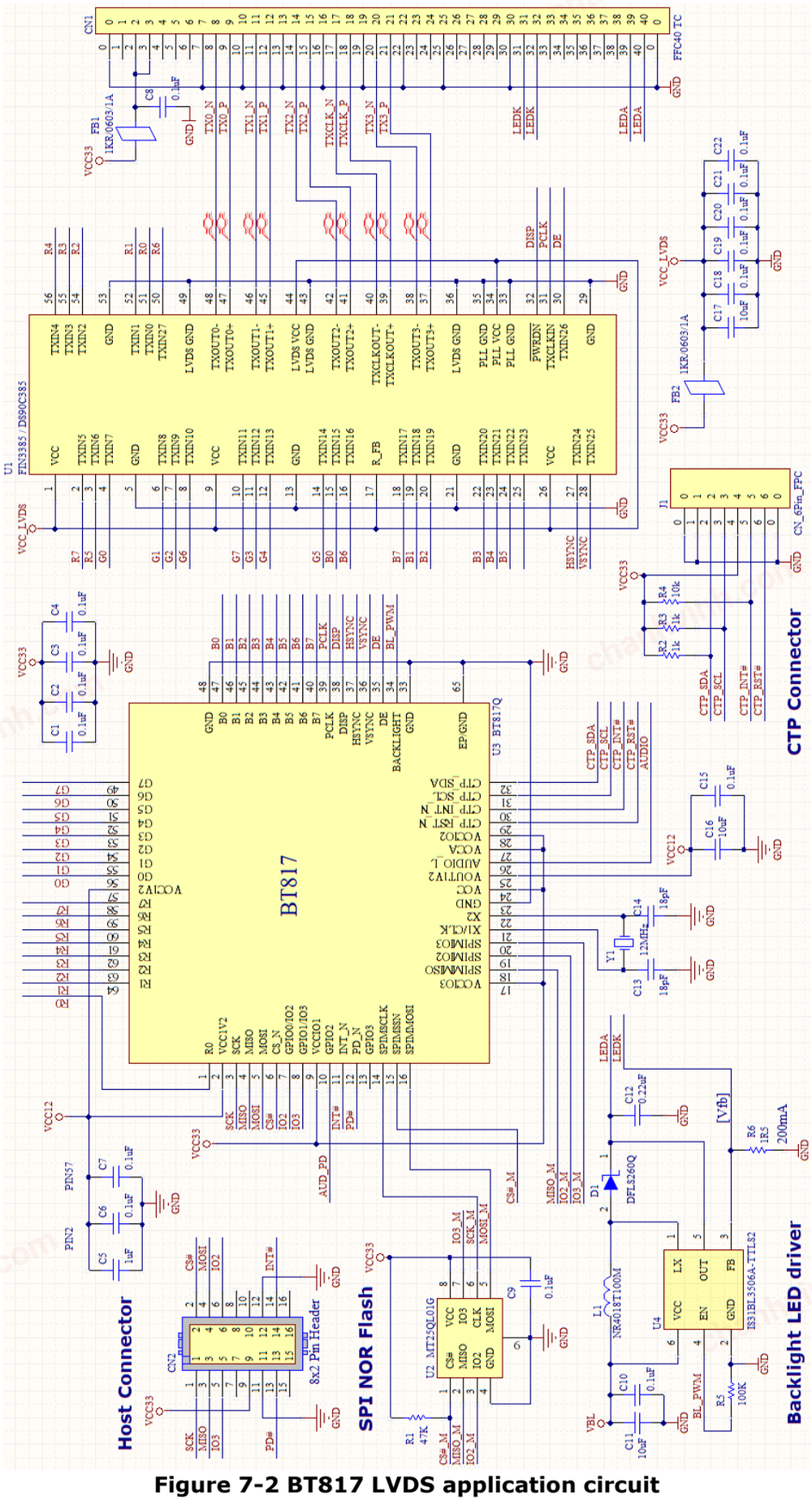



**Figure 7-2 BT817 LVDS application circuit**

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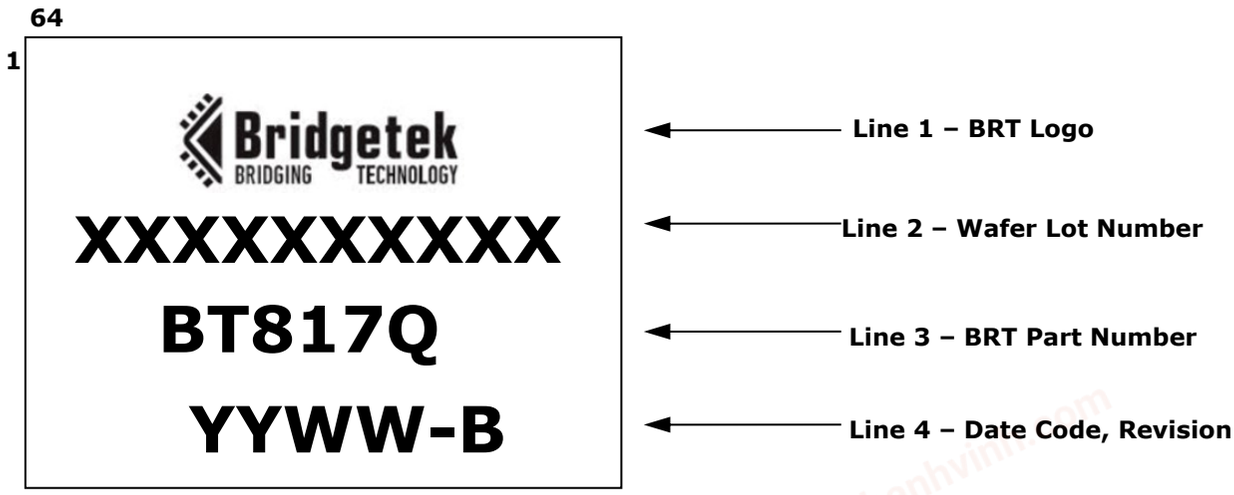


# 8 Package Parameters

The BT817/8 is available in VQFN-64 package. The package dimensions, markings and solder reflow profile for all packages are described in following sections.

## 8.1 Part Markings

### 8.1.1 Top Side




**Notes:**

1. YYWW = Date Code, where YY is year and WW is week number
2. BRT part number will be either BT817Q or BT818Q as per device selected.

### 8.1.2 Bottom Side

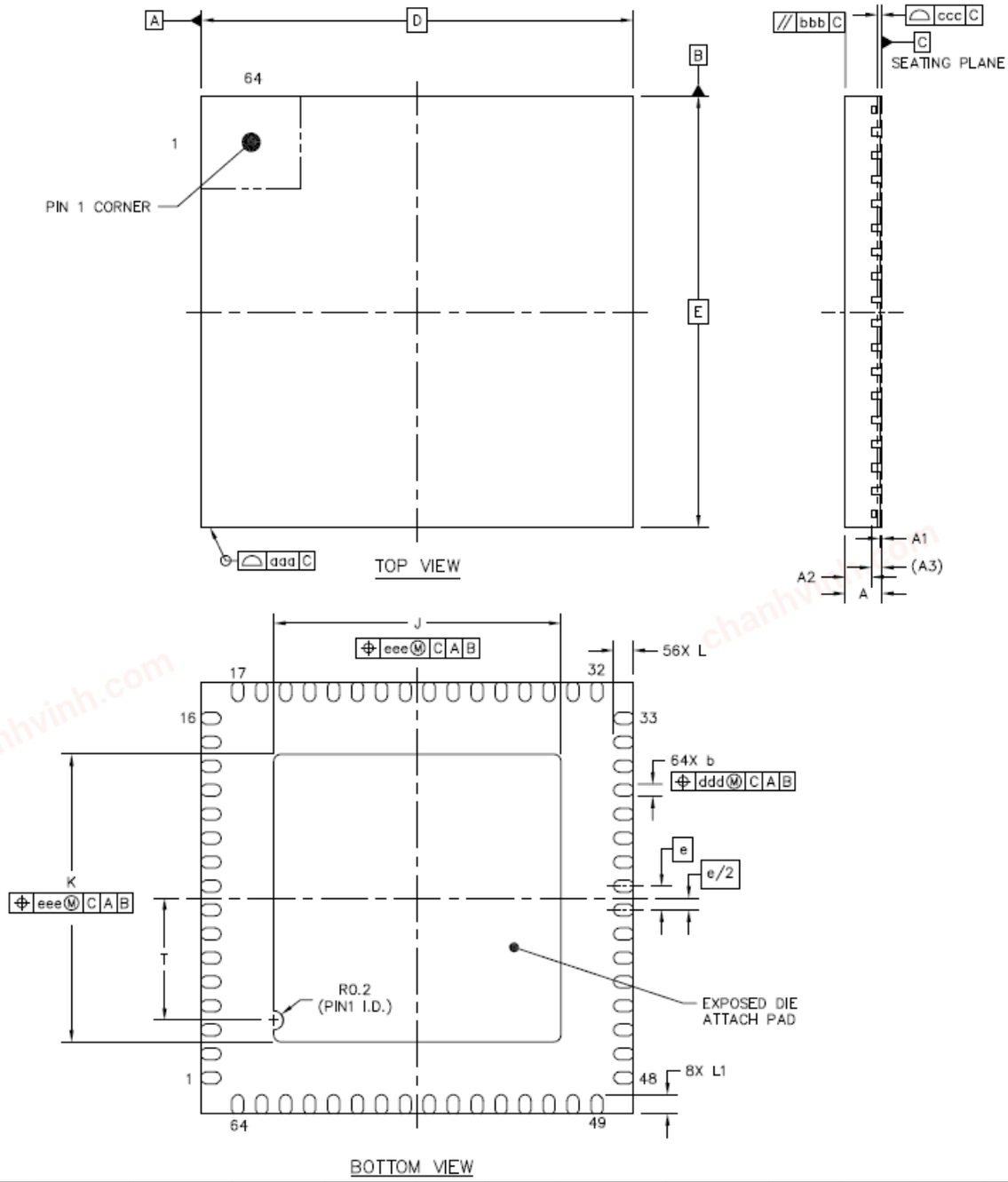
No markings should be placed on the bottom side.

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## 8.2 VQFN-64 Package Dimensions




| | A | A1 | A3 | b | D | E | J | K | e | L | L1 | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MIN. | 0.7 | 0.00 | | 0.2 | | | 5.9 | 5.9 | | 0.35 | 0.3 | 2.45 |
| NOM. | 0.75 | 0.035 | 0.203 | 0.25 | 9 | 9 | 6 | 6 | 0.50 | 0.4 | 0.4 | 2.55 |
| MAX. | 0.8 | 0.05 | | 0.3 | | | 6.1 | 6.1 | | 0.45 | 0.45 | 2.65 |

**Figure 8-1 VQFN-64 Package Dimensions**

All dimensions are in millimetres (mm). Tolerance aaa/bbb/ccc/ddd/eee: 0.1.

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## 8.3 Solder Reflow Profile

The recommended solder reflow profile for the package is shown in Figure 8-2.

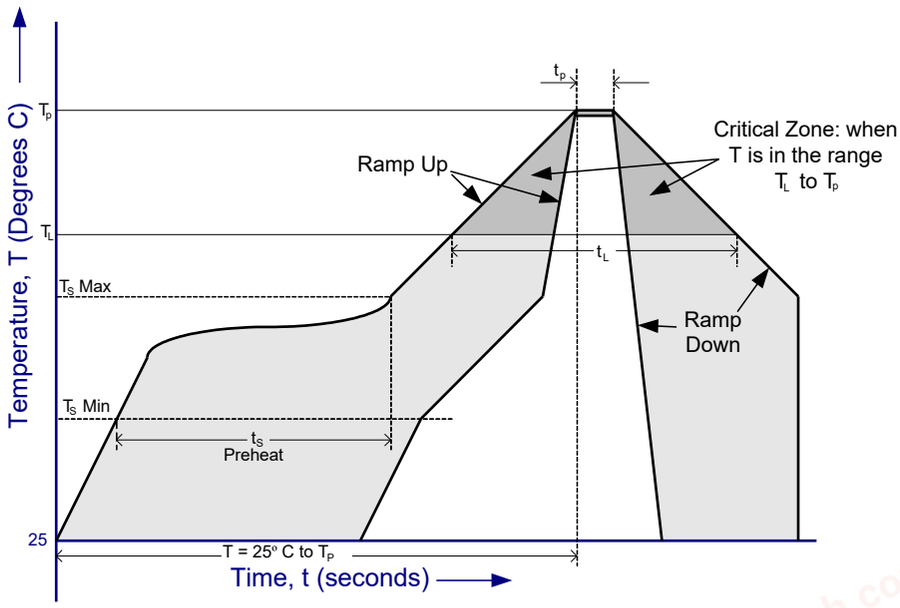



**Figure 8-2 BT817/8 Solder Reflow Profile**

The recommended values for the solder reflow profile are detailed in Figure 8-2. Values are shown for both a completely Pb free solder process (i.e. the BT817/8 is used with Pb free solder), and for a non-Pb free solder process (i.e. the BT817/8 is used with non-Pb free solder).

| Profile Feature | Pb Free Solder Process | Non-Pb Free Solder Process |
|---|---|---|
| Average Ramp Up Rate ($T_s$ to $T_p$) | 3°C / second Max. | 3°C / Second Max. |
| Preheat<br>- Temperature Min ($T_s$ Min.)<br>- Temperature Max ($T_s$ Max.)<br>- Time ($t_s$ Min to $t_s$ Max) | <br>150°C<br>200°C<br>60 to 120 seconds | <br>100°C<br>150°C<br>60 to 120 seconds |
| Time Maintained Above Critical Temperature $T_L$:<br>- Temperature ($T_L$)<br>- Time ($t_L$) | <br>217°C<br>60 to 150 seconds | <br>183°C 60 to 150 seconds |
| Peak Temperature ($T_p$) | 260°C | 240°C |
| Time within 5°C of actual Peak Temperature ($t_p$) | 20 to 40 seconds | 20 to 40 seconds |
| Ramp Down Rate | 6°C / second Max. | 6°C / second Max. |
| Time for T= 25°C to Peak Temperature, $T_p$ | 8 minutes Max. | 6 minutes Max. |

**Table 8-1 Reflow Profile Parameter Values**

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# 9 Contact Information

Refer to https://brtchip.com/contact-us/ for contact information.

**Distributor and Sales Representatives**

Please visit the Sales Network page of the Bridgetek Web site for the contact details of our distributor(s) and sales representative(s) in your country.

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# Appendix A – References

## Document References

BT81X_Series_Programming_Guide

AN_252 FT800 Audio Primer

AN_254 FT800 Designs with Visual TFT

AN_259 FT800 Example with 8-bit MCU

AN_275 FT800 Example with Arduino

AN_276 Audio File Conversion

AN_277 FT800 Create User Defined Font

AN_281 FT800 Emulator Library User Guide

AN_291 FT800 Create Multi-Language Font

AN_303 - FT800 Image File Conversion

AN_308 FT800 Example with an 8-bit MCU

AN_312 FT800 Example with ARM

AN_314 FT800 Advanced Techniques - Working with Bitmaps

AN_318 Arduino Library for FT800 Series

AN_320 FT800 Example with PIC

AN_327 EVE Screen Editor Installation Guide

AN_336 FT8xx - Selecting an LCD Display

FT800 Series Sample Application

EVE Frequently Asked Questions

## Acronyms and Abbreviations

| Terms | Description |
|---|---|
| ADPCM | Adaptive Differential Pulse Code Modulation |
| ASCII | American Standard Code for Information Interchange |
| ASTC | Adaptive Scalable Texture Compression |
| CTPM | Capacitive Touch Panel Module |
| CTSE | Capacitive Touch Screen Engine |
| EVE | Embedded Video Engine |
| HMI | Human Machine Interfaces |
| $I^2C$ | Inter-Integrated Circuit |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| MCU | Micro Controller Unit |
| MPU | Micro Processor Unit |
| PCM | Pulse Code Modulation |
| PLL | Phased Locked Loop |
| PWM | Pulse Width Modulation |

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| | |
|---|---|
| WVGA | Wide Video Graphics Array |
| ROM | Read Only Memory |
| SPI | Serial Peripheral Interface |
| VQFN | Very Thin Quad Flat Non-Leaded Package |

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# Appendix B - List of Figures and Tables

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# Appendix C - Revision History

Document Title: BT817/8 Advanced Embedded Video Engine Datasheet
Document Reference No.: BRT_000302
Clearance No.: BRT#154
Product Page: http://brtchip.com/product
Document Feedback: Send Feedback

| Revision | Changes | Date |
|---|---|---|
| Version 1.0 | Initial Release | 25-08-2020 |
| Version 1.1 | Updated related sections 4.1.5, 4.2.1, 4.2.3, 4.2.4, 4.9.4, 5.1 and 6.4.1 to remove internal clock functions | 17-09-2020 |
| Version 1.2 | Updated section "4.5 Parallel RGB Interface" to correct calculation and added note on page 27 about the HOFFSET and VOFFSET calculations<br>Updated REG_PCLK_POL definitions (section 4.5, 5.1, 6.4.3)<br>Update tape and reel qty to 2600 pcs per reel | 04-04-2022 |
| Version 1.3 | Updated the following –<br>IC Image on the cover page; BRT Logo line of the package marking; Company Address | 03-02-2025 |

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