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# 12-Bit Serial Input Multiplying D/A Converter

# DAC8043A

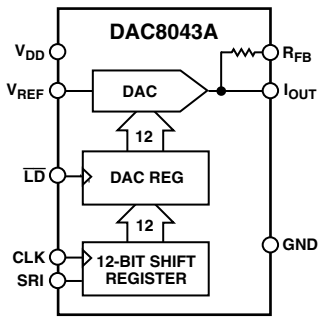
## FEATURES

**Compact SOIC, and TSSOP Packages**
**True 12-Bit Accuracy**
**5 V Operation @ <10 μA**
**Fast 3-Wire Serial Input**
**Fast 1 μs Settling Time**
**2.4 MHz 4-Quadrant Multiply BW**
**Pin-for-Pin Upgrade for DAC8043**
**Standard and Rotated Pinout**

## APPLICATIONS

**Ideal for PLC Applications in Industrial Control**
**Programmable Amplifiers and Attenuators**
**Digitally Controlled Calibration and Filters**
**Motion Control Systems**

## FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION

The DAC8043A is an improved high accuracy 12-bit multiplying digital-to-analog converter in space-saving 8-lead packages. Featuring serial input, double buffering and excellent analog performance, the DAC8043A is ideal for applications where PC board space is at a premium. Improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in/parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the D/A converter.

Consuming only 10 μA from a single 5 V power supply, the DAC8043A is the ideal low power, small size, high performance solution to many application problems.

The DAC8043A is specified over the extended industrial (–40°C to +85°C) temperature range. DAC8043A is available in a PDIP package, and the low profile 1.75 mm height SOIC-8 surface mount packages. The DAC8043AFRU is available for ultra-compact applications in a thin 1.1 mm TSSOP-8 package.

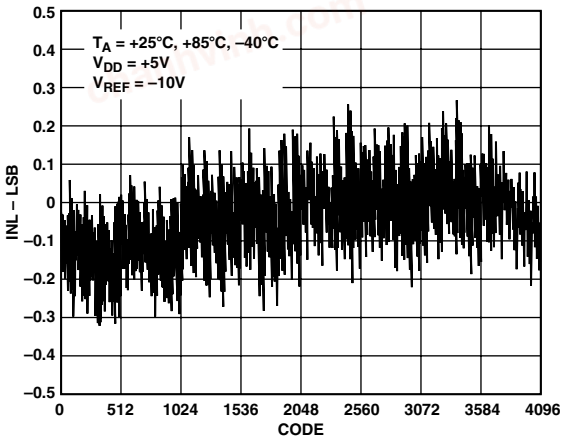



*Figure 1. Integral Nonlinearity Error vs. Code*

REV. B

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# DAC8043A–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_{DD}$ = 5 V, $V_{REF}$ = 10 V, –40°C < $T_A$ < +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | E Grade | F Grade | Unit |
|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | |
| Resolution | N | | 12 | 12 | Bits |
| Relative Accuracy | INL | | ±0.5 | ±1.0 | LSB max |
| Differential Nonlinearity | DNL | All Grades Monotonic to 12 Bits | ±0.5 | ±1.0 | LSB max |
| Gain Error[1] | $G_{FSE}$ | $T_A$ = 25°C, Data = $FFF_H$ | ±1.0 | ±2.0 | LSB max |
| | | $T_A$ = –40°C, +85°C, Data = $FFF_H$ | ±2.0 | ±2.0 | LSB max |
| Gain Tempco[2] | $TCG_{FS}$ | $I_{OUT}$ Pin Measured | ±5 | ±5 | ppm/°C max |
| Output Leakage Current | $I_{LKG}$ | Data = $000_H$, $I_{OUT}$ Pin Measured | ±5 | ±5 | nA max |
| | | $T_A$ = –40°C, +85°C, Data = $000_H$, $I_{OUT}$ Pin Measured | ±25 | ±25 | nA max |
| Zero-Scale Error[3] | $I_{ZSE}$ | Data = $000_H$ | 0.03 | 0.03 | LSB max |
| | | $T_A$ = –40°C, +85°C, Data = $000_H$ | 0.15 | 0.15 | LSB max |
| REFERENCE INPUT | | | | | |
| Input Resistance | $R_{REF}$ | Absolute Tempco < 50 ppm/°C | 7/15 | 7/15 | kΩ min/max |
| Input Capacitance[2] | $C_{REF}$ | | 5 | 5 | pF typ |
| ANALOG OUTPUT | | | | | |
| Output Capacitance[2] | $C_{OUT}$ | Data = $000_H$ | 25 | 25 | pF typ |
| | | Data = $FFF_H$ | 30 | 30 | pF typ |
| DIGITAL INPUTS | | | | | |
| Digital Input Low | $V_{IL}$ | | 0.8 | 0.8 | V max |
| Digital Input High | $V_{IH}$ | | 2.4 | 2.4 | V min |
| Input Leakage Current | $I_{IL}$ | $V_{LOGIC}$ = 0 V to 5 V | 0.001/±1 | 0.001/±1 | µA typ/max |
| Input Capacitance[2] | $C_{IL}$ | $V_{LOGIC}$ = 0 V | 10 | 10 | pF max |
| INTERFACE TIMING[2, 4] | | | | | |
| Data Setup | $t_{DS}$ | | 10 | 10 | ns min |
| Data Hold | $t_{DH}$ | | 5 | 5 | ns min |
| Clock Width High | $t_{CH}$ | | 25 | 25 | ns min |
| Clock Width Low | $t_{CL}$ | | 25 | 25 | ns min |
| Load Pulsewidth | $t_{LD}$ | | 25 | 25 | ns min |
| LSB CLK to $\overline{LD}$ DAC | $t_{ASB}$ | | 0 | 0 | ns min |
| AC CHARACTERISTICS[1, 2] | | | | | |
| Output Current Settling Time | $t_S$ | To ±0.01% of Full Scale, Ext Op Amp OP42 | 1 | 1 | µs max |
| DAC Glitch | Q | Data = $000_H$ to $FFF_H$ to $000_H$, $V_{REF}$ = 0 V | 20 | 20 | nVs max |
| Feedthrough ($V_{OUT}/V_{REF}$) | FT | $V_{REF}$ = 20 V p-p, Data = $000_H$, f = 10 kHz | 1 | 1 | mV p-p |
| Total Harmonic Distortion | THD | $V_{REF}$ = 6 V rms, Data = $FFF_H$, f = 1 kHz | –85 | –85 | dB typ |
| Output Noise Density[5] | $e_n$ | 10 Hz to 100 kHz Between $R_{FB}$ and $I_{OUT}$ | 17 | 17 | nV/√Hz max |
| Multiplying Bandwidth | BW | –3 dB, $V_{OUT}/V_{REF}$, $V_{REF}$ = 100 mV rms, Data = $FFF_H$ | 2.4 | 2.4 | MHz typ |
| SUPPLY CHARACTERISTICS | | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 4.5/5.5 | 4.5/5.5 | V min/max |
| Positive Supply Current | $I_{DD}$ | $V_{LOGIC}$ = 0 V or $V_{DD}$ | 10 | 10 | µA max |
| Power Dissipation | $P_{DISS}$ | $V_{LOGIC}$ = 0 V or $V_{DD}$ | 50 | 50 | µW max |
| Power Supply Sensitivity | PSS | $\Delta V_{DD}$ = ±5% | 0.002 | 0.002 | %/% max |

NOTES

[1]Using internal feedback resistor $R_{FB}$, see Figure 19 test circuit with $V_{REF}$ = 10 V.

[2]These parameters are guaranteed by design and not subject to production testing.

[3]Calculated from worst case $R_{REF}$: $I_{ZSE}(LSB) = (R_{REF} \times I_{LKG} \times 4096)/V_{REF}$.

[4]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[5]Calculation from $e_n = \sqrt{4KTRB}$ where: K = Boltzmann Constant (J/°K), R = Resistance (Ω), T = Resistor Temperature (°K), B = 1 Hz Bandwidth.

Specifications subject to change without notice.

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## ABSOLUTE MAXIMUM RATINGS*

$V_{DD}$ to GND ..... –0.3 V, +8 V
$V_{REF}$ to GND ..... ±18 V
$R_{FB}$ to GND ..... ±18 V
Logic Inputs to GND ..... –0.3 V, $V_{DD}$ + 0.3 V
$VI_{OUT}$ to GND ..... –0.3 V, $V_{DD}$ + 0.3 V
$I_{OUT}$ Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance $\theta_{JA}$
8-Lead PDIP Package (N-8) ..... 103°C/W
8-Lead SOIC Package (R-8) ..... 158°C/W
8-Lead TSSOP Package (RU-8) ..... 240°C/W
Maximum Junction Temperature ($T_J$ max) ..... 150°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

| Model[1] | INL (LSB) | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|
| DAC8043A1ES[2] | ±0.5 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043A1ESZ[2, 3] | ±0.5 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043A1FS[2] | ±1.0 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043A1FSZ[2, 3] | ±1.0 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043AEP | ±0.5 | –40°C to +85°C | 8-Lead PDIP | N-8 |
| DAC8043AEPZ[3] | ±0.5 | –40°C to +85°C | 8-Lead PDIP | N-8 |
| DAC8043AES | ±0.5 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043AESZ[3] | ±0.5 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043AFP | ±1.0 | –40°C to +85°C | 8-Lead PDIP | N-8 |
| DAC8043AFPZ[3] | ±1.0 | –40°C to +85°C | 8-Lead PDIP | N-8 |
| DAC8043AFRU | ±1.0 | –40°C to +85°C | 8-Lead TSSOP | RU-8 |
| DAC8043AFRU-REEL | ±1.0 | –40°C to +85°C | 8-Lead TSSOP | RU-8 |
| DAC8043AFRU-REEL7 | ±1.0 | –40°C to +85°C | 8-Lead TSSOP | RU-8 |
| DAC8043AFRUZ[3] | ±1.0 | –40°C to +85°C | 8-Lead TSSOP | RU-8 |
| DAC8043AFRUZ-REEL7[3] | ±1.0 | –40°C to +85°C | 8-Lead TSSOP | RU-8 |
| DAC8043AFS | ±1.0 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043AFS-REEL7 | ±1.0 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043AFSZ[3] | ±1.0 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |
| DAC8043AFSZ-REEL[3] | ±1.0 | –40°C to +85°C | 8-Lead SOIC_N | R-8 |

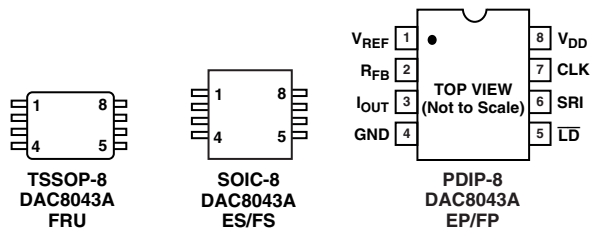
[1]The DAC8043A contains 346 transistors. The die size measures 70.3 mm × 57.1 mm = 4014 square mm.
[2]The DAC8043A1ES, DAC8043A1ESZ, DAC8043A1FS, and DAC8043A1FSZ have a rotated pinout.
[3]Z = Pb-free part.

## PIN FUNCTION DESCRIPTIONS

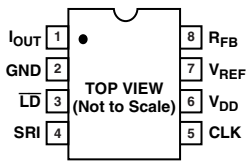
| #(*) | Name | Function |
|---|---|---|
| 1(7) | $V_{REF}$ | DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance versus code. |
| 2 (8) | $R_{FB}$ | Internal Matching Feedback Resistor. Connect to external op amp output. |
| 3 (1) | $I_{OUT}$ | DAC Current Output, full-scale output 1 LSB less than reference input voltage $-V_{REF}$. |
| 4 (2) | GND | Analog and Digital Ground. |
| 5 (3) | $\overline{LD}$ | Load Strobe, Level-Sensitive Digital Input. Transfers shift-register data to DAC register while active low. See truth table for operation. |
| 6 (4) | SRI | 12-Bit Serial Register Input, data loads directly into the shift register MSB first. Extra leading bits are ignored. |
| 7 (5) | CLK | Clock Input, positive-edge clocks data into shift register. |
| 8 (6) | $V_{DD}$ | Positive Power Supply Input. Specified range of operation 5 V ± 10%. |

*Note Pin numbers in parenthesis represent the rotated pinout of the DAC8043A1ES and DAC8043A1FS models.

## DAC8043AE/F PIN CONFIGURATIONS




## DAC8043A1E AND DAC8043A1F PIN CONFIGURATION (Rotated Pinout)




## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8043A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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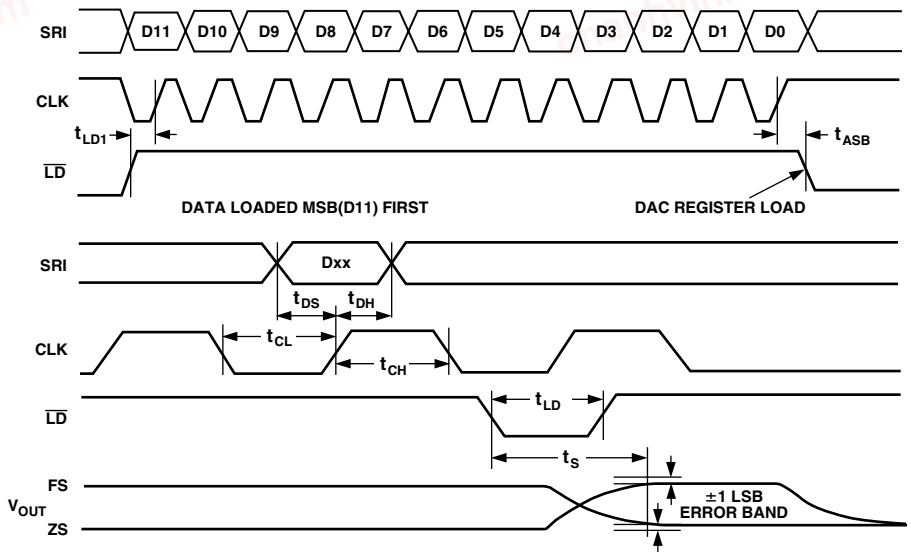



*Figure 2. Timing Diagram*

**Table I. Control-Logic Truth Table**

| CLK | $\overline{LD}$ | Serial Shift Register Function | DAC Register Function |
|---|---|---|---|
| ↑ | H | Shift-Register-Data Advanced One Bit | Latched |
| H or L | L | No Effect | Updated with Current Shift Register Contents |
| L | ↑ | No Effect | Latched All 12 Bits |

NOTES
↑ positive logic transition.
The DAC Register $\overline{LD}$ input is level-sensitive. Any time $\overline{LD}$ is logic-low data in the serial register will directly control the switches in the R-2R DAC ladder.

## Typical Performance Characteristics

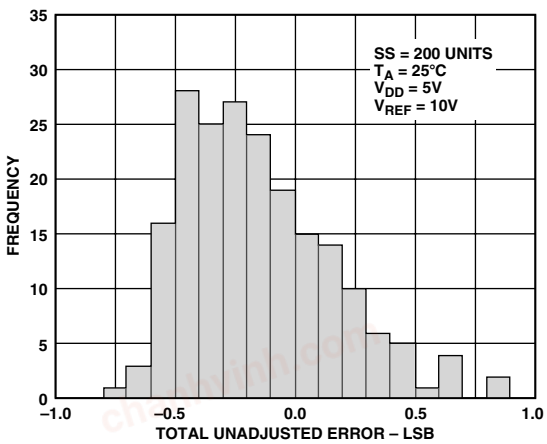



*Figure 3. Total Unadjusted Error Histogram*

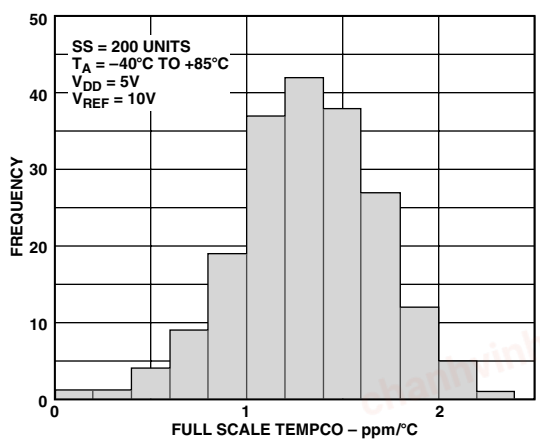



*Figure 4. Full-Scale Output Tempco Histogram*

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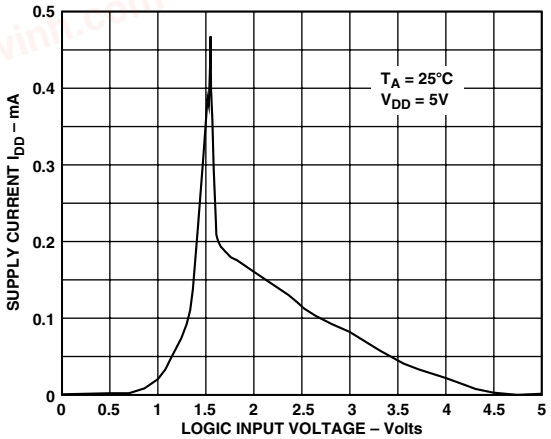



Figure 5. Supply Current vs. Logic Input Voltage

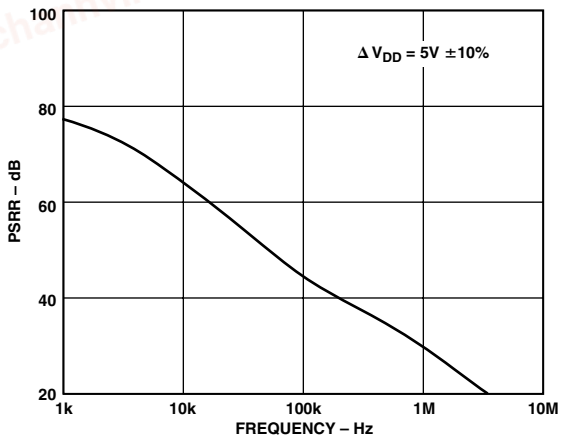



Figure 8. Power Supply Rejection vs. Frequency

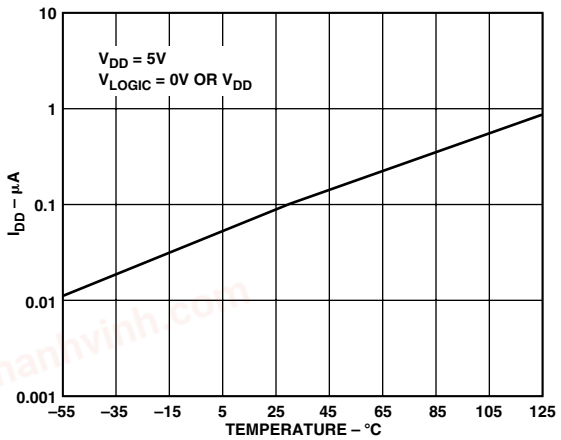



Figure 6. Supply Current vs. Temperature

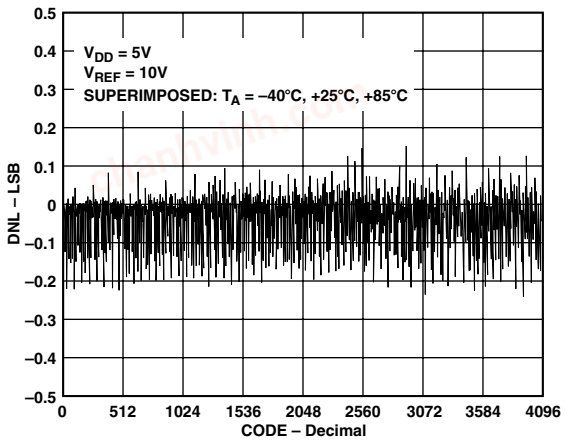



Figure 9. Linearity Error vs. Digital Code

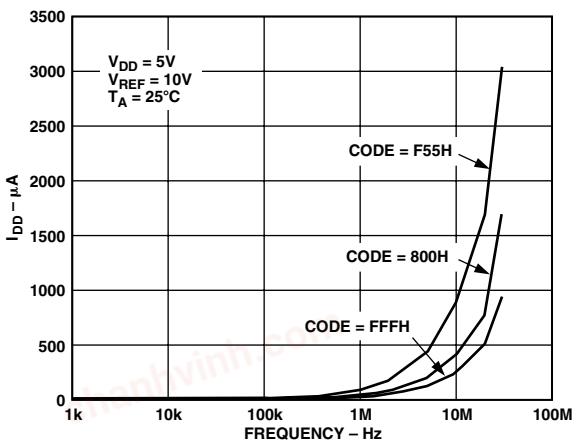



Figure 7. Supply Current vs. Clock Frequency

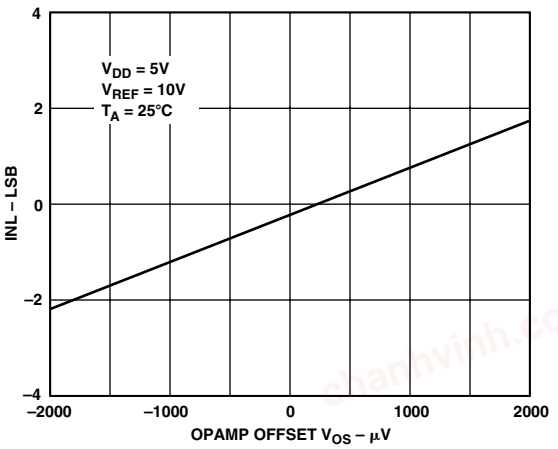



Figure 10. Linearity Error vs. External Op Amp $V_{OS}$

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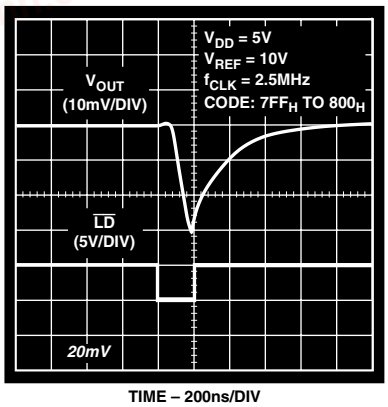



Figure 11. Midscale Transition Performance

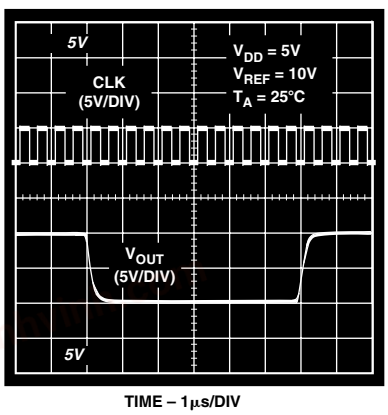



Figure 12. Large Signal Settling Time

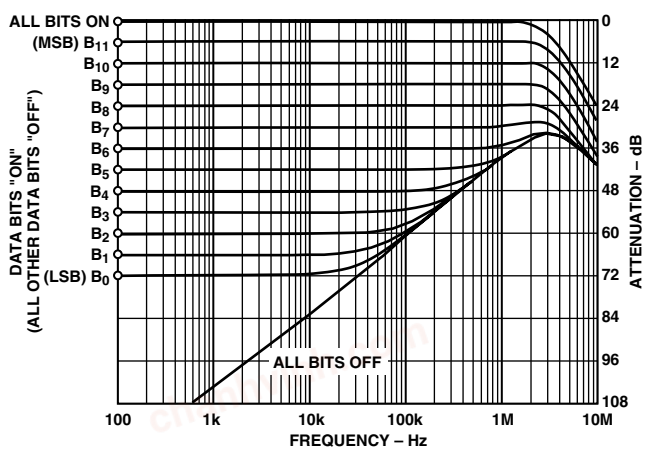



Figure 13. Reference Multiplying Bandwidth vs. Frequency and Code

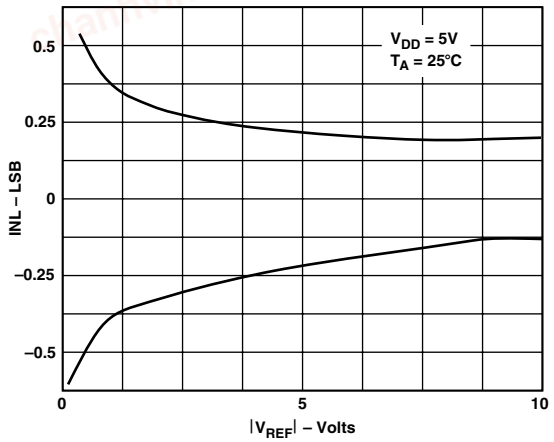



Figure 14. Linearity Error vs. Reference Voltage

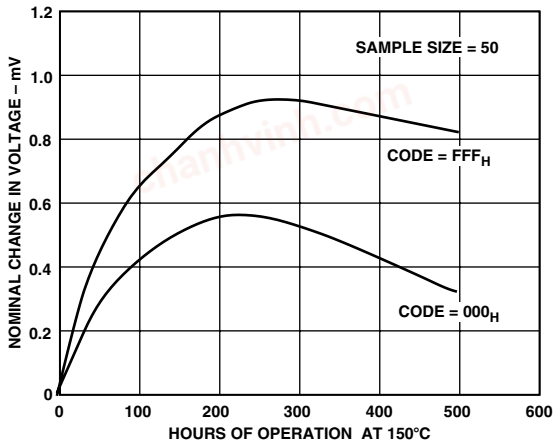



Figure 15. Long-Term Drift Accelerated by Burn-In

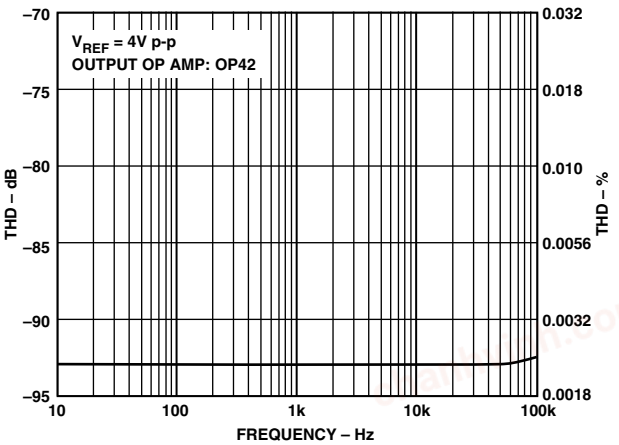



Figure 16. THD vs. Frequency

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## PARAMETER DEFINITIONS

### INTEGRAL NONLINEARITY (INL)

This is the single most important DAC specification. ADI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed as a percent of full-scale range or in terms of LSBs. Refer to Analog Devices Data Reference Manual for additional digital-to-analog converter definitions.

### INTERFACE LOGIC INFORMATION

The DAC8043A has been designed for ease of operation. The timing diagram, Figure 2, illustrates the input register loading sequence. Note that the most significant bit (MSB) is loaded first. Once the 12-bit input register is full, the data is transferred to the DAC register by taking $\overline{LD}$ momentarily low.

### DIGITAL SECTION

The DAC8043A's digital inputs, SRI, $\overline{LD}$, and CLK, are TTL compatible. The input voltage levels affect the amount of current drawn from the supply; peak supply current occurs as the digital input (VIN) passes through the transition region. See the Supply Current vs. Logic Input Voltage graph located in the typical performance characteristics curves. Maintaining the digital input voltage levels as close as possible to the supplies, VDD and GND, minimizes supply current consumption. The DAC8043A's digital inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry. Figure 17 shows the input protection diodes and series resistor; this input structure is duplicated on each digital input. High voltage static charges applied to the inputs are shunted to the supply and ground rails through forward biased diodes. These protection diodes were designed to clamp the inputs to well below dangerous levels during static discharge conditions.

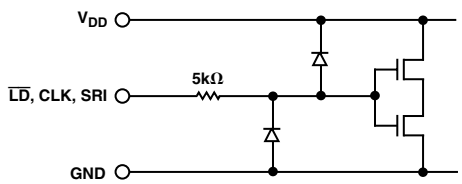



*Figure 17. Digital Input Protection*

### GENERAL CIRCUIT INFORMATION

The DAC8043A is a 12-bit multiplying D/A converter with a very low temperature coefficient. It contains an R-2R resistor ladder network, data input and control logic, and two data registers.

The digital circuitry forms an interface in which serial data can be loaded under microprocessor control into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

The analog portion of the DAC8043A contains an inverted R-2R ladder network consisting of silicon-chrome, highly-stable (50 ppm/°C) thin-film resistors, and twelve pairs of NMOS current-steering switches, see Figure 18. These switches steer binarily weighted currents into either $I_{OUT}$ or GND; this yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at $V_{REF}$ equal to R. The $V_{REF}$ input may be driven by any reference voltage or current, ac or dc that is within the limits stated in the Absolute Maximum Ratings.

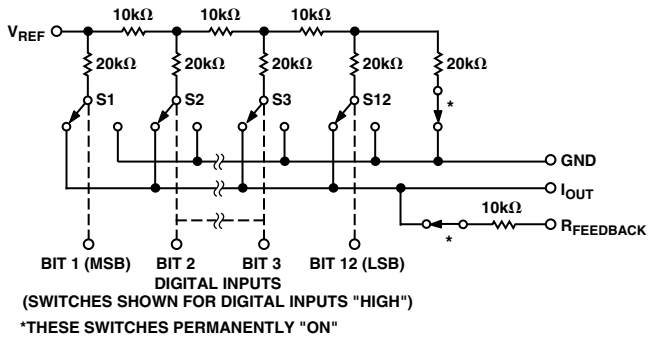



*Figure 18. Simplified DAC Circuit*

The twelve output current steering NMOS FET switches are in series with each R-2R resistor.

To further ensure accuracy across the full temperature range, permanently "ON" MOS switches were included in series with the feedback resistor and the R-2R ladder's terminating resistor. Figure 18 shows the location of the series switches. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), $V_{DD}$ must be present to turn "ON" these series switches.

## DYNAMIC PERFORMANCE

### OUTPUT IMPEDANCE

The DAC8043A's output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the $I_{OUT}$ terminal, may be between 10 kΩ (the feedback resistor alone when all digital inputs are LOW) and 7.5 kΩ (the feedback resistor in parallel with approximate 30 kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations.

### APPLICATIONS INFORMATION

In most applications, linearity depends upon the potential of the $I_{OUT}$ and GND pins being at the same voltage potential. The DAC is connected to an external precision op amp inverting input. The external amplifiers noninverting input should be tied directly to ground without the usual bias current compensating resistor. (See Figures 19 and 20.) The selected amplifier should have a low input bias current and low drift over temperature. The amplifiers input offset voltage should be nulled to less than 200 microvolts (less than 10% of 1 LSB). All grounded pins should tie to a single common ground point to avoid ground loops. The $V_{DD}$ power supply should have a low noise level with adequate bypassing. It is best to operate the DAC8043A from the analog power supply and grounds.

### UNIPOLAR 2-QUADRANT MULTIPLYING

The most straightforward application of the DAC8043A is in the 2-quadrant multiplying configuration shown in Figure 19. If the reference input signal is replaced with a fixed dc voltage

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reference, the DAC output will provide a proportional dc voltage output according to the transfer equation:

$$V_{OUT} = -D/4096 \times V_{REF}$$

where $D$ is the decimal data loaded into the DAC register and $V_{REF}$ is the externally applied reference voltage source.

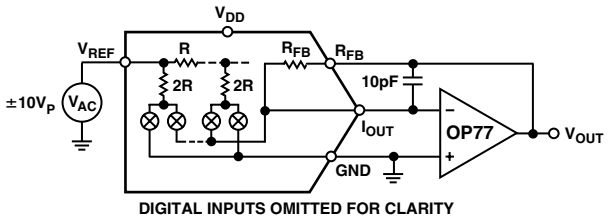



*Figure 19. Unipolar (2-Quadrant) Operation*

## BIPOLAR 4-QUADRANT MULTIPLYING

Figure 20 shows a suggested circuit to achieve 4-quadrant multiplying operation. The summing amplifier multiplies $V_{OUT1}$ by 2, and offsets the output with the reference voltage so that a midscale digital input code of 2048 places $V_{OUT2}$ at zero volts. The negative full-scale voltage will be $V_{REF}$ when the DAC is loaded with all zeros. The positive full-scale output will be $-(V_{REF} - 1\ LSB)$ when the DAC is loaded with all ones. Thus the digital coding is offset binary. The voltage output transfer equation for various input data and reference (or signal) values follows:

$$V_{OUT2} = (D/2048 - 1) \times -V_{REF}$$

where $D$ is the decimal data loaded into the DAC register and $V_{REF}$ is the externally applied reference voltage source.

Precision resistors will be necessary to avoid ratio errors. Otherwise trimming will be required to achieve full accuracy specifications available from the DAC8043A device. See the various Analog Devices Digital Potentiometer products for automated trimming solutions (e.g., the AD5204 for low voltage applications or the AD7376 for high voltage applications).

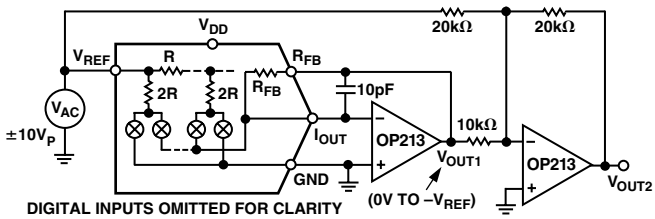


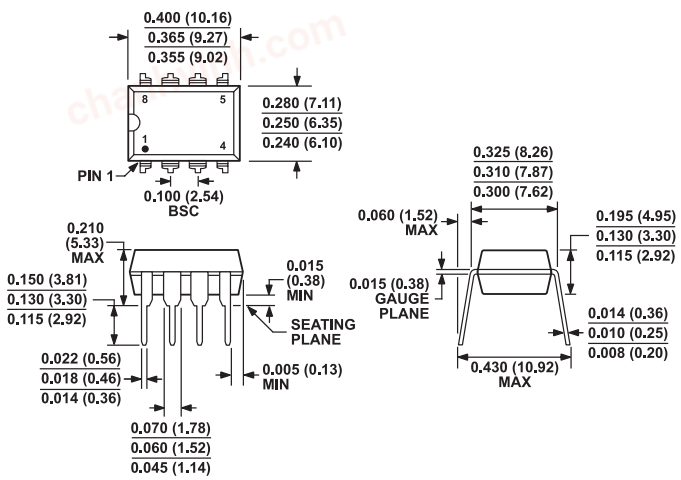

*Figure 20. Bipolar (4-Quadrant) Operation*

C00272–0–4/06 (B)

## OUTLINE DIMENSIONS

### 8-Lead Plastic Dual In-Line Package [PDIP]
### (N-8)

Dimensions shown in inches and (millimeters).

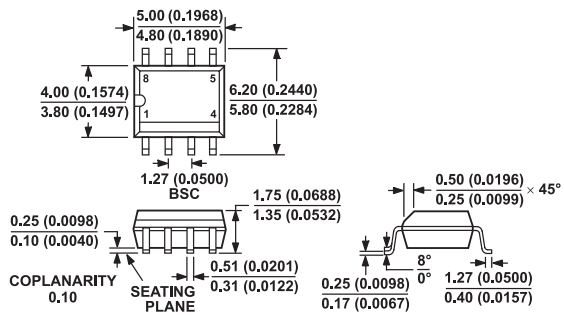



COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

### 8-Lead Standard Small Outline Package [SOIC_N]
### (R-8)
### S-Suffix

Dimensions shown in millimeters and (inches).

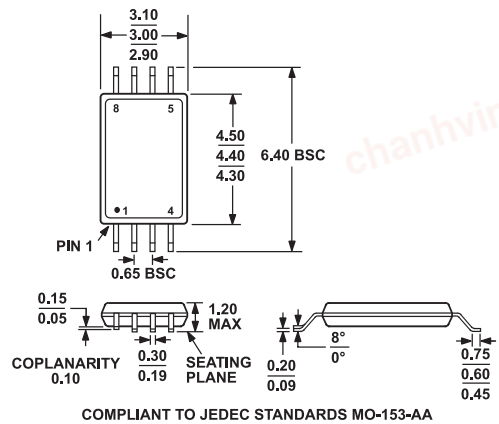



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

### 8-Lead Thin Shrink Small Outline Package [TSSOP]
### (RU-8)

Dimensions shown in millimeters.




COMPLIANT TO JEDEC STANDARDS MO-153-AA