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TMD3719

ALS/Color and Proximity Sensor

General Description

The TMD3719 features ambient light and color (RGB) sensing, flicker detection and proximity detection. The device integrates three IR VCSELs and an advanced VCSEL driver within a low-profile 6.35mm x 3.00mm x 1.00mm package.

The ambient light and color sensing function provides six concurrent ambient light sensing channels: Red, Green, Blue, Clear, Leakage and Wideband. The RGBL and Clear channels have a UV/IR blocking filter. This architecture accurately measures ambient light and enables the calculation of illuminance, chromaticity, and color temperature to manage display appearance.

The device integrates direct detection of ambient light flicker for 4 selectable frequency bins. Flicker detection is executed in parallel with ambient light and color sensing. The flicker detection engine can also buffer data for calculating other flicker frequencies externally.

The proximity function synchronizes IR emission and detection to sense nearby objects. The architecture of the engine features self-maximizing dynamic range, ambient light subtraction, advanced crosstalk cancelation, and interrupt-driven I^2C communication. Sensitivity, power consumption, and noise can be optimized with adjustable IR VCSEL timing and power. The proximity engine recognizes detect/release events and produces a configurable interrupt whenever the proximity result crosses upper or lower threshold settings.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD3719 are listed below:

Figure 1:
Added Value of Using TMD3719

Benefits	Features
• Improved Lux Accuracy for ALS Behind OLED	• High Sensitivity • Leakage Channel
• Minimized Display Distortion for Proximity Behind OLED	• Proximity Function Synchronized with Display • Multiple VCSEL Emitters to Lower the Optical Power Density

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Applications

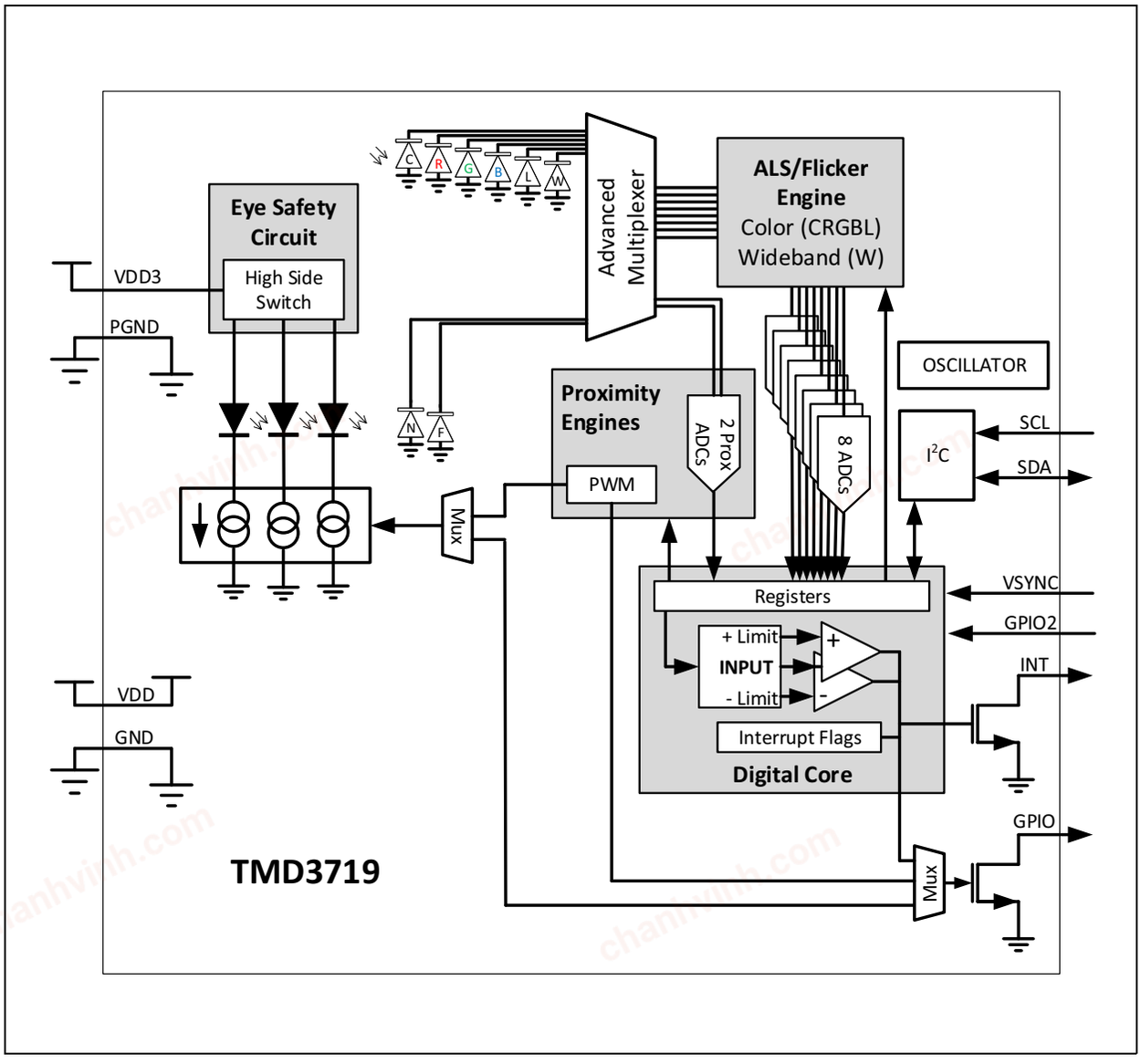
TMD3719 integrates multiple applications within one device. The applications for TMD3719 include:

- Brightness management for displays
- Color management for displays
- Camera image processing
- Flicker-immune camera operation
- Touch screen disable

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD3719



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Pin Assignments

Device pinout is described below.

Figure 3:
Pin Diagram of TMD3719

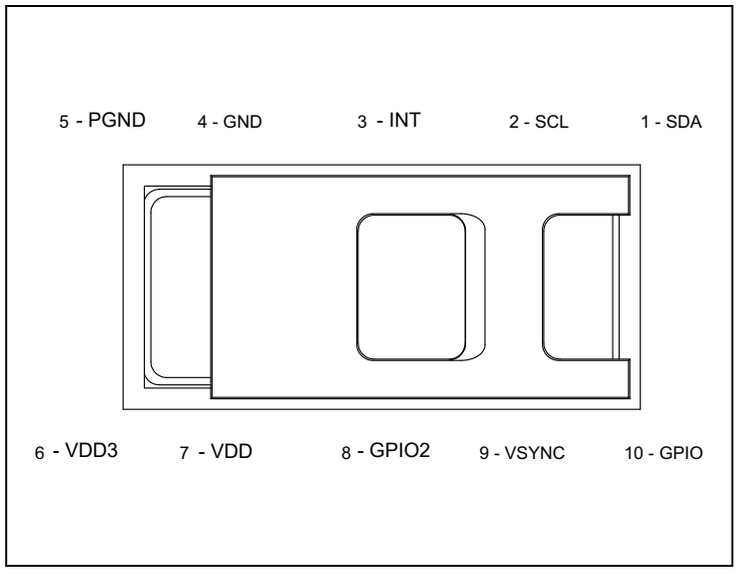

Figure 4:
Pin Description of TMD3719

Pin Number	Pin Name	Description
1	SDA	I^2C serial data I/O terminal
2	SCL	I^2C serial clock terminal
3	INT	Interrupt. Open-drain output plus supports additional output options.
4	GND	Ground. All voltages are referenced to GND/PGND, and both ground pins must be connected to ground.
5	PGND	Ground. All voltages are referenced to GND/PGND, and both ground pins must be connected to ground.
6	VDD3	Supply voltage (3.3V)
7	VDD	Supply voltage (1.8V)
8	GPIO2	General purpose input
9	VSYNC	VSYNC input
10	GPIO	Open-drain general purpose input/output

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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages with respect to GND/PGND. Device parameters are guaranteed at V_{DD} = 1.8 V and T_A = 25°C unless otherwise noted.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	Supply Voltage to GND	-0.3	1.98	V	
V_{DD3}	Emitter Supply Voltage to GND	-0.3	3.6		
V_{IO}	Digital I/O Terminal Voltage	-0.3	3.6		
I_{IO}	Digital Output Terminal Current	-1	20	mA	
I_{SINK}	VCSEL Current (1)	0	10		The VCSEL current setting should not exceed 10mA for any of the VCSELs to maintain Class 1 laser safety.
Electrostatic Discharge					
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78D
ESD_{HBM}	HBM Electrostatic Discharge	±2000		V	JEDEC/ESDA JS-001-2017
ESD_{CDM}	CDM Electrostatic Discharge	± 500		V	JEDEC JESD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_A	Operating Temperature Range (2)	-30	85		

Note(s):

1. This ensures the maximum optical power is <12mW at 940nm ±10nm.
2. While the device is operational across the temperature range, functionality will vary with temperature.

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Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply Voltage	1.7	1.8	1.98	V
V_{DD3}	Emitter Supply Voltage	2.9	3.3	3.6	V
I_{SINK}	VCSEL Current	10	10	10	mA

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Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Electrical Characteristics of TMD3719, V_{DD} = 1.8V, V_{DD3} =3.3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (1)	Active ALS State (2) (PON=AEN=1, WEN=PEN=0)		380	460	µA
		Active Proximity State (PON=PEN=1, AEN=0)		600	700	
		Idle State (3) (PON=1, AEN=PEN=0)		125	150	
		Sleep State (4) (PON = 0)		0.7	5.0	
V_{OL}	INT, SDA, GPIO output low voltage	3mA sink current			0.36	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	µA
V_{IH}	SCL, SDA, VSYNC input high voltage		1.26			V
V_{IL}	SCL, SDA, VSYNC input low voltage				0.54	V
T_{WAKEUP}	Time from sleep state exit to proximity engine ready(5)		0.5			ms
T_{ACTIVE}	Time from power-on to ready for receiving I^2C commands(5)		1.5			ms

Note(s):

1. Values are shown at the VDD pin and do not include current through the VDD3 pin.
2. This parameter indicates the supply current during periods of ALS integration. The ALS gain setting will have an effect on the active supply current. The ALS gain setting for this parameter is 2x.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
5. Not production tested. Specified by design and characterization.

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Optical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed with V_{DD} = 1.8V, V_{DD3} = 3.3V and T_A = 25°C unless otherwise noted.

Figure 8:
ALS/Color Characteristics of TMD3719, ALS Gain = 512x, Integration Time = 10.8ms (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Dark ADC count value[1]	Ee = 0µW/cm^2 ALS gain: 4096x Integration time: 22ms	0	0	3	counts
ALS gain ratios	2x	0.0032	0.0041	0.0049	
	4x	0.0068	0.0083	0.0095	
	8x	0.0138	0.0164	0.0176	
	16x	0.0270	0.0317	0.0345	
	32x	0.050	0.061	0.067	
	64x	0.105	0.124	0.134	
	128x	0.217	0.249	0.267	
	256x	0.454	0.498	0.526	
	1024x	1.85	2.02	2.50	
	2048x	3.2	4.1	10.0	
	4096x	5.0	9.0	18.0	
Clear channel irradiance responsivity[1]	White LED, 3000K[2]	559	657	756	counts/ µW/cm^2
Wideband channel irradiance responsivity[1]			332		
Lux accuracy[3]	White LED, 3000K Integration time: 100ms	85	100	115	%
ADC noise[4]	White LED, 3000K ALS gain: 1024x Integration time: 355ms		0.025		%

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Parameter	Conditions	Min	Typ	Max	Unit
Red/Clear channel ratios	White LED, 3000K	52	62	72	%
	Blue LED, λ_D = 465nm[5]	1	7	13	
	Red LED, λ_D= 615nm[6]	80	97	113	
Green/Clear channel ratios	White LED, 3000K	21	31	41	
	Green LED, λ_D = 525nm[7]	63	76	88	
	Red LED, λ_D = 615nm	5	8	12	
Blue/Clear channel ratios	White LED, 3000K	7	18	30	
	Blue LED, λ_D = 465nm	74	88	103	
	Red LED, λ_D = 615nm	0	5	12	
Leakage/Clear channel ratio	White LED, 3000K	0	1	5	
Wideband/Clear channel ratio	White LED, 3000K	36	48	60	
Wideband/IR channel ratio	IR LED = 940nm[8]	7	13	18	

Note(s):

1. ALS output values (ADATAX) are divided by 4 to account for the output having 2 sub-LSBs.
2. The White LED is an InGaN light-emitting diode with integrated phosphor that has a correlated color temperature = 3000K.
3. Lux accuracy is an illuminance estimated using the red, green, blue, and clear channels and is not 100% production tested.
4. ADC noise is calculated as the standard deviation of 1000 data samples divided by full scale and is not 100% production.
5. The Blue LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 22nm.
6. The Red LED is an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 15nm.
7. The Green LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 35nm.
8. The IR LED is an AlGaAs light-emitting diode with the following characteristics: peak wavelength λP = 940nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 42nm.

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Figure 9:
Proximity Characteristics of TMD3719

Parameter	Conditions	Min	Typ	Max	Unit
Near Response, Relative Variation[1], [4]	PGAIN = 0 (1x) All 3 ISINKs set to 10mA[5] PPULSE_LEN = 4 (64µs) PPULSE = 2 (3pulses) d= 50mm round target 84mm target distance After electrical calibration	75	100	125	%
Far Response, Relative Variation[1], [4]	PGAIN = 0 (1x) All 3 ISINKs set to 10mA[5] PPULSE_LEN = 4 (64µs) PPULSE = 2 (3pulses) d= 50mm round target 84mm target distance After electrical calibration	80	100	120	%
Near/Far Ratio Response, Relative Variation[1]	PGAIN = 0 (1x) All 3 ISINKs set to 10mA[5] PPULSE_LEN = 4 (64µs) PPULSE = 2 (3pulses) d= 50mm round target 84mm target distance After electrical calibration	87.5	100	112.5	%
Near Response, Absolute[2]	PGAIN = 0 (1x) All 3 ISINKs set to 10mA[5] PPULSE_LEN = 3 (32µs) PPULSE = 0 (1pulse) POFFSET = 0 100mm x 100mm, 90% reflective Kodak gray card 100mm target distance	5338	7117	8897	counts
Far Response, Absolute[2]	PGAIN = 0 (1x) All 3 ISINKs set to 10mA[5] PPULSE_LEN = 3 (32µs) PPULSE = 0 (1pulse) POFFSET = 0 100mm x 100mm, 90% reflective Kodak gray card 100mm target distance	5419	6774	8129	counts

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Parameter	Conditions	Min	Typ	Max	Unit
Noise/Signal[3]	PGAIN = 0 (1x) All 3 ISINKs set to 10mA[5] PPULSE_LEN = 2 (16µs) PPULSE = 7 (8pulses) POFFSET = 0			2	%

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.
2. Representative result by characterization. This characterization result does not include the VCSEL output power drift over the life of the product.
3. Production tested result is the range of 10 readings divided by the average response.
4. Production test does not include the VCSEL output power drift over the life of the product. The VCSEL output power drift will stay within ±1dB of the initial output power for standard device operation using all 3 VCSELs.
5. Use ISINK_RELEASE = ISINK_DETECT = 3 (2x), ISINK0 = 4 (5mA) and ISINK1 =ISINK2 = 5 (5mA) to set all 3 VCSELs with 10mA drive current.

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Timing Characteristics

The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with V_{DD} = 1.8V, V_{DD3} = 3.3V and T_A = 25°C unless otherwise noted.

Figure 10:
I²C Timing Characteristics of TMD3719

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I²C clock frequency	0		400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HS;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	0.6			
$t_{SU;STA}$	Repeated start condition setup time	0.6			
$t_{SU;STO}$	Stop condition setup time	0.6			
t_{LOW}	SCL clock low period	1.3			
t_{HIGH}	SCL clock low period	0.6			
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			
t_F	Clock/data fall time			300	
t_R	Clock/data rise time			300	

Figure 11:
Timing Diagram for TMD3719

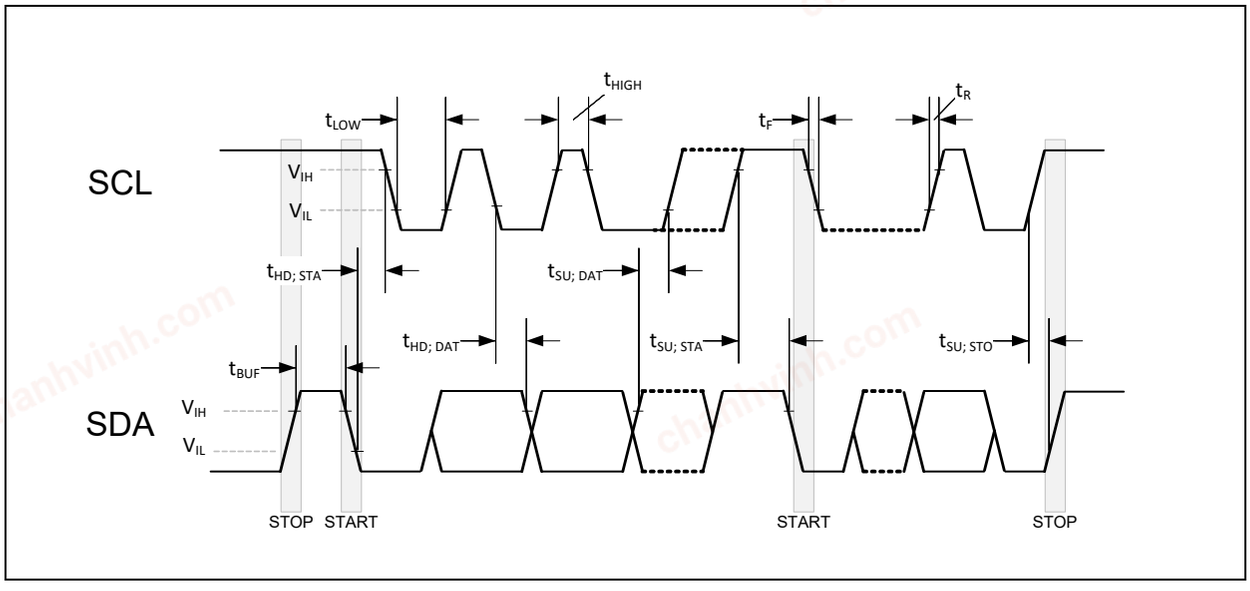

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Figure 12:
Functional Timing Characteristics of TMD3719

Symbol	Parameter	Min	Typ	Max	Unit
f_{OSC}	Oscillator clock frequency (1)	357	369	380	kHz
t_{OSL}	Oscillator clock cycle (1)	2.63	2.71	2.80	µs
$t_{(PROX\ ADC)}$	Proximity ADC conversion time		20		µs

Note(s):

1. 100% production tested.

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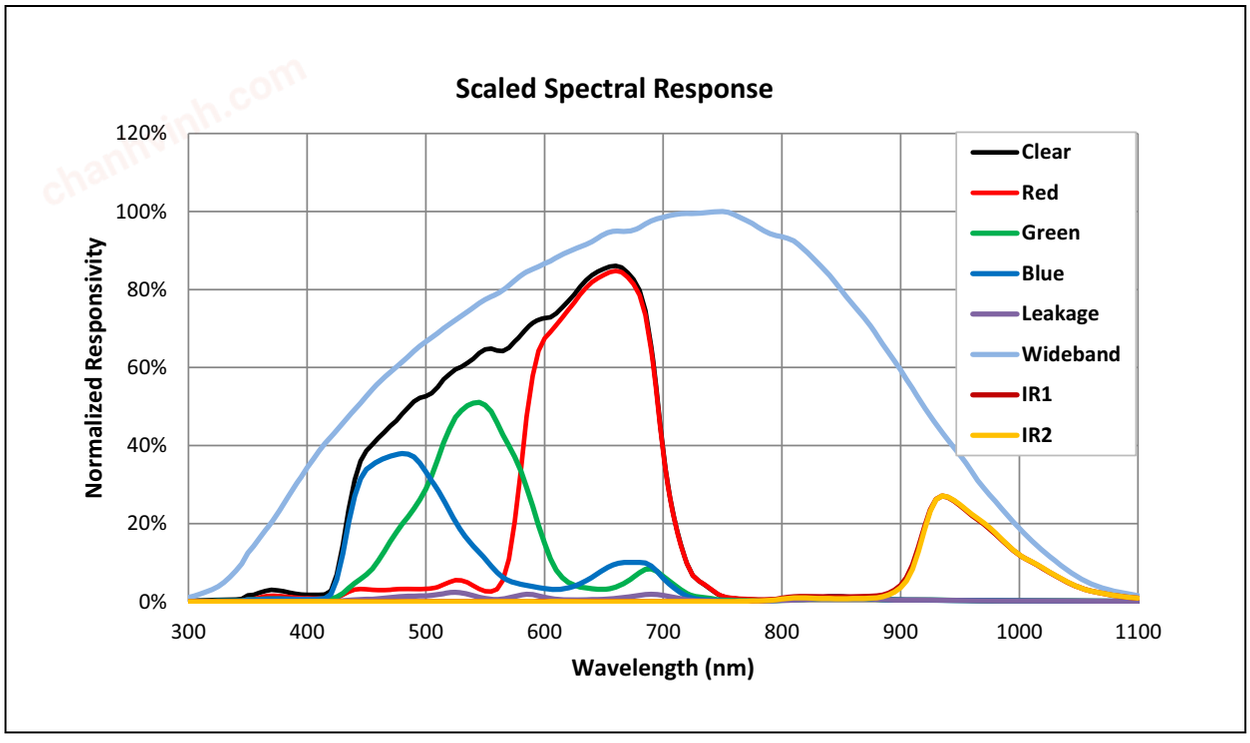
Typical Operating Characteristics

Figure 13:
Spectral Responsivity



Note(s):

1. The spectral responsivities shown in the figure are scaled based on the photodiode area of each channel. The scaling factors used to generate this figure are (relative to CLEAR): 1.25 for Leakage, 2.5 for Wideband, 0.18 for IR1 and 0.25 for IR2. Once scaled, the responsivities are normalized.

Figure 14:
Angular Response

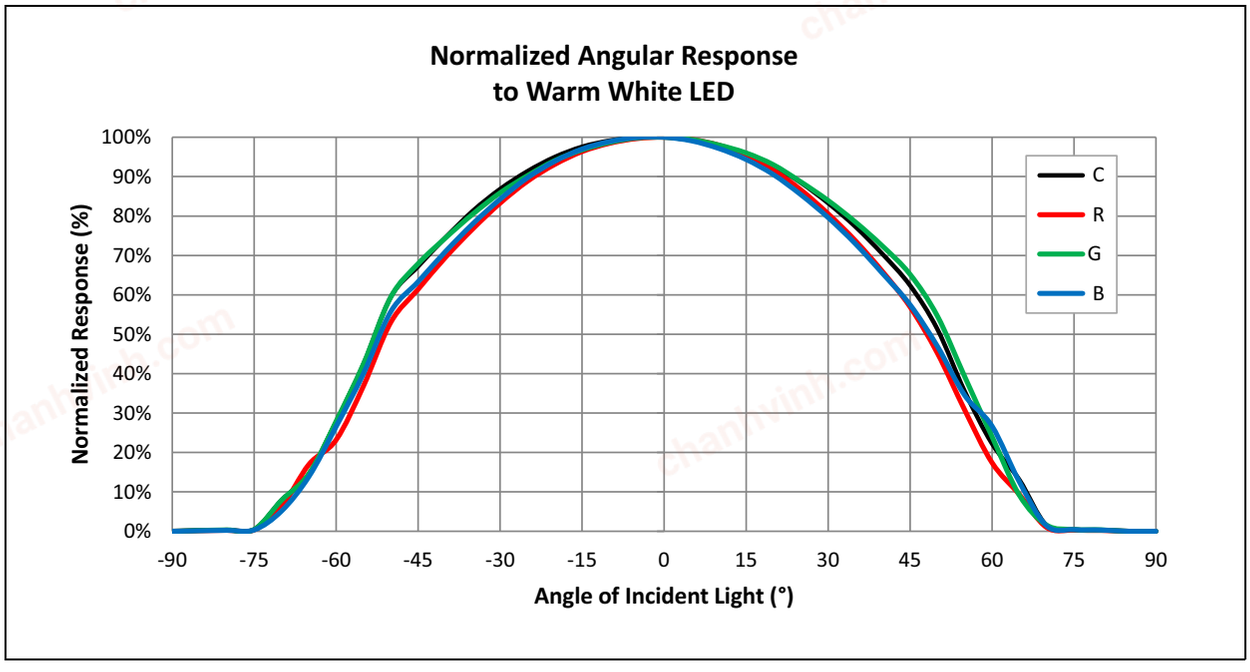


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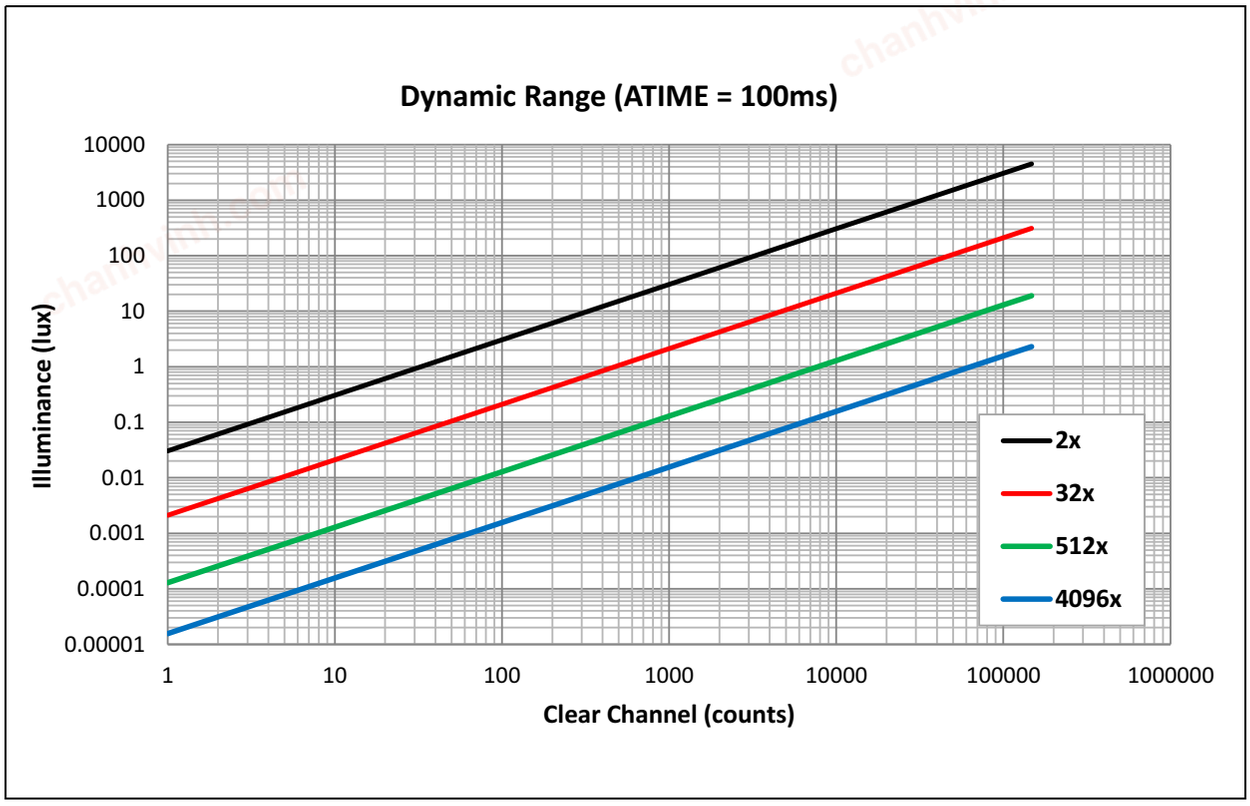
Figure 15:
Illuminance (Lux) vs. Counts (Clear Channel)



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Detailed Description

Upon power-up, POR, the device initializes. During initialization (maximum of 1.5ms), the device will deterministically send NAK on I^2C and cannot accept I^2C transactions. All communication with the device must be delayed, and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I^2C transaction occurs during this state, the I^2C core wakes up temporarily to service the communication. Once the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever a function is enabled (PEN | AEN = 1) the device exits the IDLE state. If all functions are disabled (PEN = 0 & AEN = 0), the device returns to the IDLE state.

As depicted in Figure 16 the proximity and CRGBLW color sensing functions operate in parallel when enabled (PEN | AEN = 1). In addition, when proximity calibration is requested, it will temporarily disable the proximity function. Each function is individually configured (e.g. gain, ADC integration time, wait time, persistence, thresholds, etc.).

If Sleep after Interrupt is enabled (SAI = 1 in register 0x96), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xBE and the clear status bit is in register 0xF6).

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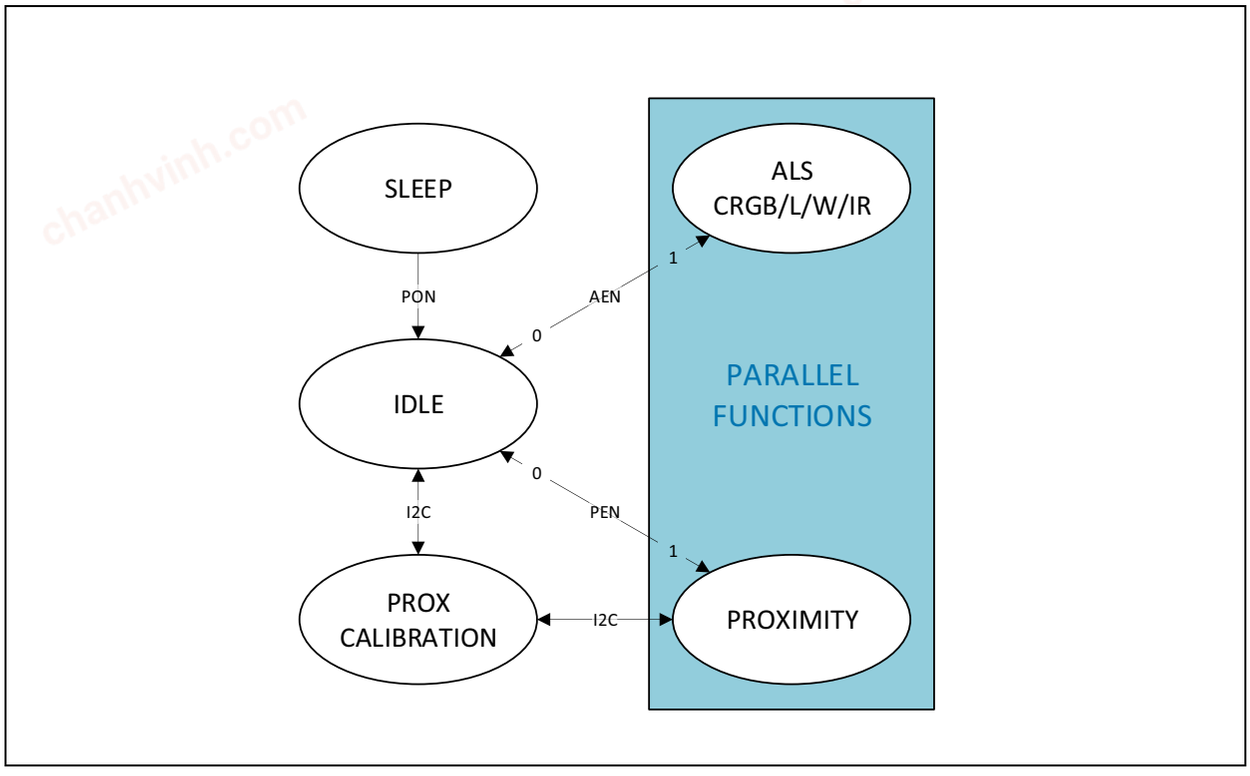
State Machine Diagrams

Figure 16:
Simplified State Diagram



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I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

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Register Overview

The device is controlled and monitored by registers accessed through the I^2C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

Register Map

The register set is summarized in Figure 17. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. Bits 7 (MSB) through 0 (LSB) are shown in the last columns of the table. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

The functions column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (bit7) to LSB (bit0). **GRAY** indicates fields apply independent of one function or apply to all functions, **GREEN** indicates fields that are pertinent to ALS/color sensing and flicker detection and **BLUE** indicates fields that are pertinent to proximity detection. **WHITE** fields are reserved and their values must not be changed at any time.

Figure 17:
Register Map

Addr	Name	Type	Description	7	6	5	4	3	2	1	0	Reset
0x2E	AILT	R/W	ALS interrupt low threshold	00000000								0x00
0x2F				00000000								0x00
0x30				00000000								0x00
0x31	AIHT	R/W	ALS interrupt high threshold	00000000								0x00
0x32				00000000								0x00
0x33				00000000								0x00
0x34	PILT0	R/W	Proximity interrupt low threshold zero	00000000								0x00
0x35				00000000								0x00
0x36	PIHT0	R/W	Proximity interrupt high threshold zero	00000000								0x00
0x37				00000000								0x00
0x38	PILT1	R/W	Proximity interrupt low threshold one	00000000								0x00
0x39				00000000								0x00
0x3A	PIHT1	R/W	Proximity interrupt high threshold one	00000000								0x00
0x3B				00000000								0x00

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Addr	Name	Type	Description	7	6	5	4	3	2	1	0	Reset
0x3C	PILTR	R/W	Proximity interrupt low threshold ratio	00000000								0x00
0x3D				00000000								0x00
0x3E	PIHTR	R/W	Proximity interrupt high threshold ratio	00000000								0x00
0x3F				00000000								0x00
0x40	FD_CFG0	R/W	Flicker detection configuration zero	000			00		0	01		0x01
0x41	FD_CFG1	R/W	Flicker detection configuration one	000			00000					0x00
0x42	FD_CFG2	R/W	Flicker detection configuration two	000			00000					0x00
0x43	FD_CFG3	R/W	Flicker detection configuration three	000			00000					0x00
0x44	FD_CFG4	R/W	Flicker detection configuration four	000			00000					0x00
0x45	FD_CFG5	R/W	Flicker detection configuration five	11111110								0xFE
0x47	FD_CFG7	R/W	Flicker detection configuration seven	000000						01		0x01
0x48	FD_CFG8	R/W	Flicker detection configuration eight	01100111								0x67
0x4F	SYNC_DELAY	R/W	Synchronized delay	00000000								0x00
0x50				00000000								0x00
0x53	VSYNC_CFG0	R/W	Vertical sync configuration zero	0001				0	0	00		0x10
0x54	VSYNC_CFG1	R/W	Vertical sync configuration one	00		010000						0x10
0x56	VSYNC_CFG2	R/W	Vertical sync configuration two	00000000								0x00
0x57	VSYNC_CFG3	R/W	Vertical sync configuration three	00000000								0x00
0x69	CALIB	R/W	Calibration start	0000000							0	0x00
0x6A	CALIBCFG0	R/W	Calibration configuration zero	0	0	00		0	000			0x00
0x6B	CALIBCFG1	R/W	Calibration configuration one	0	0	0	0	1	100			0x0C
0x6C	CALIBCFG2	R/W	Calibration configuration two	000			00000					0x00
0x6D	CALIBSTAT	R/W	Calibration status	00000					0	0	0	0x00
0x80	ENABLE	R/W	Enable device states	0	0	0	0	0	00		0	0x00

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Addr	Name	Type	Description	7	6	5	4	3	2	1	0	Reset
0x81	MEAS_MODE0	R/W	Measurement mode zero	0	0	00		00		0	0	0x00
0x82	MEAS_MODE1	R/W	Measurement mode one	0	0	000		000				0x00
0x83	TRIGGER_MODE	R/W	Trigger Mode	0	000			0	000			0x00
0x84	ATIME	R/W	ALS integration time	00000000								0x00
0x85	ASTEP	R/W	ALS integration step	11111111								0xFF
0x86				00000011								0x03
0x87	PTIME	R/W	Proximity time	00000000								0x00
0x88	WTIME	R/W	Wait time	00000000								0x00
0x89	MOD_GAIN_0_1	R/W	Modulator zero and one gain	0000				0000				0x00
0x8A	MOD_GAIN_2_3	R/W	Modulator two and three gain	0000				0000				0x00
0x8B	MOD_GAIN_4_5	R/W	Modulator four and five gain	0000				0000				0x00
0x8C	MOD_GAIN_6_7	R/W	Modulator six and seven gain	0000				0000				0x00
0x8D	AGC_ENABLE	R/W	AGC enable	0	0	0	0	0	0	0	0	0x00
0x90	AUXID	R	Auxiliary identification	00000011								0x03
0x91	REVID	R	Revision identification	00010011								0x13
0x92	ID	R	Device identification	01000000								0x40
0x93	CFG0	R/W	Configuration zero	0	0	100		000				0x20
0x96	CFG3	R/W	Configuration three	00		0	0	1111				0x0F
0x97	CFG4	R/W	Configuration four	0000				0000				0x00
0x9A	PERS	R/W	Persistence configuration	0001				0001				0x11
0x9B	CFG8	R/W	Configuration eight	10		000000						0x80
0x9C	CFG9	R/W	Configuration nine	0	0	000000						0x00
0x9D	CFG10	R/W	Configuration ten	11		11		0010				0xF2
0x9E	CFG11	R/W	Configuration eleven	0	1	000000						0x40
0x9F	CFG12	R/W	Configuration twelve	00000				000				0x00
0xA4	AZ_CONFIG	R/W	Autozero configuration	11111111								0xFF
0xA7	CFG20	R/W	Configuration twenty	000			0	0000				0x00
0xAA	PCFG1	R/W	Proximity configuration one	0	000			0	000			0x00
0xAB	PCFG2	R/W	Proximity configuration two	00		00		0000				0x00
0xAC	PCFG3	R/W	Proximity configuration three	0000				0000				0x00

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Addr	Name	Type	Description	7	6	5	4	3	2	1	0	Reset
0xAD	PCFG4	R/W	Proximity configuration four	0000				10		10		0x0A
0xAE	PCFG5	R/W	Proximity configuration five	00001111								0x0F
0xAF	PCFG6	R/W	Proximity configuration six	0	000			0	0	0	0	0x00
0xB0	PCFG7	R/W	Proximity configuration seven	000			0	0	001			0x01
0xB1	POFFSET0	R/W	Proximity offset zero	00000000								0x00
0xB2				00000000								0x00
0xB3	PXAVG	R/W	Proximity average	00000000								0x00
0xB4				00000000								0x00
0xB5	PBSLN	R/W	Proximity baseline	00000000								0x00
0xB6				00000000								0x00
0xB7	STATUS	R/W	Device status one	0	0	0	0	0	0	0	0	0x00
0xB8	STATUS2	R/W	Device status two	0	0	0	0	0	0	0	0	0x00
0xB9	STATUS3	R/W	Device status three	0	0	0	0	0	0	0	0	0x00
0xBA	STATUS4	R/W	Device status four	0	0	0	0	0	0	0	0	0x00
0xBB	STATUS5	R/W	Device status five	0000				0	00		0	0x00
0xBD	STATUS7	R/W	Device status seven	0	0	00		0	0	0	0	0x00
0xBE	STATUS8	R/W	Device status eight	00		0	0	0	0	0	0	0x00
0xBF	STATUS9	R	Device status nine	0000				0	000			0x00
0xC0	ASTATUS	R	ALS status	0000000							0	0x00
0xC1	ADATA0	R	ALS channel zero data	00000000								0x00
0xC2				00000000								0x00
0xC3				00000000								0x00
0xC4	ADATA1	R	ALS channel one data	00000000								0x00
0xC5				00000000								0x00
0xC6				00000000								0x00
0xC7	ADATA2	R	ALS channel two data	00000000								0x00
0xC8				00000000								0x00
0xC9				00000000								0x00

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Addr	Name	Type	Description	7	6	5	4	3	2	1	0	Reset
0xCA	ADATA3	R	ALS channel three data	00000000 00000000 00000000								0x00
0xCB												0x00
0xCC												0x00
0xCD	ADATA4	R	ALS channel four data	00000000 00000000 00000000								0x00
0xCE												0x00
0xCF												0x00
0xD0	ADATA5	R	ALS channel five data	00000000 00000000 00000000								0x00
0xD1												0x00
0xD2												0x00
0xD3	ADATA6	R	ALS channel six data	00000000 00000000 00000000								0x00
0xD4												0x00
0xD5												0x00
0xD6	ADATA7	R	ALS channel seven data	00000000 00000000 00000000								0x00
0xD7												0x00
0xD8												0x00
0xD9	PSTATUS	R	Proximity status	0	0	000000						0x00
0xDA	PDATA0	R	Proximity channel zero data	00000000 00000000								0x00
0xDB												0x00
0xDC	PDATA1	R	Proximity channel one data	00000000 00000000								0x00
0xDD												0x00
0xDE	PDATAR	R	Proximity channel ratio data	00000000 00000000								0x00
0xDF												0x00
0xF2	GPIO	R/W	GPIO configuration	00		0	0	0	0	1	0	0x02
0xF4	AGC_GAIN_MAX	R/W	Maximum AGC gain	00000					110			0x06
0xF5	INTENAB	R/W	Enable interrupts	0	0	0	0	0	0	0	0	0x00
0xF6	CONTROL	R/W	Control	00000					0	0	0	0x00
0xF7	POFFSET1	R/W	Proximity offset one	00000000 00000000								0x00
0xF8												0x00
0xF9	FIFO_MAP	R/W	FIFO buffer map configuration	0	0	0	0	0	0	0	0	0x00

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Addr	Name	Type	Description	7	6	5	4	3	2	1	0	Reset
0xFA	FIFO_MAP2	R/W	FIFO buffer map configuration two	000			0	0	0	0	0	0x00
0xFB	FIFO_STATUS	R	FIFO buffer status	0	0000000							0x00
0xFC	FDATA	R	FIFO buffer data	00000000 00000000 00000000 00000000								0x00
0xFD												0x00
0xFE												0x00
0xFF												0x00

Detailed Register Descriptions

ALS Interrupt Thresholds

ALS level detection uses data generated by the ADC Channel X. The channel can be selected via ALS_TH_CHANNEL (see CFG12). The ALS Interrupt Threshold registers provide 24-bit values to be used as the high and low thresholds for comparison to the 24-bit ADATAX values. If AIEN is enabled and ADATAX is not between AILT and AIHT for the number of consecutive samples specified in APERS an interrupt is asserted on the interrupt pin. These registers are read/write.

Figure 18:
ALS Interrupt Thresholds

Bits	Addr	Field	Reset	Type	Description
7:0	0x2E	AILT	0x00	R/W	ALS Interrupt Low Threshold
15:8	0x2F		0x00	R/W	
23:16	0x30		0x00	R/W	
7:0	0x31	AIHT	0x00	R/W	ALS Interrupt High Threshold
15:8	0x32		0x00	R/W	
23:16	0x33		0x00	R/W	

Note(s):

1. Return to the Register Map (0x2E, 0x2F, 0x30, 0x31, 0x32, 0x33)

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Proximity Interrupt Thresholds

The Proximity Interrupt Threshold Registers set the high and low trigger points for the comparison function which generates an interrupt. Interrupt generation is subject to the value set in persistence filter (PPERS). These registers are read/write.

Figure 19:
Proximity Interrupt Thresholds

Bits	Addr	Field	Reset	Type	Description
7:0	0x34	PILT0	0x00	R/W	Proximity Interrupt Low Threshold Zero
15:8	0x35		0x00	R/W	
7:0	0x36	PIHT0	0x00	R/W	Proximity Interrupt High Threshold Zero
15:8	0x37		0x00	R/W	
7:0	0x38	PILT1	0x00	R/W	Proximity Interrupt Low Threshold One
15:8	0x39		0x00	R/W	
7:0	0x3A	PIHT1	0x00	R/W	Proximity Interrupt High Threshold One
15:8	0x3B		0x00	R/W	
7:0	0x3C	PILTR	0x00	R/W	Proximity Interrupt Low Threshold Ratio
15:8	0x3D		0x00	R/W	
7:0	0x3E	PIHTR	0x00	R/W	Proximity Interrupt High Threshold Ratio
15:8	0x3F		0x00	R/W	

Note(s):

1. Return to the Register Map (0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F)

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Figure 20:
FD_CFG0

Addr: 0x40		FD_CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4:3	FD_SAMPLES	00	R/W	Flicker Detection Number of Samples. **VALUE** / **SAMPLES** 0 (default) / 128 1 / 256 2 / 512 3 / 1024(2)
2	Reserved	0		
1:0	FD_TIME	01	R/W	Flicker Detection Time. **VALUE** / **TIME** 0 / 50ms 1 (default) / 100ms 2 / 200ms 3 / User defined by FD_SAMPLE_TIME and FD_SAMPLES

Note(s):

1. Return to the Register Map (0x40)
2. If FD_MODE = 1 then number of samples changes from 1024 to unlimited.

Figure 21:
FD_CFG1

Addr: 0x41		FD_CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4:0	FD_BIN0	00000	R/W	**Flicker Detection Bin Zero.** Coefficient to use for Bin 0.

Note(s):

1. Return to the Register Map (0x41)

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Figure 22:
FD_CFG2

Addr: 0x42		FD_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4:0	FD_BIN1	00000	R/W	**Flicker Detection Bin One.** Coefficient to use for Bin 1.

Note(s):

1. Return to the Register Map (0x42)

Figure 23:
FD_CFG3

Addr: 0x43		FD_CFG3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4:0	FD_BIN2	00000	R/W	**Flicker Detection Bin Two.** Coefficient to use for Bin 2.

Note(s):

1. Return to the Register Map (0x43)

Figure 24:
FD_CFG4

Addr: 0x44		FD_CFG4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4:0	FD_BIN3	00000	R/W	**Flicker Detection Bin Three.** Coefficient to use for Bin 3.

Note(s):

1. Return to the Register Map (0x44)

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Figure 25:
FD_CFG5

Addr: 0x45		FD_CFG5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FD_CHANNEL_DISABLE	0xFE	R/W	**Flicker Detection Channel Disable.** Selects which channels to be used for flicker detection.

Note(s):

1. Return to the Register Map (0x45)

Figure 26:
FD_CFG7

Addr: 0x47		FD_CFG7		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	000000		
1:0	FD_SAMPLE_TIME_H	01	R/W	**Flicker Detection Sample Time High.** These bits are the high byte of the 10 bits used for setting the flicker detection integration time.

Note(s):

1. Return to the Register Map (0x47)

Figure 27:
FD_CFG8

Addr: 0x48		FD_CFG8		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FD_SAMPLE_TIME_L	0x67	R/W	**Flicker Detection Sample Time Low.** This register is the low byte of the 10 bits used for setting the flicker detection integration time.

Note(s):

1. Return to the Register Map (0x48)

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Figure 28:
SYNC_DELAY

Bits	Addr	Field	Reset	Type	Description
7:0	0x4F	SYNC_DELAY	0x00	R/W	Synchronized Delay
14:8	0x50 [6:0]		0000000	R/W	

Note(s):

1. Return to the Register Map (0x4F, 0x50)

Figure 29:
VSYNC_CFG0

Addr: 0x53		VSYNC_CFG0			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:4	Reserved	0001			
3	VSYNC_FREQ_LL_IGNORE	0	R/W	VSYNC Frequency Low Limit Ignore.	
2	Reserved	0			
1:0	OSC_CAL_MODE	00	R/W	Oscillator Calibration Mode.	
				VALUE	**MODE**
				0 (default)	No oscillator calibration
				1	Single oscillator calibration after PON is set to 1.
				2	Oscillator calibration is performed whenever possible
				3	Reserved

Note(s):

1. Return to the Register Map (0x53)

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Figure 30:
VSYNC_CFG1

Addr: 0x54		VSYNC_CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	00		
5:0	VSYNC_FREQ	010000	R/W	Vertical SYNC Frequency. Frequency = 28Hz + (2Hz * VSYNC_FREQ)

Note(s):

1. Return to the Register Map (0x54)

Figure 31:
VSYNC_CFG2

Addr: 0x56		VSYNC_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	VSYNC_CFG2	0x00	R/W	**Vertical Sync Configuration Two.** Start time delay for first set of proximity pulses for SYNC measurement.

Note(s):

1. Return to the Register Map (0x56)

Figure 32:
VSYNC_CFG3

Addr: 0x57		VSYNC_CFG3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	VSYNC_CFG3	0x00	R/W	**Vertical Sync Configuration Three.** Start time delay for second set of proximity pulses for SYNC measurement.

Note(s):

1. Return to the Register Map (0x57)

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Figure 33:
CALIB

Addr: 0x69		CALIB		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:1	Reserved	0000000		
0	START_OFFSET_CALIB	0	PUSH	**Start Offset Calibration.** Starts the proximity offset register calibration routine. Results are stored in the Proximity Offset Registers (0xC7 – 0xC8). The CALIB_FINISHED flag is asserted when calibration is complete and an interrupt (CINT) is asserted if CIEN is set. Calibration can be stopped immediately by writing a 0 to this field.

Note(s):

1. Return to the Register Map (0x69)

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Figure 34:
CALIBCFG0

Addr: 0x6A		CALIBCFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	DCAVG_AUTO_BSLN	0	R/W	**DC Averaging Automatic Baseline.** Load the DC average calculated during offset calibration into the PBSLN registers at the end of calibration. Note that if the offset is adjusted (by zero detection) during the DC averaging, the average may be incorrect.
6	DCAVG_AUTO_OFFSET_ADJUST	0	R/W	**DC Averaging Auto Offset Adjust.** If set, then during DC averaging, whenever an ADC measurement is zero, the appropriate offset register will be decreased and the OFFSET_ADJUSTED flag is set. Note also that DC averaging is not automatically restarted when this happens, so the calculated baseline might be wrong. Software could restart averaging in this case.
5:4	Reserved	00		
3	BINSRCH_SKIP	0	R/W	**Binary Search Skip.** When asserted the calibration routine will skip the binary search step. It is useful if zeros are detected during the DC averaging process to manually reset the baseline and reduce the likelihood of zero counts.
2:0	DCAVG_ITERATIONS	000	R/W	**DC Averaging Iterations.** Sets the number of proximity results during calibration that are averaged after the binary search is complete. During this period, whenever a result is zero, the appropriate offset register is automatically decremented.

VALUE	ITERATIONS
0	Skip
1	2
2	4
...	$2^{DCAVG_ITERATIONS}$
6	64
7	128

Note(s):

1. Return to the Register Map (0x6A)

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Figure 35:
CALIBCFG1

Addr: 0x6B		CALIBCFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	PROX_AUTO_OFFSET_ ADJUST	0	R/W	**Proximity Auto Offset Adjust.** If set, then during proximity/gesture mode, whenever an ADC measurement is zero, the appropriate offset register will be decreased. If this happens, OFFSET_ADJUSTED will be set to 1 and CINT will occur if enabled.
5	PROX_SUBT_BSLN1	0	R/W	Proximity Subtract Baseline One.
4	PROX_SUBT_BSLN0	0	R/W	Proximity Subtract Baseline Zero.
3	PXAVG_AUTO_BSLN	1	R/W	**Proximity Average Auto Baseline Adjust.** If asserted, PBSLN is automatically updated with the value of PXAVG whenever PXAVG is less than previous PBSLN. If this happens, BASELINE_ ADJUSTED will be set to 1 and CINT will occur if enabled.
2:0	PXAVG_ITERATIONS	100	R/W	**Proximity Average Iterations.** Sets the number of proximity results that are averaged during normal proximity operation. The resulting proximity average is stored as a 14-bit value in the PXAVG registers after each set of iterations is complete.

VALUE	ITERATIONS
0	Skip
1	2
2	4
...	$2^{DCAVG_ITERATIONS}$
6	64
7	128

Note(s):

1. Return to the Register Map (0x6B)

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Figure 36:
CALIBCFG2

Addr: 0x6C		CALIBCFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	BINSRCH_TARGET	000	R/W	**Binary Search Target.** Sets the target value for proximity used during calibration. The target value is $2^{(BINSRCH_TARGET + 2)} - 1$ counts.

VALUE	COUNTS
0	3
1	7
2	15
...	$2^{(BINSRCH_TARGET + 2)}-1$
6	255
7	511

4:0	Reserved	00000		

Note(s):

1. Return to the Register Map (0x6C)

Figure 37:
CALIBSTAT

Addr: 0x6D		CALIBSTAT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	00000		
2	BASELINE_ADJUSTED	0	R/W	**Baseline Adjusted Automatically.** Indicates that PBSLN was reduced because PXAVG was smaller than PBSLN. Only occurs if PXAVG_AUTO_BSLN is set. Clear bit by writing 1 to it.
1	OFFSET_ADJUSTED	0	R/W	**Offset Adjusted Automatically.** Indicates that proximity offset has been adjusted automatically. Only occurs if PROX_AUTO_OFFSET_ADJUST is set. Clear bit by writing 1 to it.
0	CALIB_FINISHED	0	R/W	**Calibration Finished.** Indicates that calibration is complete. Clear bit by writing 1 to it.

Note(s):

1. Return to the Register Map (0x6D)

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Power, Enable, and Operation

The enable register has fields that power on the device and enable the functions. To operate the device, first set all configuration fields for all functions, then set PON = 1, and finally enable functions. Changing configuration register values while functions are operating may result in invalid results.

Figure 38:
ENABLE

Addr: 0x80		ENABLE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	FDEN	0	R/W	**Flicker Detection Enable.** Writing a 1 activates flicker detection. Writing a 0 disables flicker detection.
5	Reserved	0		
4	AEN	0	R/W	**ALS Enable.** Writing a 1 enables ALS/Color. Writing a 0 disables ALS/Color.
3	PEN	0	R/W	**Proximity Enable.** Writing a 1 enables proximity. Writing a 0 disables proximity.
2:1	Reserved	00		
0	PON	0	R/W	**Power ON.** When asserted, the internal oscillator is activated, allowing timers and ADC channels to operate. Writing a 0 disables the oscillator and clears PEN and AEN. Only set this bit after all other registers have been initialized by the host.

Note(s):

1. Return to the Register Map (0x80)

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Figure 39:
MEAS_MODE0

Addr: 0x81		MEAS_MODE0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	CL_APF_VSYNC	0	R/W	Classical ALS Proximity Flicker Detection with next VSYNC.
5:4	Reserved	00		
3:2	PROX_DIODE_ENABLE	00	R/W	**Proximity Diode Enable.** Write '11' to these two bits to enable the proximity diodes for measurement.
1	ALS DIODE SELECTION	0	R/W	**ALS Diode Selection.** Select which chain mode to use for ALS measurements. Writing a 0 will select ALS Set A and writing a 1 will select ALS Set B.
0	ALS_DIODE_ENABLE	0	R/W	**Enable ALS Diodes.** Write 1 to enable the ALS diodes for measurement.

Note(s):

1. Return to the Register Map (0x81)

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Figure 40:
MEAS_MODE1

Addr: 0x82		MEAS_MODE1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	FD_MODE	0	R/W	**Flicker Detection Mode.** Writing a 0 will set the FD to on-chip mode and writing a 1 will set the FD to data sampling mode.
5:3	Reserved	000	R/W	
2:0	FIFO_MODE	0	R/W	FIFO Mode.

VALUE	MODE
0	Off
1	32-bit
2	16-bit ALS
3	16-bit FD
4	8-bit FD
5 - 7	Reserved

Note(s):

1. Return to the Register Map (0x82)

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Figure 41:
TRIGGER_MODE

Addr: 0x83		TRIGGER_MODE			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7	VSYNC_START_ALIGN	0	R/W	**VSYNC Start Alignment.** Enables aligned start for ALS/Proximity/Flicker with VSYNC.	
6:4	PROX_TRIGGER_TIMING	000	R/W	**Proximity Trigger Timing.** Selects Proximity trigger timing step.	
				VALUE	**TIMING**
				0	Off
				1	Normal (2.78ms)
				2	Long (50ms)
				3	Fast (86.61µs)
				4	Fast/Long (1.56ms)
				5	VSYNC
				6, 7	Reserved
3	Reserved	0		**Modulator Trigger Timing.** Selects Modulator trigger timing step.	
2:0	MOD_TRIGGER_TIMING	0	R/W	**VALUE**	**TIMING**
				0	Off
				1	Normal (2.78ms)
				2	Long (50ms)
				3	Fast (86.61µs)
				4	Fast/Long (1.56ms)
				5	VSYNC
				6, 7	Reserved

Note(s):

1. Return to the Register Map (0x83)

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Figure 42:
ATIME

Addr: 0x84		ATIME		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	ATIME	0x00	R/W	**ALS Integration Time.** Sets the number of ALS/color integration steps from 1 to 256.

VALUE	INTEGRATION TIME
0	ASTEP
n	ASTEP × (*n*+1)
255	256 × ASTEP

Note(s):

1. Return to the Register Map (0x84)

Figure 43:
ASTEP

Bits	Addr	Field	Reset	Type	Description
7:0	0x85	ASTEP	0xFF	R/W	**ALS Integration Time Step Size.** Sets the integration time per step in increments of 2.7127µs. The default value is 1023. Type is read/write.
15:8	0x86		0x03	R/W	

VALUE	STEP SIZE
0	2.71µs
n	2.7127µs × (*n*+1)
1023	2.78ms
18431	50ms
65535	178ms

Note(s):

1. Return to the Register Map (0x85, 0x86)

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Figure 44:
PTIME

Addr: 0x87		PTIME		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	PTIME	0x00	R/W	**Proximity Sample Time.** Sets the sample rate of proximity.

Note(s):

1. Return to the Register Map (0x87)

Figure 45:
WTIME

Addr: 0x88		WTIME		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	WTIME	0	R/W	**Wait Time.** Sets the sample rate of the ALS/color function.

Note(s):

1. Return to the Register Map (0x88)

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Figure 46:
MOD_GAIN_0_1

Addr: 0x89		MOD_GAIN_0_1			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:4	MOD_GAIN1	0000	R/W	Modulator One Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

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Addr: 0x89		MOD_GAIN_0_1			
Bit	Field	Reset	Type	Bit Description	
3:0	MOD_GAIN0	0000	R/W	Modulator Zero Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

Note(s):

1. Return to the Register Map (0x89)

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Figure 47:
MOD_GAIN_2_3

Addr: 0x8A		MOD_GAIN_2_3			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:4	MOD_GAIN3	0000	R/W	Modulator Three Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

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Addr: 0x8A		MOD_GAIN_2_3			
Bit	Field	Reset	Type	Bit Description	
3:0	MOD_GAIN2	0000	R/W	Modulator Two Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

Note(s):

1. Return to the Register Map (0x8A)

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Figure 48:
MOD_GAIN_4_5

Addr: 0x8B		MOD_GAIN_4_5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MOD_GAIN5	0000	R/W	Modulator Five Gain.

VALUE	GAIN
0	2x
1	4x
2	8x
3	16x
4	32x
5	64x
6	128x
7	256x
8	512x
9	1024x
10	2048x
11	4096x
12 - 15	Reserved

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Addr: 0x8B		MOD_GAIN_4_5			
Bit	Field	Reset	Type	Bit Description	
3:0	MOD_GAIN4	0000	R/W	Modulator Four Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

Note(s):

1. Return to the Register Map (0x8B)

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Figure 49:
MOD_GAIN_6_7

Addr: 0x8C		MOD_GAIN_6_7			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:4	MOD_GAIN7	0000	R/W	Modulator Seven Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

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Addr: 0x8C		MOD_GAIN_6_7			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
3:0	MOD_GAIN6	0000	R/W	Modulator Six Gain.	
				VALUE	**GAIN**
				0	2x
				1	4x
				2	8x
				3	16x
				4	32x
				5	64x
				6	128x
				7	256x
				8	512x
				9	1024x
				10	2048x
				11	4096x
				12 - 15	Reserved

Note(s):

1. Return to the Register Map (0x8C)

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Figure 50:
AGC_ENABLE

Addr: 0x8D		AGC_ENABLE		
Bit	Field	Reset	Type	Bit Description
7	AGC_ENABLE_MOD_7	0	R/W	**AGC Enable Modulator Seven.** If asserted, then device will use automatic gain control for the modulator seven to maximize ALS signal while avoiding saturation.
6	AGC_ENABLE_MOD_6	0	R/W	**AGC Enable Modulator Six.** If asserted, then device will use automatic gain control for the modulator six to maximize ALS signal while avoiding saturation.
5	AGC_ENABLE_MOD_5	0	R/W	**AGC Enable Modulator Five.** If asserted, then device will use automatic gain control for the modulator five to maximize ALS signal while avoiding saturation.
4	AGC_ENABLE_MOD_4	0	R/W	**AGC Enable Modulator Four.** If asserted, then device will use automatic gain control for the modulator four to maximize ALS signal while avoiding saturation.
3	AGC_ENABLE_MOD_3	0	R/W	**AGC Enable Modulator Three.** If asserted, then device will use automatic gain control for the modulator three to maximize ALS signal while avoiding saturation.
2	AGC_ENABLE_MOD_2	0	R/W	**AGC Enable Modulator Two.** If asserted, then device will use automatic gain control for the modulator two to maximize ALS signal while avoiding saturation.
1	AGC_ENABLE_MOD_1	0	R/W	**AGC Enable Modulator One.** If asserted, then device will use automatic gain control for the modulator one to maximize ALS signal while avoiding saturation.
0	AGC_ENABLE_MOD_0	0	R/W	**AGC Enable Modulator Zero.** If asserted, then device will use automatic gain control for the modulator zero to maximize ALS signal while avoiding saturation.

Note(s):

1. Return to the Register Map (0x8D)

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Identification

The identification registers provide auxiliary identification for special cases, wafer revision data, and device identification. All identification registers are read only.

Figure 51:
Identification Registers

Bits	Addr	Field	Reset	Type	Description
7:0	0x90	AUXID	0x03	R	Auxiliary Identification.
7:0	0x91	REVID	0x13	R	Revision Identification.
7:0	0x92	ID	0x40	R	Device Identification.

Note(s):

1. Return to the Register Map (0x90, 0x91, 0x92)

Figure 52:
CFG0

Addr: 0x93		CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	LOWPOWER_IDLE	0	R/W	**Low Power Idle.** When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled.
5:3	Reserved	100		
2:0	RAM_BANK	000	R/W	**RAM Bank Selection.** Specifies the RAM bank to access in registers 0x00 to 0x7F.

VALUE	BANK
0	0
1	4
2, 4, 5, 6, 7	Remote Control
3	On-Chip Flicker

Note(s):

1. Return to the Register Map (0x93)

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Figure 53:
CFG3

Addr: 0x96		CFG3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	00		
5	HXTALK_MODE1	0	R/W	**High Crosstalk Mode.** If asserted, the proximity engine uses a 10-bit output mode for no aperture proximity operation intended for extremely high optical crosstalk systems. HXTALK_MODE1 and HXTALK_MODE2 must both be asserted for this function to work.
4	SAI	0	R/W	**Sleep After Interrupt.** If asserted, the oscillator is turned off whenever interrupt is active (low). SAI_ ACTIVE is set in this event. To activate the oscillator again, service and clear all interrupts plus clear the SAI_ACTIVE bit.
3:0	Reserved	1111		

Note(s):

1. Return to the Register Map (0x96)

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Figure 54:
CFG4

Addr: 0x97		CFG4			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:4	INT_PINMAP	0000	R/W	**Interrupt Pin Map.** Selects the signal to output on the INT pin.	
				VALUE	**INTERRUPT PIN**
				0	Normal
				1	Reserved
				2	AINT Direct
				3	PINT Direct
				4, 5	Inverted
				6	VCSEL pulse
				7 - 15	Reserved
3:0	GPIO_PINMAP	0000	R/W	**GPIO Pin Map.** Selects the signal to output on the GPIO pin.	
				VALUE	**GPIO PIN**
				0	Normal
				1	Reserved
				2	AINT Direct
				3	PINT Direct
				4, 5	Inverted
				6	VCSEL pulse
				7 - 15	Reserved

Note(s):

1. Return to the Register Map (0x97)

Persistence filters limit the rate of interrupts generated for proximity and ALS/color data.

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Figure 55:
PERS

Addr: 0x9A		PERS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	PPERS	0001	R/W	**Proximity Interrupt Persistence.** Defines a filter for the number of consecutive occurrences that PDATA must remain outside the threshold range between PILT and PIHT before an interrupt is generated. Any sample that is inside the threshold range resets the counter to 0.
				VALUE / **CONSECUTIVE PDATA OUT OF RANGE TO INTERRUPT**
				0 / Every proximity cycle generates an interrupt
				1 / 1
				2 / 2
				... / PPERS
				15 / 15
3:0	APERS	0001	R/W	**ALS Interrupt Persistence.** Defines a filter for the number of consecutive occurrences that ALS/color data must remain outside the threshold range between AILT and AIHT before an interrupt is generated. The ALS data channel used for the persistence filter is set by ALS_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0.
				VALUE / **CONSECUTIVE ADATA OUT OF RANGE TO INTERRUPT**
				0 / Every ALS cycle generates an interrupt
				1 / 1
				2 / 2
				3 / 3
				4 / 5
				5 / 10
				... / 5 × (APERS – 3)
				14 / 55
				15 / 60

Note(s):

1. Return to the Register Map (0x9A)

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Figure 56:
CFG8

Addr: 0x9B		CFG8		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	FIFO_THR	10	R/W	**FIFO Threshold.** Sets a threshold on the FIFO level that triggers the first FIFO buffer interrupt (FINT).
				VALUE / **FIFO_LVL**
				0 / 1
				1 / 8
				2 / 16
				3 / 32
5:0	Reserved	000000		

Note(s):

1. Return to the Register Map (0x9B)

Figure 57:
CFG9

Addr: 0x9C		CGF9		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	SIEN_FD	0	R/W	**System Interrupt Flicker Detection.** Enables system interrupt when flicker detection status change has occurred.
5:0	Reserved	000000		

Note(s):

1. Return to the Register Map (0x9C)

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Figure 58:
CFG10

Addr: 0x9D		CFG10		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	ALS_AGC_HIGH_HYST	11	R/W	**ALS AGC High Hysteresis.** Sets the ALS data threshold at which AGAIN is reduced when ALS AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to (ATIME + 1) × (ASTEP + 1).
				VALUE / **SIGNAL**
				0 / 50%
				1 / 62.5%
				2 / 75%
				3 / 87.5%
5:4	ALS_AGC_LOW_HYST	11	R/W	**ALS AGC Low Hysteresis.** Sets the ALS data threshold at which AGAIN is increased when ALS AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to (ATIME + 1) × (ASTEP + 1).
				VALUE / **SIGNAL**
				0 / 12.5%
				1 / 25%
				2 / 37.5%
				3 / 50%
3:0	Reserved	0010		

Note(s):

1. Return to the Register Map (0x9D)

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Figure 59:
CFG11

Addr: 0x9E		CFG11		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	AINT_DIRECT	0	R/W	**ALS Interrupt Direct.** Enables the direct mode of ALS interrupt. The status of the ALS interrupt is directly output on the INT pin if this mode is enabled and the pin is configured to do so according to the INT_PINMAP setting.
6	PINT_DIRECT	1	R/W	**Proximity Interrupt Direct.** If asserted, the proximity interrupt has a hysteresis loop built into the interrupt. After setting PEN = 1, the device interrupts once PDATA is below PILT or above PIHT. After this initial interrupt, the device will then interrupt based on the direction that the PDATA changes relative to each threshold. An interrupt is generated when PDATA increases from below to above PIHT to indicate a Detect condition, and an interrupt is generated when PDATA decreases from above to below PILT to indicate a Release condition. With built-in hysteresis, it is no longer necessary to change the thresholds between Detect or Release interrupts. This bit applies to PINT0 and PINT1 by using PDATA0 and PDATA1 respectively, as well as the respective thresholds.
5:0	Reserved	000000		

Note(s):

1. Return to the Register Map (0x9E)

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Figure 60:
CFG12

Addr: 0x9F		CFG12				
Bit	**Field**	**Reset**	**Type**	**Bit Description**		
7:3	Reserved	00000				
2:0	ALS_TH_CHANNEL	000	R/W	**ALS Thresholds Channel.** Sets the channel used for interrupts and persistence if enabled, to determine device status and ALS gain settings.		
				VALUE	**CHANNEL**	**DEFAULT**
				0	0	CLEAR
				1	1	RED
				2	2	GREEN
				3	3	BLUE
				4	4	LEAKAGE
				5	5	WIDEBAND
				6	6	IR1
				7	7	IR2

Note(s):

1. Return to the Register Map (0x9F)

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ALS autozero configuration is used to set how often the ALS engine offsets are reset to compensate for changes in device temperature.

Figure 61:
AZ_CONFIG

Addr: 0xA4		AZ_CONFIG		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	AZ_NTH_ITERATION	0xFF	R/W	**ALS Autozero Frequency.** Sets the frequency at which the device performs autozero of the ALS pulse counter.

VALUE	AUTOZERO FREQUENCY
0	Never
1	Every cycle
2	Every 2 cycles
...	Every *(AZ_NTH_ITERATION)* cycles
253	Every 253 cycles
254	Every 254 cycles
255	Only once (before 1st cycle)

Note(s):

1. Return to the Register Map (0xA4)

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Figure 62:
CFG20

Addr: 0xA7		CFG20		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4	FLICKER_FIFO_MODE	0	R/W	**Flicker FIFO Mode.**
3:0	Reserved	0000		

Note(s):

1. Return to the Register Map (0xA7)

Figure 63:
PCFG1

Addr: 0xAA		PCFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	HXTALK_MODE2	0	R/W	**High Crosstalk Mode.** If asserted, the proximity engine uses a 10-bit output mode for no aperture proximity operation intended for extremely high optical crosstalk systems. HXTALK_MODE1 and HXTALK_MODE2 must both be asserted for this function to work.
6:4	Reserved	000		
3	PROX_FILTER_DOWNSAMPLE	0	R/W	**Proximity Filter Down Sample.** Sets how often proximity results are checked for interrupts and persistence when PROX_FILTER is enabled.
2:0	PROX_FILTER	000	R/W	**Proximity Filter.** Selects the filter size for proximity, *n*. The average is a moving window of length *n*, and the result is updated and used either every cycle (PROX_FILTER_DOWNSAMPLE = 0) or every *n* cycles (PROX_FILTER_ DOWNSAMPLE = 1).

VALUE	FILTER LENGTH
0	1
1	2
...	PROX_FILTER + 1
6	7
7	8

Note(s):

1. Return to the Register Map (0xAA)

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Figure 64:
PCFG2

Addr: 0xAB		PCFG2			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:6	ISINK_RELEASE	00	R/W	**Current Sink Release Scaler.** Current sink scaler used during release setting.	
				VALUE	**SCALER**
				0	0.5
				1	1
				2	1.5
				3	2
5:4	ISINK_DETECT	00	R/W	**Current Sink Detect Scaler.** Current sink scaler used during detect setting.	
				VALUE	**SCALER**
				0	0.5
				1	1
				2	1.5
				3	2
3:0	ILEDS2_SINK2 (2)	0000	R/W	Current Sink Slave Two.	
				VALUE	**CURRENT**
				0	0 mA
				...	*n* mA
				7	7 mA

Note(s):

1. Return to the Register Map (0xAB)
2. The maximum value setting is limited to a maximum of 7.

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Figure 65:
PCFG3

Addr: 0xAC		PCFG3			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:4	ILEDS1_SINK1 (2)	0	R/W	Current Sink Slave One.	
				VALUE	**CURRENT**
				0	0 mA
				...	*n* mA
				7	7 mA
3:0	ILEDM0_SINK0 (2)	0	R/W	Current Sink Master Zero.	
				VALUE	**CURRENT**
				0	1 mA
				...	*n+1* mA
				7	8 mA

Note(s):

1. Return to the Register Map (0xAC)
2. The maximum value setting is limited to a maximum of 7.

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Figure 66:
PCFG4

Addr: 0xAD		PCFG4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0000		
3:2	PGAIN1	10	R/W	Proximity Gain One. Sets the gain for proximity engine one. **VALUE** / **PROXIMITY GAIN** 0 / 1x 1 / 2x 2 / 4x 3 / 8x
1:0	PGAIN0	10	R/W	Proximity Gain Zero. Sets the gain for proximity engine zero. **VALUE** / **PROXIMITY GAIN** 0 / 1x 1 / 2x 2 / 4x 3 / 8x

Note(s):

1. Return to the Register Map (0xAD)

Figure 67:
PCFG5

Addr: 0xAE		PCFG5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	PPULSE	0x0F	R/W	**Proximity Pulse Count.** Specifies the maximum number of proximity pulses per sample. The number of pulses is equal to PPULSE + 1. The pulse count can be set between 1 and 256 pulses.

Note(s):

1. Return to the Register Map (0xAE)

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Figure 68:
PCFG6

Addr: 0xAF		PCFG6		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	PDATA_EVAL_CH	0	R/W	**Proximity Evaluation Channel.** This bit selects which channel is used for the proximity baseline calculation. If set to 0 then PDATA0 is used, if set to 1 then PDATA1 is used.
6:4	Reserved	000		
3	PDATA1_H_AND	0	R/W	**Proximity One High Threshold And.** If set to 1 then the high threshold of PDATA1 is seen as an AND for the proximity interrupt.
2	PDATA1_L_AND	0	R/W	**Proximity One Low Threshold And.** If set to 1 then the low threshold of PDATA1 is seen as an AND for the proximity interrupt.
1	PDATA0_H_AND	0	R/W	**Proximity Zero High Threshold And.** If set to 1 then the high threshold of PDATA0 is seen as an AND for the proximity interrupt.
0	PDATA0_L_AND	0	R/W	**Proximity Zero Low Threshold And.** If set to 1 then the low threshold of PDATA0 is seen as an AND for the proximity interrupt.

Note(s):

1. Return to the Register Map (0xAF)

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Figure 69:
PCFG7

Addr: 0xB0		PCFG7		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4	PROX_PRE_FILTER	0	R/W	**Proximity Pre-Filter.** When this bit is set, the 2 most recent proximity integrations will be combined and PDATA will be ~2x the value of a single integration when this bit is not set.
3	Reserved	0		
2:0	PPULSE_LEN	001	R/W	**Proximity Pulse Length.** Sets the proximity pulse length.

VALUE	PULSE LENGTH
0	4µs
1	8µs
2	16µs
3	32µs
4	64µs
5	128µs
6	256µs
7	512µs

Note(s):

1. Return to the Register Map (0xB0)

Figure 70:
POFFSET0

Bits	Addr	Field	Reset	Type	Description
7:0	0xB1	POFFSET0	0x00	R/W	Proximity Offset Zero
15:8	0xB2		0x00	R/W	

Note(s):

1. Return to the Register Map (0xB1, 0xB2)

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Figure 71:
PXAVG

Bits	Addr	Field	Reset	Type	Description
7:0	0xB3	PXAVG	0x00	R/W	Proximity Average
15:8	0xB4		0x00	R/W	

Note(s):

1. Return to the Register Map (0xB3, 0xB4)

Figure 72:
PBSLN

Bits	Addr	Field	Reset	Type	Description
7:0	0xB5	PBSLN	0x00	R/W	Proximity Baseline
15:8	0xB6		0x00	R/W	

Note(s):

1. Return to the Register Map (0xB5, 0xB6)

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Status Registers

The primary status register for TMD3719 indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a 1 to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s), then write the register value back to STATUS to clear the handled events. Writing 0 to these bits will not clear those bits if they have a value of 1, which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared.

Figure 73:
STATUS

Addr: 0xB7		STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ASAT	0	R	**ALS Saturation.** If ASIEN is set, indicates ALS saturation. Check the STATUS3 register to differentiate between analog or digital saturation.
6	FDSAT	0	R	**Flicker Detection Saturation.** If FDSIEN is set, indicates Flicker Detection saturation. Check the STATUS4 register to differentiate between analog or digital saturation.
5	PSAT	0	R	**Proximity Saturation.** If PSIEN is set, indicates analog saturation during a previous proximity cycle. Check the STATUS2 register to differentiate between ambient or reflected light saturation.
4	PINT	0	R	**Proximity Interrupt One.** If PIEN is set, indicates that a proximity detect or release event that met the programmed proximity thresholds and persistence occurred.
3	AINT	0	R	**ALS Interrupt.** If AIEN is set, indicates that an ALS event that met the programmed ALS thresholds and persistence occurred.
2	FINT	0	R	**FIFO Buffer Interrupt.** If FIEN is set, indicates that the FIFO_LVL fulfills the threshold condition. If cleared by writing 1, the interrupt will be asserted again as more data is collected. To fully clear this interrupt, all data must be read from the FIFO buffer.
1	CINT	0	R	**Calibration Interrupt.** If CIEN is set, indicates that either calibration is finished or that one of certain events have occurred during normal operation. If each function is enabled, CINT will be asserted if too many zeros occur too often in a period of samples, if the proximity baseline has decreased, or if at least one offset register has been adjusted. Check the CALIBSTAT register to identify the triggering event(s).
0	SINT	0	R	**System Interrupt.** If SIEN is set, indicates that one or more of several events has occurred or is complete. The events related to this interrupt are indicated in the STATUS5 register (0xBB): flicker detection register status has changed.

Note(s):

1. Return to the Register Map (0xB7)

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Additional status registers indicate details about saturation, interrupts, and device execution.

Figure 74:
STATUS2

Addr: 0xB8		STATUS2		
Bit	Field	Reset	Type	Bit Description
7	PVALID	0	R	**Proximity Valid.** Indicates that the proximity state has completed a cycle since either an assertion of PEN or the last readout of PDATA.
6	AVALID	0	R	**ALS Valid.** Indicates that the ALS state has completed a cycle since either an assertion of AEN or the last readout of the ASTATUS register.
5	PSAT1_ADC	0	R	**Proximity One ADC Saturation.** Indicates that the maximum proximity ADC value has occurred for proximity channel one during proximity measurement.
4	PSAT1_ REFLECTIVE	0	R	**Proximity One Reflective Saturation.** Indicates that the intensity of reflected light has exceeded the maximum integration level for the proximity analog circuit for channel one during proximity measurement.
3	PSAT1_ AMBIENT	0	R	**Proximity One Ambient Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the proximity analog circuit for channel one during proximity measurement.
2	PSAT0_ADC	0	R	**Proximity Zero ADC Saturation.** Indicates that the maximum proximity ADC value has occurred for proximity channel zero during proximity measurement.
1	PSAT0_ REFLECTIVE	0	R	**Proximity Zero Reflective Saturation.** Indicates that the intensity of reflected light has exceeded the maximum integration level for the proximity analog circuit for channel zero during proximity measurement.
0	PSAT0_ AMBIENT	0	R	**Proximity Zero Ambient Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the proximity analog circuit for channel zero during proximity measurement.

Note(s):

1. Return to the Register Map (0xB8)

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Figure 75:
STATUS3

Addr: 0xB9		STATUS3		
Bit	Field	Reset	Type	Bit Description
7	ASAT7_ANALOG	0	R	**ALS Channel Seven Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel seven analog circuit.
6	ASAT6_ANALOG	0	R	**ALS Channel Six Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel six analog circuit.
5	ASAT5_ANALOG	0	R	**ALS Channel Five Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel five analog circuit.
4	ASAT4_ANALOG	0	R	**ALS Channel Four Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel four analog circuit.
3	ASAT3_ANALOG	0	R	**ALS Channel Three Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel three analog circuit.
2	ASAT2_ANALOG	0	R	**ALS Channel Two Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel two analog circuit.
1	ASAT1_ANALOG	0	R	**ALS Channel One Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel one analog circuit.
0	ASAT0_ANALOG	0	R	**ALS Channel Zero Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS channel zero analog circuit.

Note(s):

1. Return to the Register Map (0xB9)

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Figure 76:
STATUS4

Addr: 0xBA		STATUS4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	OSCCAL_SAT	0	R	Oscillator Calibration Saturation.
6	Reserved	0		
5	OSCCAL_FINISHED	0	R	Oscillator Calibration Finished.
4	FD_SAT_DETECTED	0	R	**Flicker Saturation Detected.** Indicates that saturation occurred during the last flicker detection measurement, and the result may not be valid. Write 1 to this bit to clear this field.
3	FD_BUSY	0	R	**Flicker Detection Busy.** Indicates flicker detection is in progress.
2	FD_TRIG_ERROR	0	R	**Flicker Detect Trigger Error.** Indicates that there is a timing error that prevents flicker detect from functioning correctly.
1	PROX_TRIG_ERROR	0	R	**Proximity Trigger Error.** Indicates that there is a timing error that prevents proximity from functioning correctly. The number of pulses and/or pulse length are too long for the PTIME configured for the device.
0	MOD_TRIG_ERROR	0	R	**Modulator Trigger Error.** Indicates that there is a timing error that prevents ALS from functioning correctly. The WTIME is too short for the ATIME configured for the device.

Note(s):

1. Return to the Register Map (0xBA)

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Figure 77:
STATUS5

Addr: 0xBB		STATUS5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0000		
3	SINT_FD	0	R	**Flicker Detect Interrupt.** If SIEN_FD is set, indicates that the FD_STATUS register status has changed.
2:1	Reserved	00		
0	SINT_SYNC_ERROR	0	R	**Synchronization Error Interrupt.** If SINT_SYNC_ERROR is set, indicates there was a synchronization error.

Note(s):

1. Return to the Register Map (0xBB)

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Figure 78:
STATUS7

Addr: 0xBD		STATUS7		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	AINT_AIHT	0	R	**ALS Interrupt High.** Indicates that an ALS interrupt occurred because the ALS data exceeded the high threshold.
6	AINT_AILT	0	R	**ALS Interrupt Low.** Indicates that an ALS interrupt occurred because the ALS data is below the low threshold.
5:4	Reserved	00		
3	PINT1_PIHT	0	R	**Proximity One Interrupt High.** Indicates that a proximity one interrupt occurred because the proximity one data exceeded the high threshold.
2	PINT1_PILT	0	R	**Proximity One Interrupt Low.** Indicates that a proximity one interrupt occurred because the proximity one data is below the low threshold.
1	PINT0_PIHT	0	R	**Proximity Zero Interrupt High.** Indicates that a proximity zero interrupt occurred because the proximity zero data exceeded the high threshold.
0	PINT0_PILT	0	R	**Proximity Zero Interrupt Low.** Indicates that a proximity zero interrupt occurred because the proximity zero data is below the low threshold.

Note(s):

1. Return to the Register Map (0xBD)

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Figure 79:
STATUS8

Addr: 0xBE		STATUS8		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	00		
5	FVALID	0	R	**Flicker Data Valid.** Indicates that the flicker detection has completed a cycle since assertion of FDEN or since the last readout of the FSTATUS register.
4	Reserved	0		
3	SYNC_LOST	0	R	**Synchronization Lost.** Indicates when synchronization of VSYNC is lost.
2	Reserved	0		
1	SAI_ACTIVE	0	R	**Sleep After Interrupt Active.** Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit.
0	INIT_BUSY	0	R	**Initialization Busy.** Indicates that the device is initializing. This bit will remain 1 for about 300µs after power on. Do not interact with the device until initialization is complete.

Note(s):

1. Return to the Register Map (0xBE)

Figure 80:
STATUS9

Addr: 0xBF		STATUS9		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0000		
3	SYNC_ERROR	0	R	**Synchronization Error**
2:0	Reserved	000		

Note(s):

1. Return to the Register Map (0xBF)

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Figure 81:
ASTATUS

Addr: 0xC0		ASTATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:1	Reserved	0000000		
0	ASAT_STATUS	0	R	**ALS Saturation Status.** Indicates if the latched ALS data is affected by analog or digital saturation.

Note(s):

1. Return to the Register Map (0xC0)

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Figure 82:
ALS Data Registers

Bits	Addr	Field	Reset	Type	Description
7:0	0xC1	ADATA0	0x00	R	**ALS Channel Zero Data.** CLEAR data
15:8	0xC2		0x00	R	
23:16	0xC3		0x00	R	
7:0	0xC4	ADATA1	0x00	R	**ALS Channel One Data.** RED data
15:8	0xC5		0x00	R	
23:16	0xC6		0x00	R	
7:0	0xC7	ADATA2	0x00	R	**ALS Channel Two Data.** GREEN data
15:8	0xC8		0x00	R	
23:16	0xC9		0x00	R	
7:0	0xCA	ADATA3	0x00	R	**ALS Channel Three Data.** BLUE data
15:8	0xCB		0x00	R	
23:16	0xCC		0x00	R	
7:0	0xCD	ADATA4	0x00	R	**ALS Channel Four Data.** LEAKAGE data
15:8	0xCE		0x00	R	
23:16	0xCF		0x00	R	
7:0	0xD0	ADATA5	0x00	R	**ALS Channel Five Data.** WIDEBAND data
15:8	0xD1		0x00	R	
23:16	0xD2		0x00	R	
7:0	0xD3	ADATA6	0x00	R	**ALS Channel Six Data.** IR1 data
15:8	0xD4		0x00	R	
23:16	0xD5		0x00	R	
7:0	0xD6	ADATA7	0x00	R	**ALS Channel Seven Data.** IR2 data
15:8	0xD7		0x00	R	
23:16	0xD8		0x00	R	

Note(s):

1. Return to the Register Map (0xC1, 0xC2, 0xC3, 0xC4, 0xC5, 0xC6, 0xC7, 0xC8, 0xC9, 0xCA, 0xCB, 0xCC, 0xCD, 0xCE, 0xCF, 0xD0, 0xD1, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, 0xD8).

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Figure 83:
PSTATUS

Addr: 0xD9		PSTATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	SMUX_PRX_MS_STAT	0	R	SMUX Proximity Mode Select Status.
5:0	PSAT_STATUS	000000	R	**Proximity Saturation Status.** Indicates if the latched proximity data is affected by analog or digital saturation.

Note(s):

1. Return to the Register Map (0xD9)

Figure 84:
Proximity Data

Bits	Addr	Field	Reset	Type	Description
7:0	0xDA	PDATA0	0x00	R	Proximity Data Zero
15:8	0xDB		0x00	R	
7:0	0xDC	PDATA1	0x00	R	Proximity Data One
15:8	0xDD		0x00	R	
7:0	0xDE	PDATAR	0x00	R	Proximity Data Ratio
15:8	0xDF		0x00	R	

Note(s):

1. Return to the Register Map (0xDA, 0xDB, 0xDC, 0xDD, 0xDE, 0xDF)

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Figure 85:
GPIO

Addr: 0xF2		GPIO		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	00		
5	INT_INVERT	0	R/W	**Interrupt Invert.** If asserted, the output on interrupt pin is inverted. This is useful for direct interrupt output if active = high.
4	INT_IN_EN	0	R/W	**Interrupt Input Enable.** If asserted, the interrupt pin can be used as an input.
3	GPIO_INVERT	0	R/W	**GPIO Invert.** If asserted, the output on GPIO is inverted. This is useful for direct interrupt output if active = high.
2	GPIO_IN_EN	0	R/W	**GPIO Input Enable.** If asserted, the GPIO pin accepts a non-floating input.
1	GPIO_OUT	1	R/W	**GPIO Output.** If asserted, the output state of the GPIO is active directly.
0	GPIO_IN	0	R/W	**GPIO Input.** Indicates the status of the GPIO input if GPIO_IN_EN is asserted.

Note(s):

1. Return to the Register Map (0xF2)

Figure 86:
AGC_GAIN_MAX

Addr: 0xF4		AGC_GAIN_MAX		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	00000		
2:0	AGC_MOD_GAIN_MAX	110	R/W	**AGC Modulator Gain Max.** Sets the maximum modulator gain for the AGC engine.

Note(s):

1. Return to the Register Map (0xF4)

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Figure 87:
INTENAB

Addr: 0xF5		INTENAB		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ASIEN	0	R/W	**ALS Saturation Interrupt Enable.** When asserted permits ALS saturation interrupts to be generated.
6	FDSIEN	0	R/W	**Flicker Detect Saturation Interrupt Enable.** When asserted permits flicker detection saturation interrupts to be generated.
5	PSIEN	0	R/W	**Proximity Saturation Interrupt Enable.** When asserted permits proximity saturation interrupts to be generated.
4	PIEN	0	R/W	**Proximity Interrupt Enable.** When asserted permits proximity interrupts to be generated, subject to the proximity thresholds and persistence filter.
3	AIEN	0	R/W	**ALS Interrupt Enable.** When asserted permits ALS interrupts to be generated, subject to the ALS thresholds and persistence filter. Bit is mirrored in the ENABLE register.
2	FIEN	0	R/W	**FIFO Buffer Interrupt Enable.** When asserted permits interrupt to be generated when FIFO_LVL exceeds the FIFO threshold condition.
1	CIEN	0	R/W	**Calibration Interrupt Enable.** When asserted permits calibration interrupts to be generated.
0	SIEN	0	R/W	**System Interrupt Enable.** When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed.

Note(s):

1. Return to the Register Map (0xF5)

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Figure 88:
CONTROL

Addr: 0xF6		CONTROL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	00000		
2	ALS_MANUAL_AZ	0	R/W	**ALS Manual Autozero.** Starts a manual autozero of the ALS engines. Set AEN = 0 before starting a manual autozero for it to work.
1	FIFO_CLR	0	R/W	**FIFO Buffer Clear.** Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL.
0	CLEAR_SAI_ACTIVE	0	R/W	**Clear Sleep-After-Interrupt Active.** Clears SAI_ACTIVE, ends sleep, and restarts device operation.

Note(s):

1. Return to the Register Map (0xF6)

Figure 89:
POFFSET1

Bits	Addr	Field	Reset	Type	Description
7:0	0xF7	POFFSET1	0x00	R/W	Proximity Offset One
15:8	0xF8		0x00	R/W	

Note(s):

1. Return to the Register Map (0xF7, 0xF8)

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Figure 90:
FIFO_MAP

Addr: 0xF9		FIFO_MAP		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	FIFO_WRITE_ADATA7	0	R/W	**FIFO Write ALS Data Seven.** If asserted, ADATA7 is written to the FIFO Buffer.
6	FIFO_WRITE_ADATA6	0	R/W	**FIFO Write ALS Data Six.** If asserted, ADATA6 is written to the FIFO Buffer.
5	FIFO_WRITE_ADATA5	0	R/W	**FIFO Write ALS Data Five.** If asserted, ADATA5 is written to the FIFO Buffer.
4	FIFO_WRITE_ADATA4	0	R/W	**FIFO Write ALS Data Four.** If asserted, ADATA4 is written to the FIFO Buffer.
3	FIFO_WRITE_ADATA3	0	R/W	**FIFO Write ALS Data Three.** If asserted, ADATA3 is written to the FIFO Buffer.
2	FIFO_WRITE_ADATA2	0	R/W	**FIFO Write ALS Data Two.** If asserted, ADATA2 is written to the FIFO Buffer.
1	FIFO_WRITE_ADATA1	0	R/W	**FIFO Write ALS Data One.** If asserted, ADATA1 is written to the FIFO Buffer.
0	FIFO_WRITE_ADATA0	0	R/W	**FIFO Write ALS Data Zero.** If asserted, ADATA0 is written to the FIFO Buffer.

Note(s):

1. Return to the Register Map (0xF9)

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Figure 91:
FIFO_MAP2

Addr: 0xFA		FIFO_MAP2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	Reserved	000		
4	FIFO_WRITE_FD_RESULT	0	R/W	**FIFO Write Flicker Detection Result.** If asserted, flicker detection on-chip calculation result is written to the FIFO Buffer.
3	FIFO_WRITE_FD_DATA	0	R/W	**FIFO Write Flicker Detection Data.** If asserted, flicker detection data is written to the FIFO Buffer.
2	FIFO_WRITE_PDATAR	0	R/W	**FIFO Write Proximity Ratio Data.** If asserted, proximity ratio data is written to the FIFO Buffer.
1	FIFO_WRITE_PDATA1	0	R/W	**FIFO Write Proximity One Data.** If asserted, proximity one data is written to the FIFO Buffer.
0	FIFO_WRITE_PDATA0	0	R/W	**FIFO Write Proximity Zero Data.** If asserted, proximity zero data is written to the FIFO Buffer.

Note(s):

1. Return to the Register Map (0xFA)

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FIFO Buffer Data and Status

The FIFO buffer is used to poll proximity or ALS data with fewer I^2C read and write transactions. The FIFO buffer is 256 bytes of RAM. If the FIFO overflows (i.e. 129 datasets before host/system reads data from the FIFO buffer), an overflow flag will be set and new data will be lost. Host/Systems acquire data by reading addresses: 0xFC – 0xFF. The register address pointer automatically wraps from 0xFF to 0xFC as data are read. Data can be read one byte at a time or in blocks (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL update for each two byte entry. If the FIFO continues to be accessed after FIFO_LVL = 0, the device will return 0 for all data.

The FINT interrupt indicates when there is valid data in the FIFO buffer. The amount of unread data is indicated by the FIFO_LVL.

Figure 92:
FIFO_STATUS

Addr: 0xFB		FIFO_STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	FIFO_OV	0	R	**FIFO Buffer Overflow.** Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO buffer is read.
6:0	FIFO_LVL	0000000	R	**FIFO Buffer Level.** Indicates the number of entries (each are 4 bytes) available in the FIFO buffer waiting for readout. The FIFO RAM is 256byte (128 words) so the FIFO_LVL ranges from 0 entries to 64 entries.

Note(s):

1. Return to the Register Map (0xFB)

Figure 93:
FDATA

Bits	Addr	Field	Reset	Type	Description
7:0	0xFC	FDATA	0x00	R	FIFO Buffer Data
15:8	0xFD		0x00	R	
23:16	0xFE		0x00	R	
31:24	0xFF		0x00	R	

Note(s):

1. Return to the Register Map (0xFC, 0xFD, 0xFE, 0xFF)

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Application Information

Figure 94:
TMD3719 Typical Application Circuit

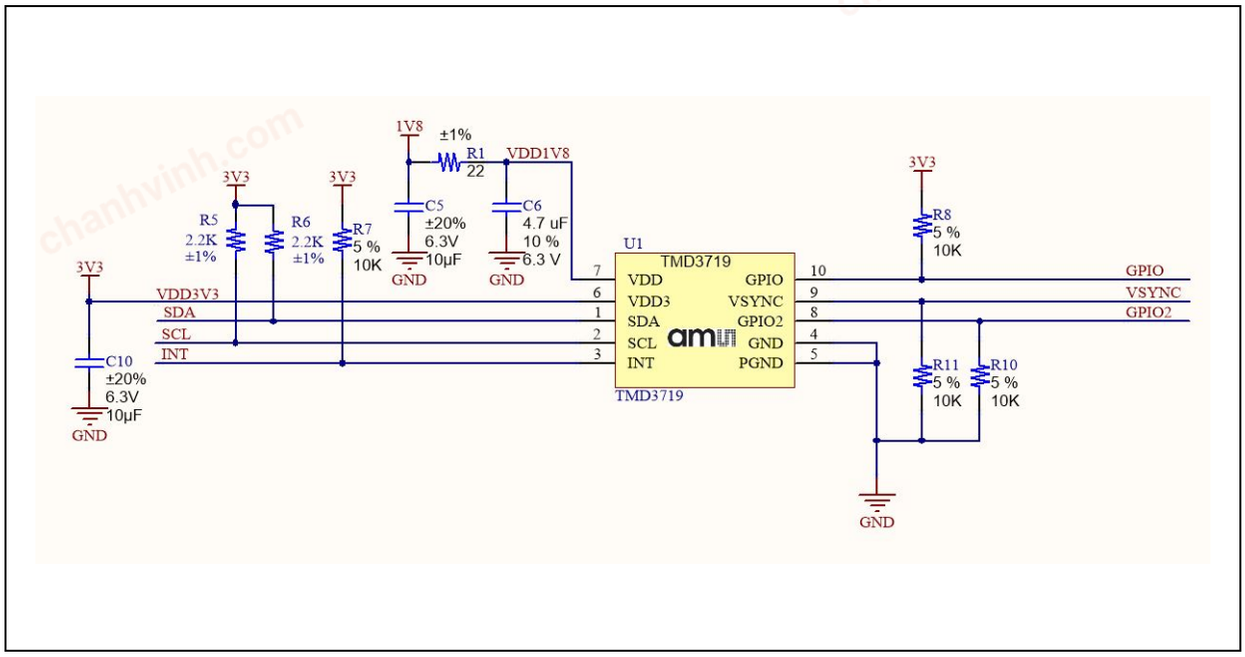
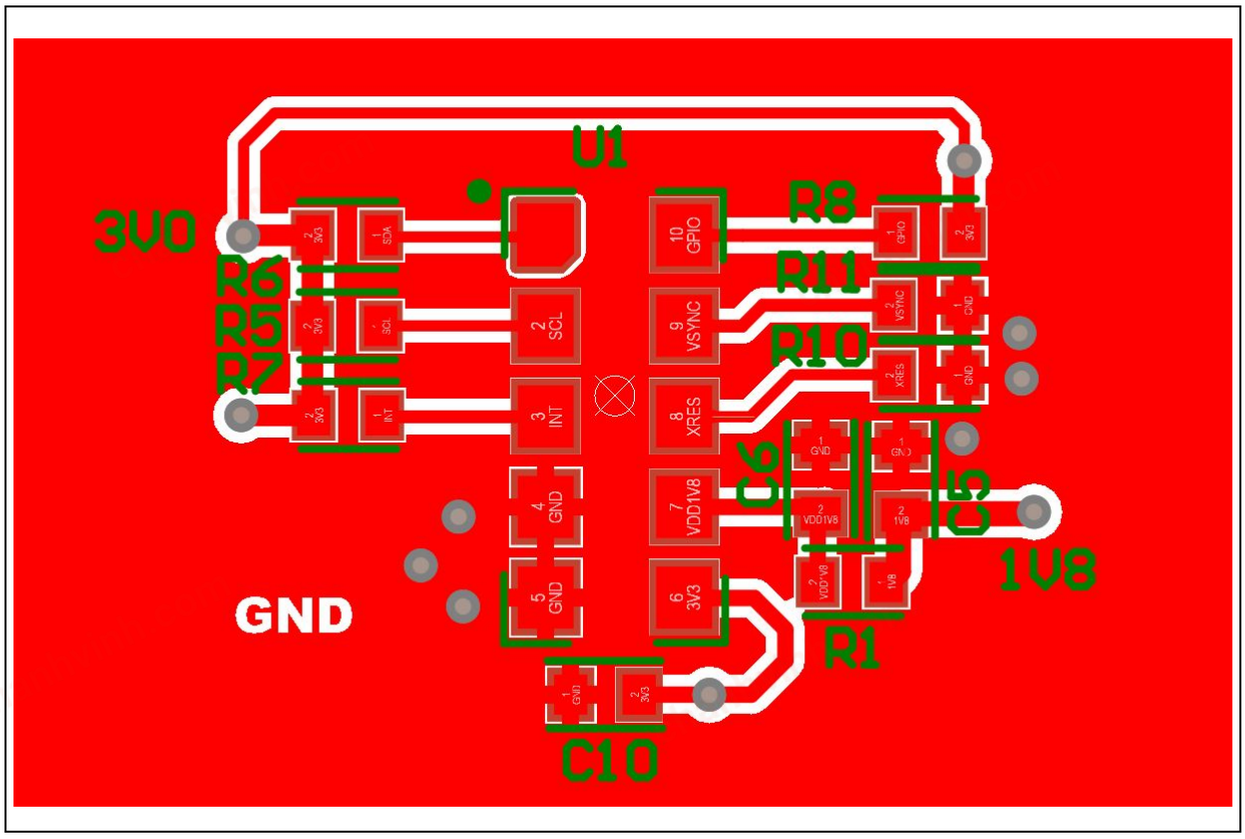


Figure 95:
TMD3719 Recommended Circuit Layout



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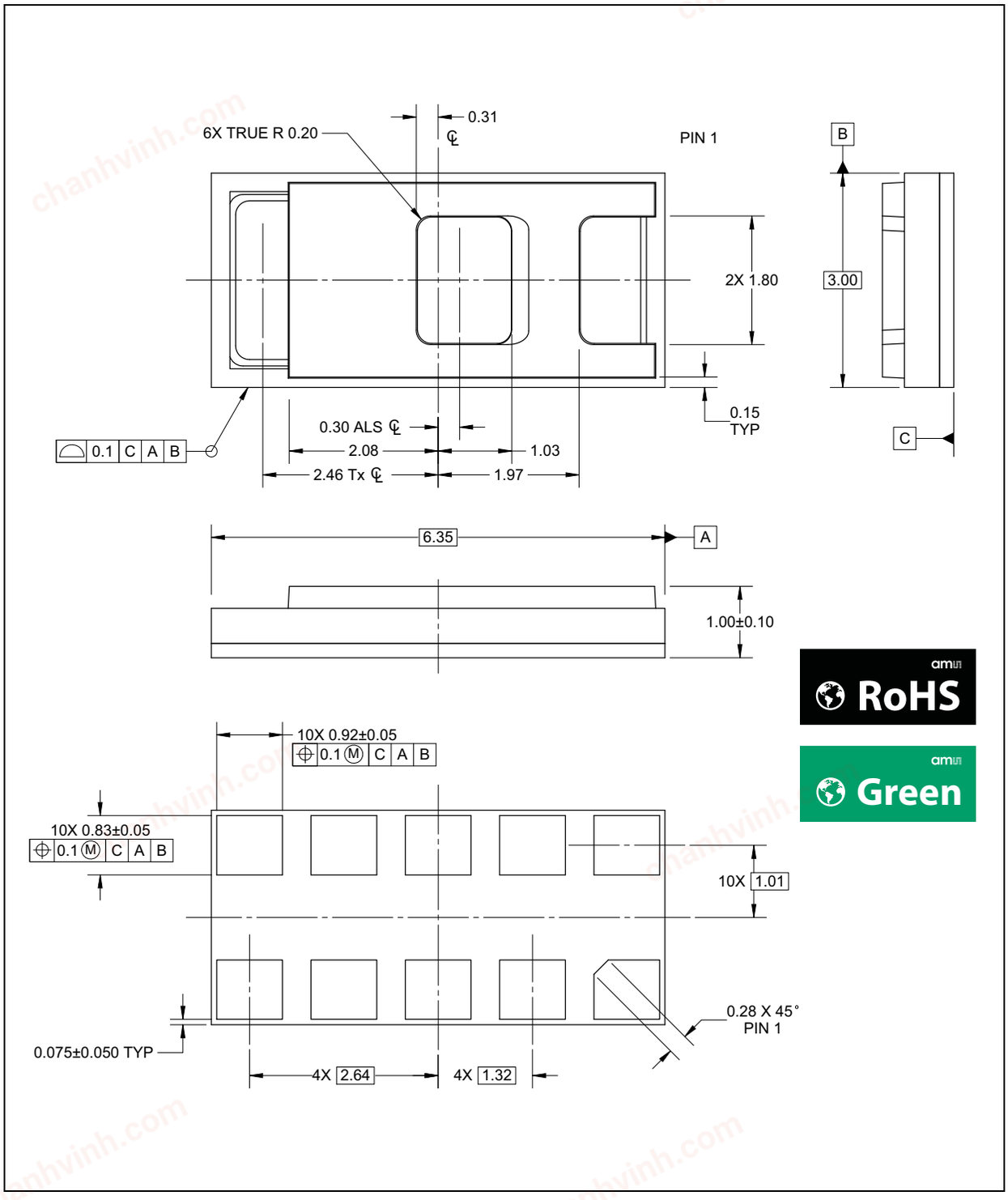
Package Drawings & Markings

Figure 96:
TMD3719 Module Dimensions



Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. Contacts are copper with NiPdAu plating.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.
6. Measurement guarantee by lot acceptance testing using 20 units.

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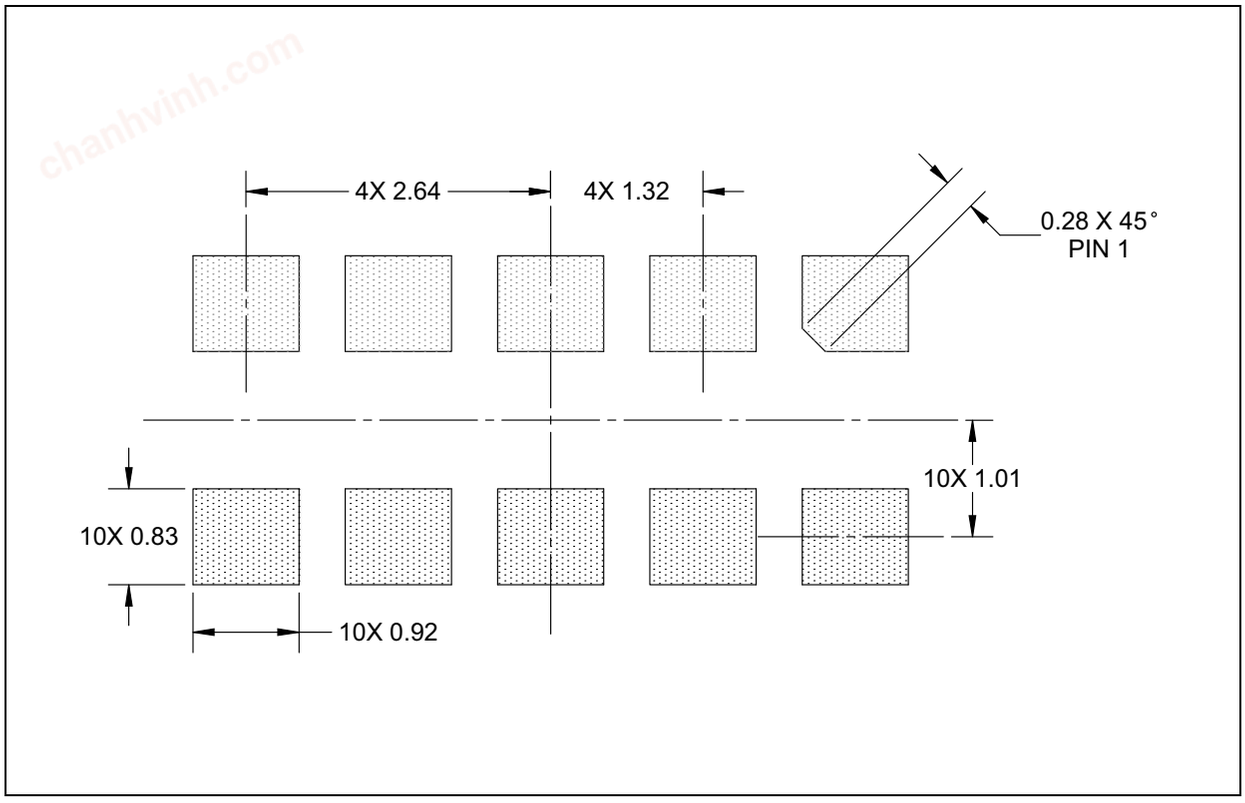
PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 97:
Recommended PCB Pad Layout



Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

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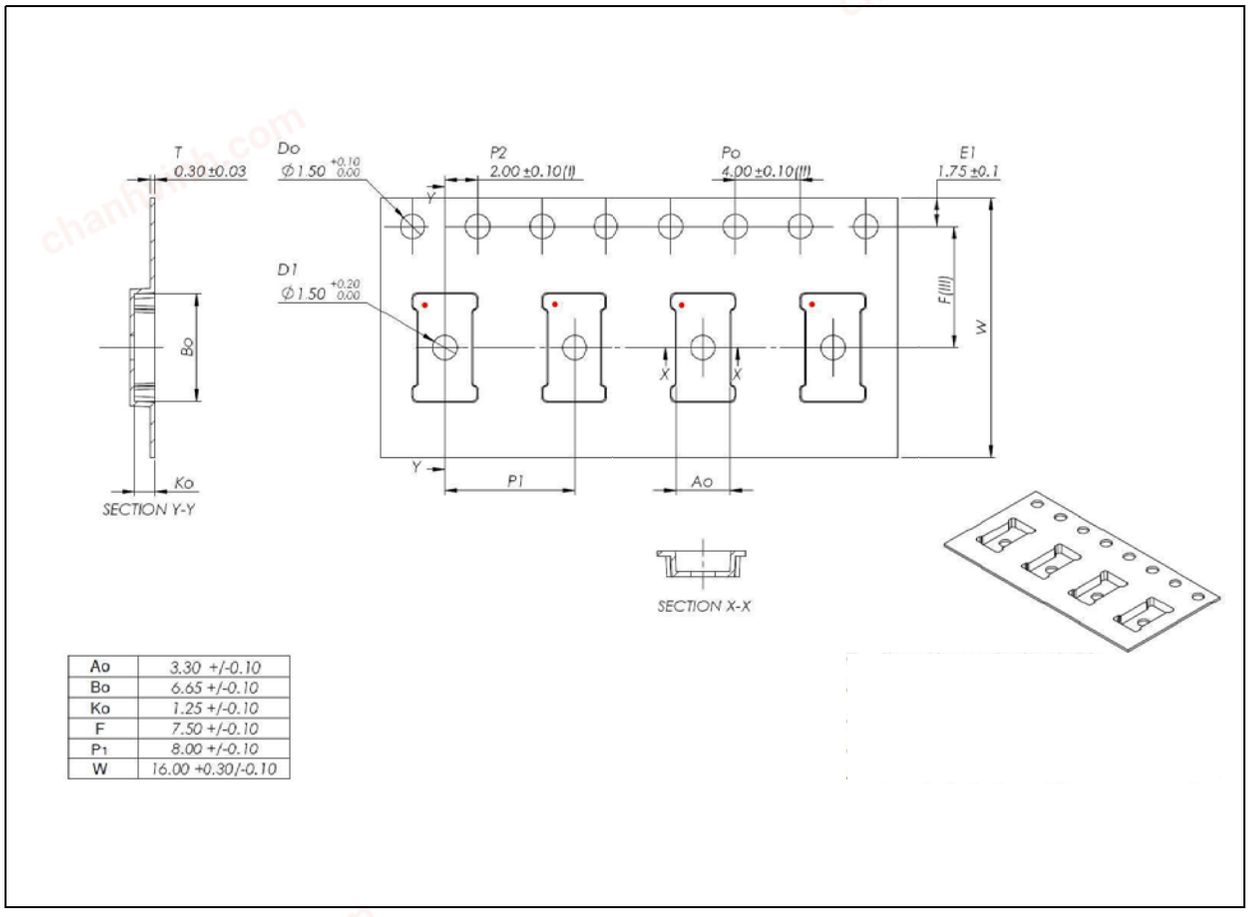
Tape & Reel Information

Figure 98:
TMD3719 Tape and Reel Mechanical Drawing



Ao	3.30 +/-0.10
Bo	6.65 +/-0.10
Ko	1.25 +/-0.10
F	7.50 +/-0.10
P1	8.00 +/-0.10
W	16.00 +0.30/-0.10

Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is generally 330 millimeters in diameter and contains 10000 parts. Please reconfirm for actual orders.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

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Soldering & Storage Information

Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 99:
Solder Reflow Profile

Profile Feature Preheat/ Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100°C	150°C
Temperature Max (T_{smax})	150°C	200°C
Time (t_s) from (T_{smin} to T_{smax})	60s - 120s	60s-120s
Ramp-up rate (T_L to T_P)	max. 3°C/s	max. 3°C/s
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60s - 150s	217°C 60s - 150s
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp of 235°C. For suppliers T_P must equal or exceed the Classification temp of 235°C.	For users T_P must not exceed the Classification temp of 260°C. For suppliers T_P must equal or exceed the Classification temp of 260°C.
Time (t_P)(1) within 5°C of the specified classification temperature (T_c)	20(1) seconds	30(1) seconds
Ramp-down rate (T_P to T_L)	Max. 6°C/s	Max. 6°C/s
Time 25°C to peak temperature	Max. 6 minutes	Max. 8 minutes

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

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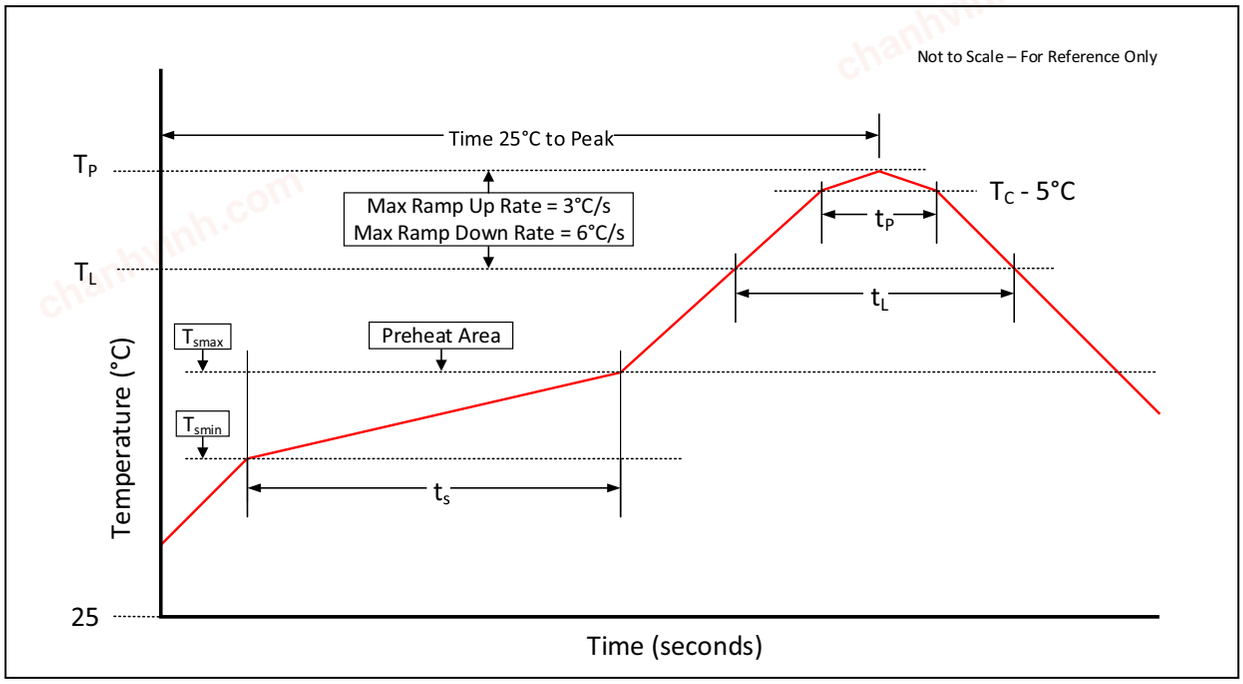
Figure 100:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

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Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

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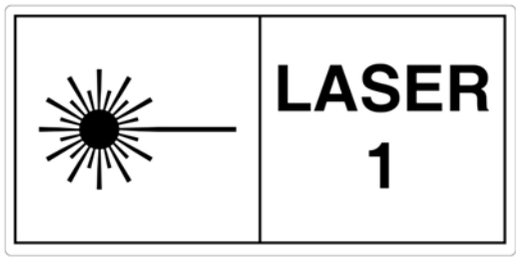
Laser Eye Safety

The TMD3719 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC 60825-1:2014. This applied to the stand-alone device. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions. Use outside of the recommended condition or any physical modification to the module during development could result in hazardous levels of radiation exposure.



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Ordering & Contact Information

Figure 101:
Ordering Information

Ordering Code	Address	Interface	Delivery Form	Delivery Quantity
TMD37193	0x39	1.8V I^2C	Tape & Reel	10000 pcs/reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
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Revision Information

Changes from 1-01 (2020-Aug-11) to current revision 1-03 (2020-Nov-20)	Page
1-01 (2020-Aug-11) to 1-02 (2020-Sep-11)	
Updated Figure 8	7
1-02 (2020-Sep-11) to 1-03 (2020-Nov-20)	
Updated Figure 9 and notes below	10
Updated Register Map (Status9)	18
Updated Figure 59	55
Added Status9 Register	71

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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