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# TMD2755

## ALS + Proximity Sensor Module

## General Description

The TMD2755 features proximity detection and digital ambient light sensing (ALS). The extremely narrow 1.1mm module incorporates an IR VCSEL and factory calibrated VCSEL driver. The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated VCSEL). Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features a wide range offset adjustment to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS and IR photodiodes have dedicated data converters producing 16-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control display backlight.

*Ordering Information and Content Guide appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of TMD2755, ALS + Proximity Sensor Module are listed below:

**Figure 1:**
**Added Value of Using TMD2755**

| Benefits | Features |
|---|---|
| • Optimized for narrow bezel mobile phones | • Small narrow 1.1mm x 3.25mm x 0.60mm module |
| • Reduced power consumption | • 1.8V power supply with 1.8V $I^2C$ bus<br>• Sleep mode (0.7µA)<br>• VCSEL IR emitter |
| • Enabled superior proximity detection | • Integrated factory calibrated 940nm IR VCSEL<br>• Crosstalk and ambient light cancellation<br>• Wide configuration range |
| • Accurate ambient light sensing | • High sensitivity<br>• 2 channels (photopic ALS + IR)<br>• Programmable gain and integration time |
| • Industrial design flexibility | • Offset emitter/detector package design |

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## Applications

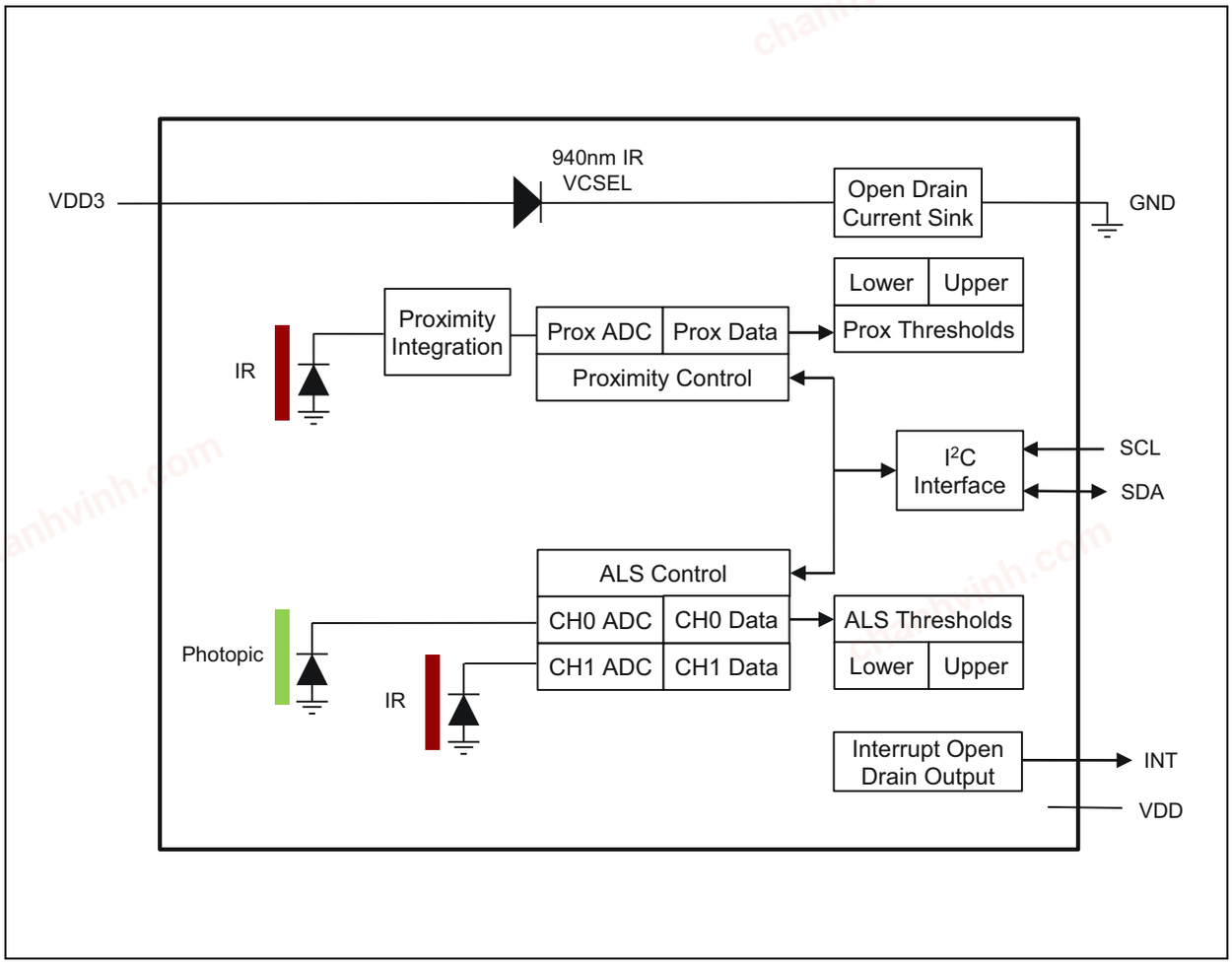
The TMD2755 applications include:

- Mobile phone display management
- Mobile phone user proximity detection

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**
**Functional Blocks of TMD2755**



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## Pin Assignments

Figure 3:
Pin Diagram

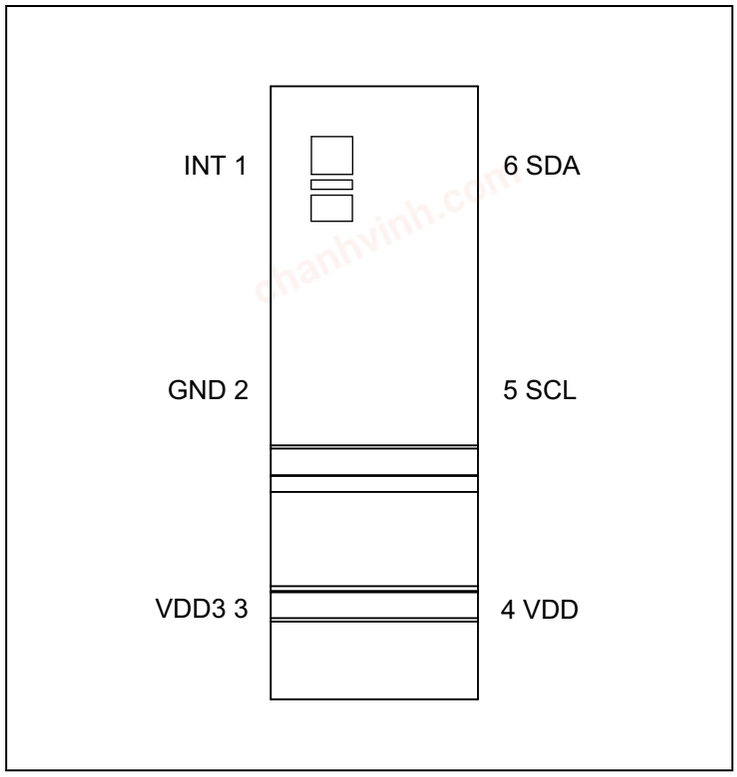



Figure 4:
Pin Description of TMD2755

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | INT | Interrupt. Open drain output (active low). If INT is not used, tie to GND for enhanced ESD protection. |
| 2 | GND | Ground. All voltages are referenced to GND. |
| 3 | VDD3 | Supply voltage for IR emitter (3.0/3.3V) |
| 4 | VDD | Supply voltage for sensor (1.8V). To enable the device to recover from a high voltage ESD strike, it is recommended to connect VDD to a host GPIO pin for independent power control. |
| 5 | SCL | $I^2C$ serial clock input terminal |
| 6 | SDA | $I^2C$ serial data I/O terminal |

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## Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**
**Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| **Electrical Parameters** | | | | | |
| VDD | Supply Voltage to GND | -0.3 | 1.98 | V | |
| VDD3 | IR Emitter Voltage to GND | -0.3 | 3.6 | V | |
| $V_{IO}$ | Digital I/O Terminal Voltage | -0.3 | 3.6 | V | |
| $I_{IO}$ | Digital Output Terminal Current | -1 | 20 | mA | |
| **Electrostatic Discharge** | | | | | |
| $I_{SCR}$ | Input Current (latch-up immunity) | ± 100 | | mA | Class II JEDEC JESD78E |
| $ESD_{HBM}$ | HBM Electrostatic Discharge | ± 2000 | | V | JEDEC/ESDA JS-001-2017 |
| $ESD_{CDM}$ | CDM Electrostatic Discharge | ± 500 | | V | JEDEC JS-002-2014 |
| **Temperature Ranges and Storage Conditions** | | | | | |
| $T_{STRG}$ | Storage Temperature Range | -40 | 85 | °C | |
| $T_{BODY}$ | Package Body Temperature | | 260 | °C | IPC/JEDEC J-STD-020<br>The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” |
| $RH_{NC}$ | Relative Humidity (non-condensing) | | 85 | % | |
| $P_{DISS}$ | Power Dissipation | | 50 | mW | Average power dissipation over a 1 second period |
| MSL | Moisture Sensitivity Level | 3 | | | Represents a max. floor life time of 168h |

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## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**
**Recommended Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD | Supply Voltage to Sensor | 1.7 | 1.8 | 1.98 | V |
| VDD3 | Supply Voltage to IR Emitter | 2.9 | 3.3 | 3.6 | V |
| $T_A$ | Operating Ambient Temperature | -30 | | 85 | °C |

**Note(s):**

1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

**Figure 7:**
**Operating Characteristics, VDD = 1.8V, $T_A$ = 25°C (unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | Oscillator Frequency | | 7.9 | 8.1 | 8.3 | MHz |
| $I_{DD}$ | Supply Current (1) | Active Proximity State (PON=1) (2) | | 360 | | µA |
| | | Active ALS State (PON=1) (2) | | 80 | | |
| | | Idle State (PON=1) (3) | | 35 | | |
| | | Sleep State (PON = 0) (4) | | 0.6 | | |
| $V_{OL}$ | INT, SDA Output Low Voltage | 6mA Sink Current | | | 0.6 | V |
| $I_{LEAK}$ | Leakage Current, SDA, SCL, INT | | -5 | | 5 | µA |
| $V_{IH}$ | SCL, SDA Input High Voltage (5) | | 1.26 | | | V |
| $V_{IL}$ | SCL, SDA Input Low Voltage | | | | 0.54 | V |
| $t_{Active}$ | Time from Power-On to Ready to Receive $I^2C$ Commands | | | 1.5 | | ms |

**Note(s):**

1. Values are shown at the VDD pin and do not include current through the IR VCSEL emitter.
2. Active state occurs when PON =1 and the device is actively integrating either proximity or ALS. For proximity, this time is determined by the number of pulses (PPLUSE) and the pulse length (PULSE_LEN). For ALS, this time is determined by the ALS integration time (ATIME). Both proximity and ALS active states can occur at the same time.
3. Idle state occurs when PON=1 and the device is not in the active state.
4. Sleep state occurs when PON = 0 and $I^2C$ bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
5. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.4V

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**Figure 8:**
**ALS Optical Characteristics (VDD = 1.8V, $T_A$ = 25°C unless otherwise noted)**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CH0 ALS Sensitivity | Warm White LED @ 8µW/cm$^2$<br>AGAIN = 128x<br>ATIME = 100ms | -15% | 2600 | +15% | Counts |
| | Warm White LED @ 8µW/cm$^2$<br>AGAIN = 1024x<br>ATIME = 100ms | | 21320 | | Counts |
| CH1 ALS Sensitivity | 940nm LED @ 21.1µW/cm$^2$<br>AGAIN = 128x<br>ATIME = 100ms | -20% | 1483 | +20% | Counts |
| | 940nm LED @ 21.1µW/cm$^2$<br>AGAIN = 1024x<br>ATIME = 100ms | | 12160 | | Counts |
| ALS Integration Step Size | | 2.68 | 2.78 | 2.90 | ms |
| ALS CH0 / CH1 Dark Count | 0µW/cm$^2$<br>AGAIN = 1024x<br>ATIME = 50ms | 0 | 1 | 2 | Counts |
| ALS 16x Gain Scaling | Relative to 128x | | 0.125 | | x |
| ALS 1024x Gain Scaling | Relative to 128x | | 8.2 | | x |

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**Figure 9:**
**Proximity Optical Characteristics (VDD = 1.8V, VDD3 = 3.0V, $T_A$ = 25°C unless otherwise noted)**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Response: Absolute (1) | PGAIN1 = 4x; PGAIN2 = 2.5x<br>PLDRIVE = 7mA<br>PPULSE = 2 pulses<br>PPULSE_LEN = 40µs<br>HW Averaging = 8<br>BINSRCH_TARGET = 15<br>APC = disabled<br>Post Calibration<br>Target material: 18% reflective surface<br>No glass above module<br>Target Size: 100mm x 100mm<br>Target Distance: 30mm | | 115 | | Counts |
| Part to Part Variation (3) | Same as Response: Absolute except target is 51mm diameter diffusor | | | ±25 | % |
| Response: No target (2) | Same as Response: Absolute except no target | 5 | 13 | 20 | Counts |

**Note(s):**

1. Representative result by characterization.
2. Response with no target varies with power supply characteristics and system noise.
3. At factory final test.

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# Typical Operating Characteristics

**Figure 10:**
**ALS Average Angular Response to 2700K White LED (pin 1 [-90°] to pin 3 [90°])**

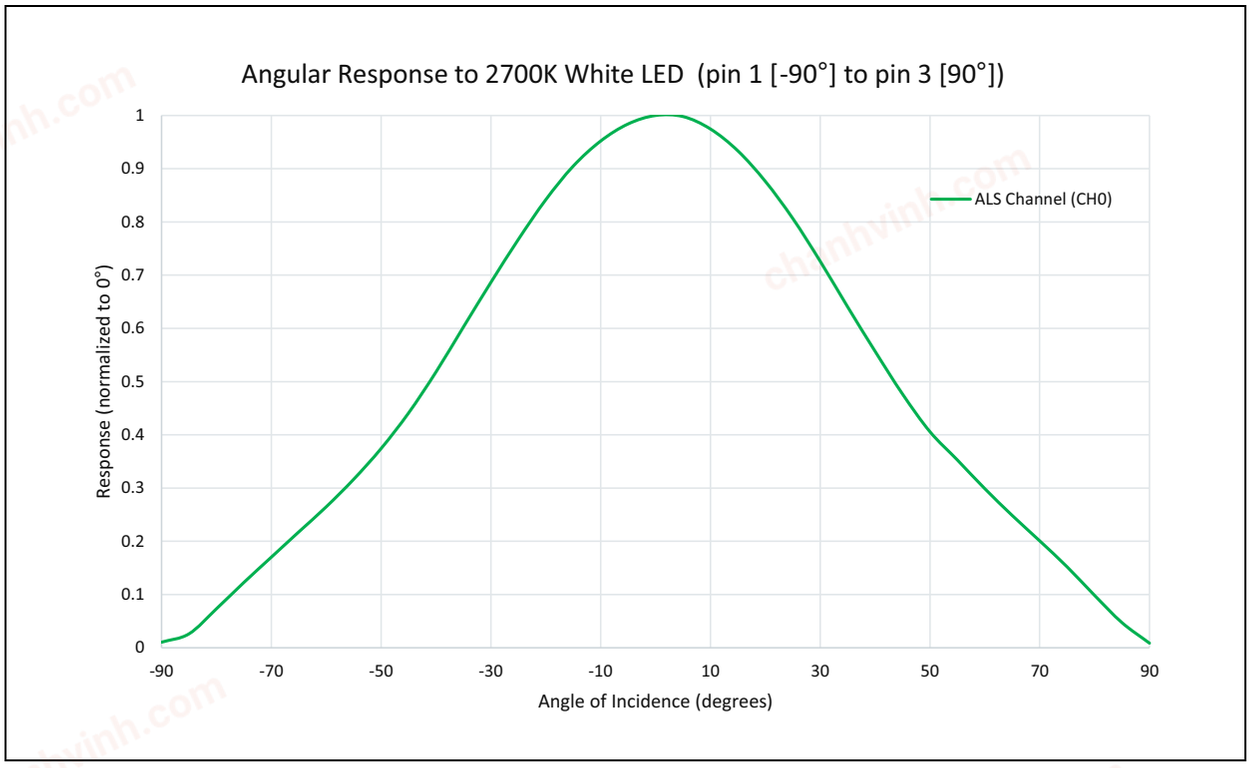
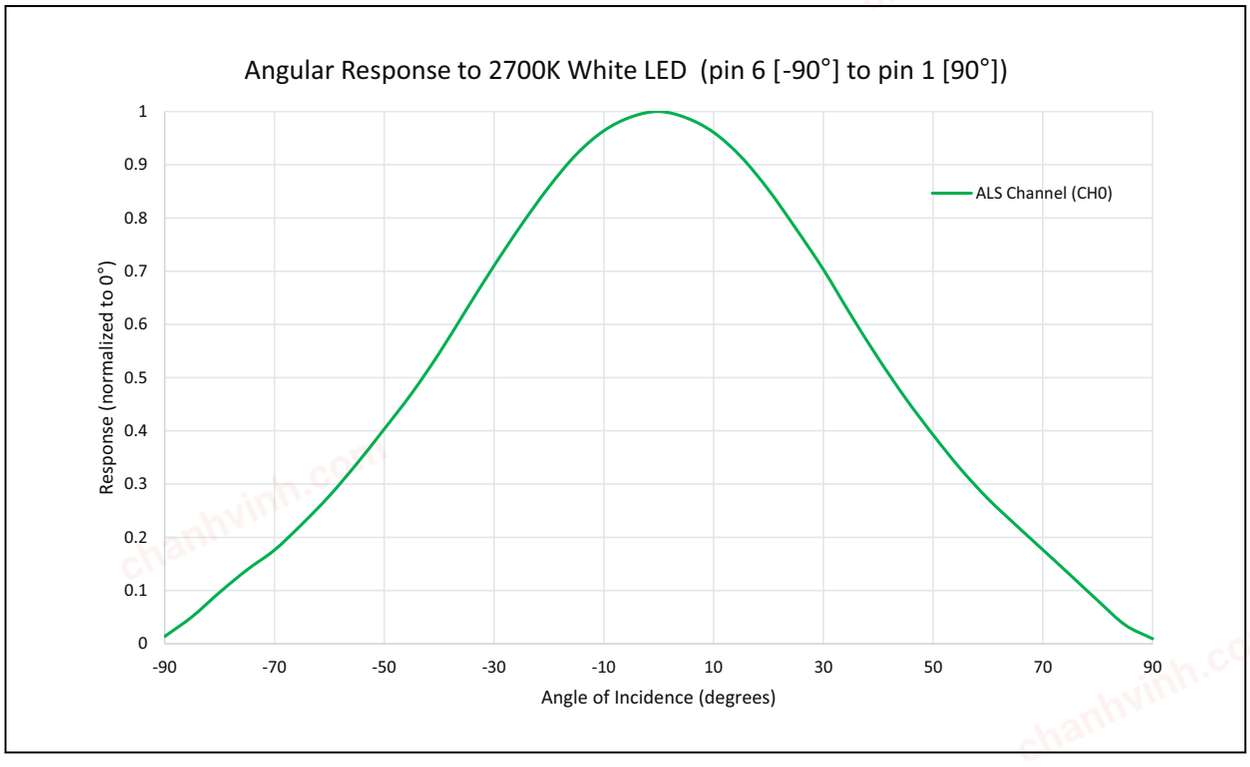



**Figure 11:**
**ALS Average Angular Response to 2700K White LED (pin 6 [-90°] to pin 1 [90°])**



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**Figure 12:**
**Spectral Responsivity**

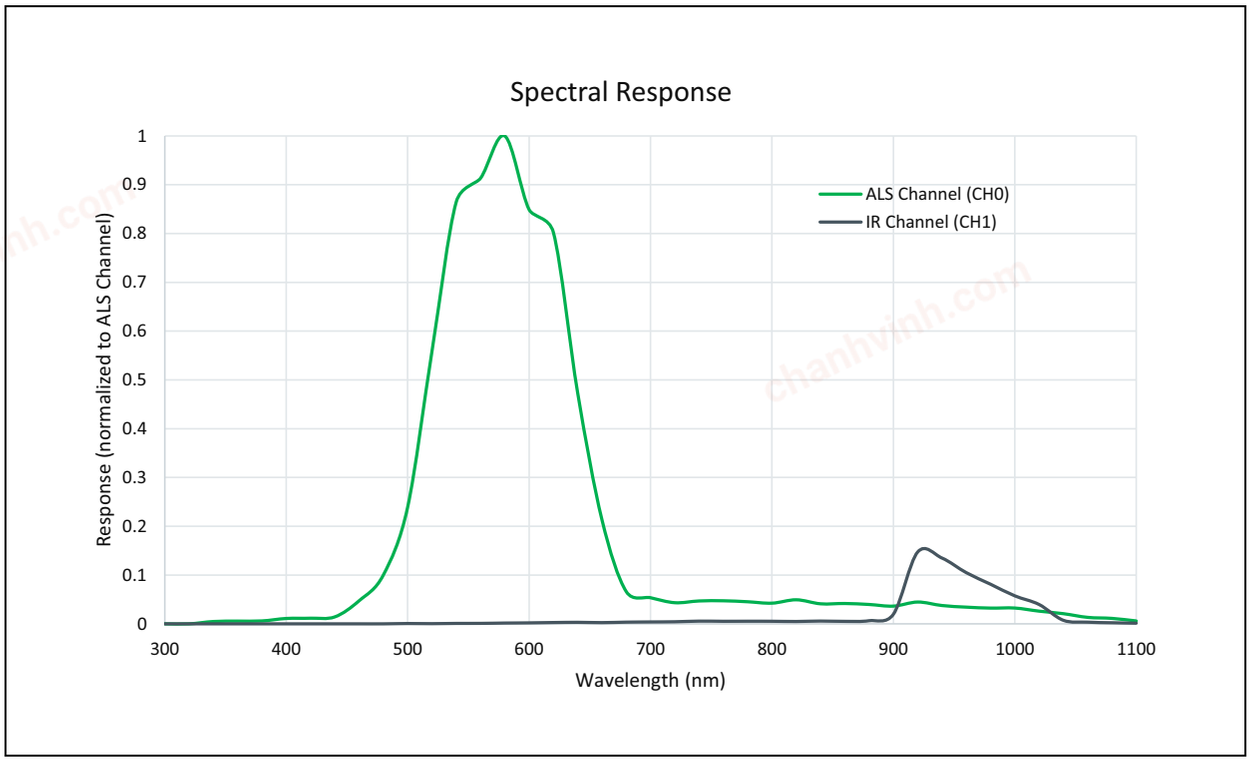
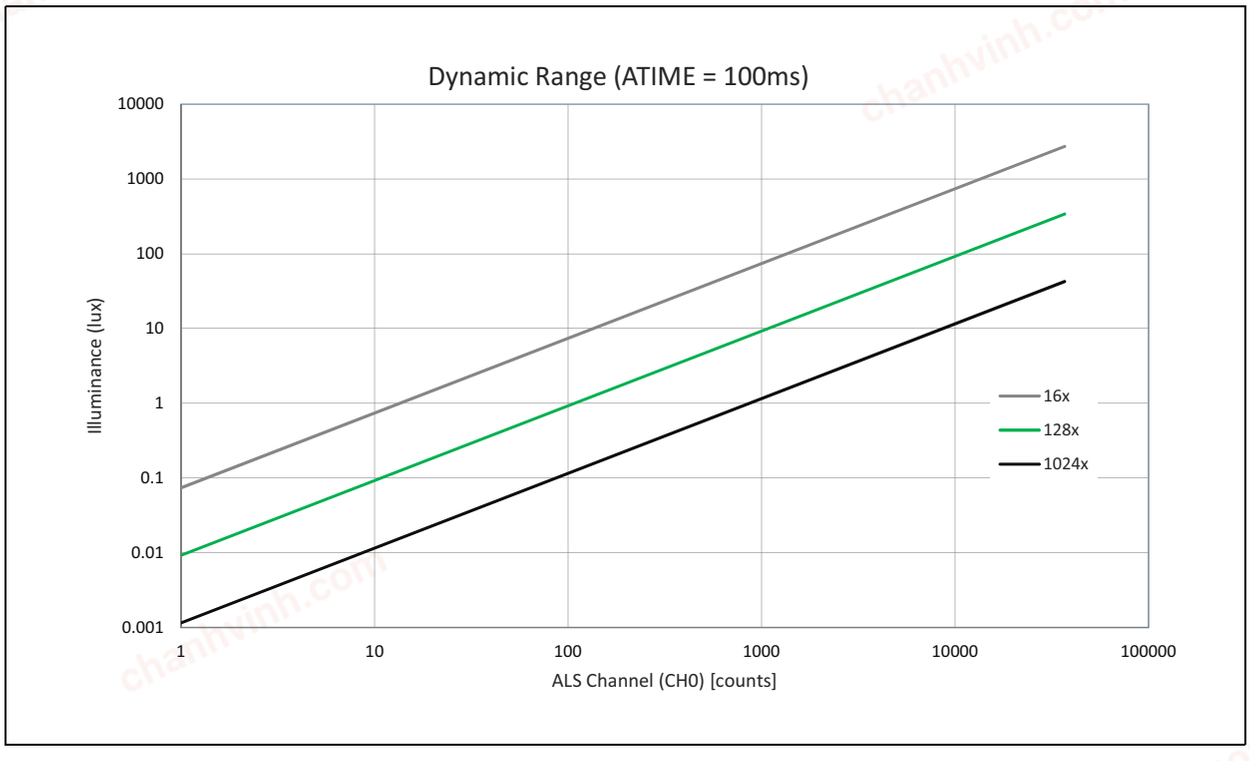



**Figure 13:**
**Illuminance (Lux) vs Counts (ALS Channel (CH0))**



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# Detailed Description

## Proximity

Proximity results are affected by three fundamental factors: the integrated IR VCSEL emission, IR reception, and environmental factors, including target distance and surface reflectivity. The IR reception signal path begins with IR detection from a photodiode and ends with the 14-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register. The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

## Ambient Light Sensing, ALS

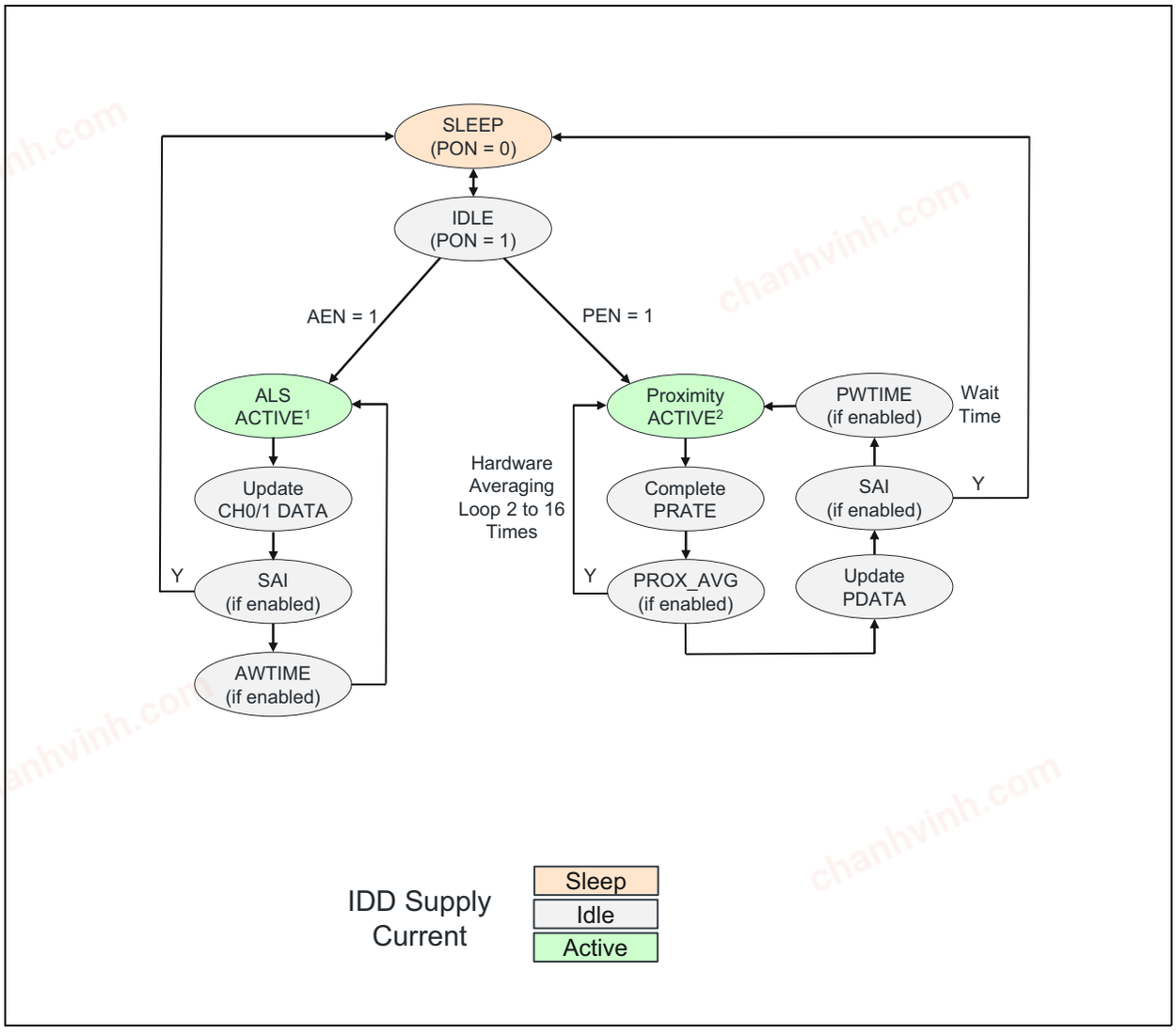
The ALS reception signal path begins as photodiodes receive filtered light and ends with 16-bit results. Channel 0 contains a photopic filter and channel 1 contains an infrared (IR) filter which is used both for the proximity function and also to accurately measure ambient light levels. Signals from both photodiodes are simultaneously accumulated for a period of time set by the value in ATIME before the results are available. Gain is adjustable by either 128x or 1024x to facilitate operation over a wide range of lighting conditions under dark glass with low transmissivity. Based on the optical glass used on top of the device, custom equations are empirically derived to calculate the amount of ambient light using the ALS results.

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## Operational State Diagram

**Figure 14:**
**Operational State Diagram**




**Note(s):**

1. ALS active time = ALS integration time (ATIME)
2. Proximity active time = (7 x (PULSE_LEN + 42.15µs)) + PPULSE x (2 x PULSE_LEN + 84.3µs) + 78.75µs.

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## I²C Characteristics

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

### *I²C Write Transaction*

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9$^{th}$ clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

### *I²C Read Transaction*

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9$^{TH}$ clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without “re”-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9$^{th}$ clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

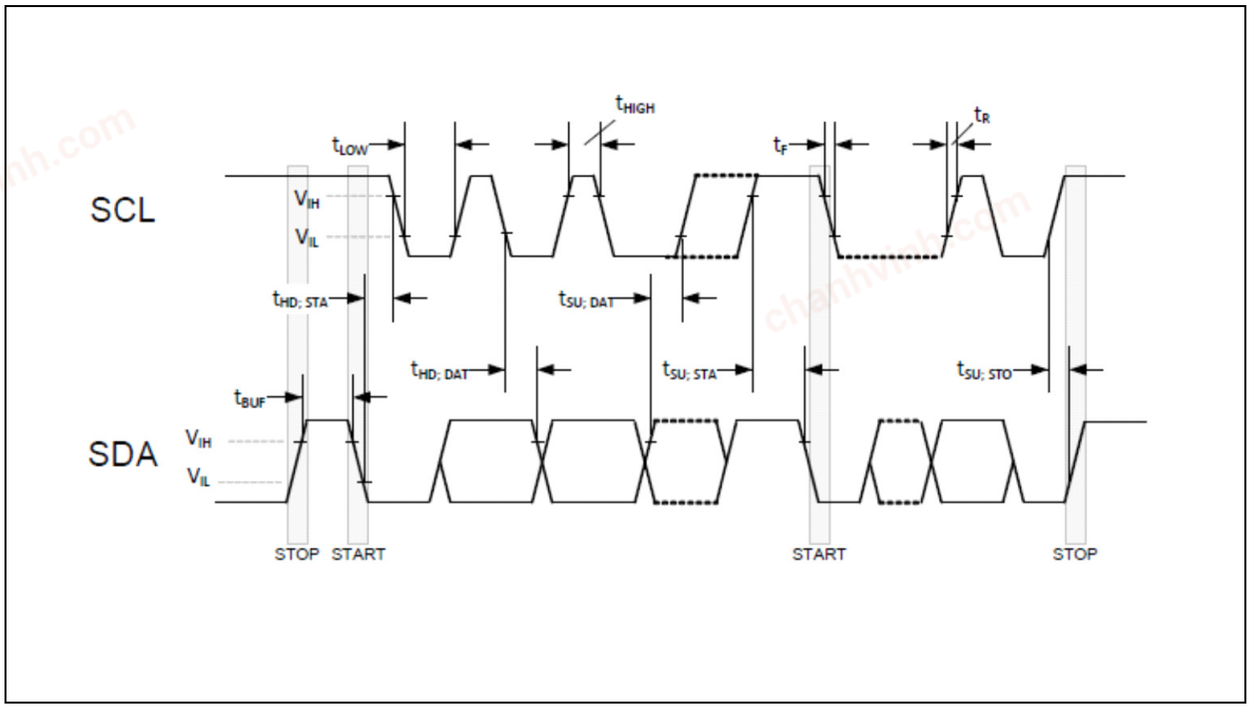
http://www.i2c-bus.org/references/

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## Timing Diagrams

**Figure 15:**
**I²C Timing Diagrams**



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## Register Description

Figure 16:
Register Overview

| Address | Register Name | R/W | Register Function | Reset Value |
|---|---|---|---|---|
| 0x80 | ENABLE | R/W | Enables states and interrupts | 0x00 |
| 0x81 | ATIME | R/W | ADC integration time | 0x00 |
| 0x82 | PRATE | R/W | Proximity time | 0x1F |
| 0x83 | AWTIME | R/W | ALS wait time | 0x00 |
| 0x84 | AILTL | R/W | ALS interrupt low threshold low byte | 0x00 |
| 0x85 | AILTH | R/W | ALS interrupt low threshold high byte | 0x00 |
| 0x86 | AIHTL | R/W | ALS interrupt high threshold low byte | 0x00 |
| 0x87 | AIHTH | R/W | ALS interrupt high threshold high byte | 0x00 |
| 0x88 | PILTL | R/W | Proximity interrupt low threshold low byte | 0x00 |
| 0x89 | PILTH | R/W | Proximity interrupt low threshold high byte | 0x00 |
| 0x8A | PIHTL | R/W | Proximity interrupt high threshold low byte | 0x00 |
| 0x8B | PIHTH | R/W | Proximity interrupt high threshold high byte | 0x00 |
| 0x8C | PERS | R/W | ALS and proximity interrupt persistence filters | 0x00 |
| 0x8D | CFG0 | R/W | Configuration zero | 0x50 |
| 0x8E | PCFG0 | R/W | Proximity configuration zero | 0x8F |
| 0x8F | PCFG1 | R/W | Proximity configuration one | 0x32 |
| 0x90 | PCFG2 | R/W | Proximity configuration two | 0x20 |
| 0x91 | CFG1 | R/W | Configuration one | 0x68 |
| 0x92 | REVID | R | Revision ID | 0x00 |
| 0x93 | ID | R | Device ID | 0x50 |
| 0x94 | STATUS | R, SC | Device status | 0x00 |
| 0x95 | ALSL | R | ALS (CH0) low data | 0x00 |
| 0x96 | ALSH | R | ALS (CH0) high data | 0x00 |
| 0x97 | IRL | R | IR (CH1) low data | 0x00 |
| 0x98 | IRH | R | IR (CH1) high data | 0x00 |
| 0x99 | PDATAL | R | Proximity ADC low data | 0x00 |
| 0x9A | PDATAH | R | Proximity ADC high data | 0x00 |

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| Address | Register Name | R/W | Register Function | Reset Value |
|---|---|---|---|---|
| 0xA6 | REVID2 | R | Revision ID two | 0x00 or 0x0C |
| 0xA8 | SOFTRST | R/W | Soft reset | 0x00 |
| 0xA9 | PWTIME | R/W | Proximity wait time | 0x00 |
| 0xAA | CFG8 | R/W | Configuration eight (must be set to 0x29) | 0x2A |
| 0xAB | CFG3 | R/W | Configuration three | 0x01 |
| 0xAE | CFG6 | R/W | Configuration six | 0x3F |
| 0xC0 | POFFSETL | R/W | Proximity offset low data | 0x00 |
| 0xC1 | POFFSETH | R/W | Proximity offset high data | 0x00 |
| 0xD7 | CALIB | R/W | Proximity offset calibration | 0x00 |
| 0xD8 | CALIB_OFFSET | R/W | Proximity offset extension | 0x00 |
| 0xD9 | CALIBCFG | R/W | Proximity offset calibration control | 0x50 |
| 0xDC | CALIBSTAT | R | Proximity offset calibration status | 0x00 |
| 0xDD | INTENAB | R/W | Interrupt enables | 0x00 |
| 0xE6 | FAC_L | R | Factory data low | 0x00 to 0xFF |
| 0xE7 | FAC_H | R | Factory data high | 0x00 to 0xFF |
| 0xF9 | TEST9 | R/W | Test nine (must be set to 0x02) | 0x0C |

**Note(s):**

1. R = Read Only / W = Write Only / R/W = Read or Write / SC = Self Clearing after access.

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## Detailed Register Description

### *Enable Register (Address 0x80)*

**Figure 17:**
**Enable Register**

| Addr: 0x80 | | Enable | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:5 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 4 | PWEN | 0 | RW | This bit activates the proximity wait feature which is set by the PWTIME register. Active high. (1) |
| 3 | AWEN | 0 | RW | This bit activates the ALS wait feature which is set by the AWTIME register. Active high. |
| 2 | PEN | 0 | RW | This bit activates the proximity detection. Active high. |
| 1 | AEN | 0 | RW | This bit actives the ALS function. Active high. |
| 0 | PON | 0 | RW | This field activates the internal oscillator and ADC channels. Active high. |

**Note(s):**

1. When the ALS function is enabled (AEN = 1), this bit must be set to a one (PWEN = 1).

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

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### *ATIME Register (Address 0x81)*

**Figure 18:**
**ATIME Register**

| Addr: 0x81 | | ATIME | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | | | |
| 7:0 | ATIME | 0x00 | RW | The ATIME value specifies the ALS integration time in 2.78ms intervals. 0x00 indicates 2.78ms. The maximum ALS count value depends on the integration time. For every 2.78ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.78ms. | | | |
| | | | | **Value** | **Integration Cycles** | **Integration Time** | **Maximum ALS Value** |
| | | | | 0x00 | 1 | 2.78ms | 1023 |
| | | | | 0x01 | 2 | 5.56ms | 2047 |
| | | | | 0x11 | 18 | 50.0ms | 18431 |
| | | | | 0x23 | 36 | 100ms | 36863 |
| | | | | 0x3F | 64 | 178ms | 65535 |
| | | | | 0xFF | 256 | 712ms | 65535 |

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.78ms nominal rate. Loading 0x00 will generate a 2.78ms integration time, loading 0x01 will generate a 5.56ms integration time, and so forth.

### *PRATE Register (Address 0x82)*

**Figure 19:**
**PRATE Register**

| Addr: 0x82 | | PRATE | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | PRATE | 0x1F | RW | This register defines the duration of 1 Prox Sample, which is (PRATE + 1)*88µs. |

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### AWTIME Register (Address 0x83)

Figure 20:
AWTIME Register

| Addr: 0x83 | | AWTIME | | | | |
|---|---|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description | | |
| 7:0 | AWTIME | 0x00 | RW | Value that specifies the wait time in 2.78ms increments. | | |
| | | | | Value | Increments | Wait Time |
| | | | | 0x00 | 1 | 2.78ms (33.4ms) |
| | | | | 0x01 | 2 | 5.56ms (66.7ms) |
| | | | | 0x11 | 18 | 50.0ms (600ms) |
| | | | | 0x23 | 36 | 100ms (1.20s) |
| | | | | 0x3F | 64 | 178ms (2.14s) |
| | | | | 0xFF | 256 | 712ms (8.54s) |

The wait timer is implemented using a down counter. Wait time = Increment x 2.78ms. If AWLONG is enabled then Wait time = Increment x 2.78ms x 12.

### AILTL Register (Address 0x84)

Figure 21:
AILTL Register

| Addr: 0x84 | | AILTL | | |
|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | AILTL | 0x00 | RW | This register sets the low byte of the LOW ALS threshold. |

### AILTH Register (Address 0x85)

Figure 22:
AILTH Register

| Addr: 0x85 | | AILTH | | |
|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | AILTH | 0x00 | RW | This register sets the high byte of the LOW ALS threshold. |

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The ALS (CH0) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the ALS channel (CH0) is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

### *AIHTL Register (Address 0x86)*

**Figure 23:**
**AIHTL Register**

| Addr: 0x86 | | AIHTL | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | AIHTL | 0x00 | RW | This register sets the low byte of the HIGH ALS threshold. |

### *AIHTH Register (Address 0x87)*

**Figure 24:**
**AIHTH Register**

| Addr: 0x87 | | AIHTH | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | AIHTH | 0x00 | RW | This register sets the high byte of the HIGH ALS threshold. |

The ALS (CH0) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the ALS channel (CH0) is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

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### PILTL Register (Address 0x88)

Figure 25:
PILTL Register

| Addr: 0x88 | | PILTL | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | PILTL | 0x00 | RW | This register contains the low byte of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register contains the LOW threshold which is an 8-bit value which is compared against the upper 8-bits of the 10-bit proximity value. |

### PILTH Register (Address 0x89)

Figure 26:
PILTH Register

| Addr: 0x89 | | PILTH | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:6 | Reserved | 00 | RW | Reserved. Must be set to default value. |
| 5:0 | PILTH | 0x00 | RW | This register contains the upper 6 bits of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register is ignored. |

The contents of the PILTH and PILTL registers are combined and treated as a fourteen (14) bit threshold low value. If the value generated by the proximity ADC (PDATA) is below the PILTL/H threshold and the PPERS value is reached, then the low proximity threshold is breached. When setting the 14-bit proximity threshold, PILTL must be written first, immediately follow by PILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PILTL contains an 8-bit threshold which is compared against the upper 8-bits of the 10-bit value. PILTH is ignored.

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### PIHTL Register (Address 0x8A)

Figure 27:
PIHTL Register

| Addr: 0x8A | | PIHTL | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | PIHTL | 0x00 | RW | This register contains the low byte of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register contains the HIGH threshold which is an 8-bit value which is compared against the upper 8-bits of the 10-bit proximity value. |

### PIHTH Register (Address 0x8B)

Figure 28:
PIHTH Register

| Addr: 0x8B | | PIHTH | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:6 | Reserved | 00 | RW | Reserved. Must be set to default value. |
| 5:0 | PIHTH | 0x00 | RW | This register contains the upper 6 bits of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register is ignored. |

The contents of the PIHTH and PIHTL registers are combined and treated as a fourteen (14) bit threshold high value. If the value generated by the proximity ADC (PDATA) is above the PIHTL/H threshold and the PPERS value is reached, then the high proximity threshold is breached. When setting the 14-bit proximity threshold, PIHTL must be written first, immediately follow by PIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PIHTL contains an 8-bit threshold which is compared against the upper 8-bits of the 10-bit value. PIHTH is ignored.

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### *PERS Register (Address 0x8C)*

**Figure 29:**
**PERS Register**

| Addr: 0x8C | | PERS | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | |
| 7:4 | PPERS | 0 (0000) | RW | This register sets the proximity persistence filter. | |
| | | | | Value | Interrupt |
| | | | | 0 (0000) | Every proximity cycle |
| | | | | 1 (0001) | Any value outside proximity thresholds |
| | | | | 2 (0010) | 2 consecutive proximity values out of range |
| | | | | 3 (0011) | 3 consecutive proximity values out of range |
| | | | | … | …. |
| | | | | 15 (1111) | 15 consecutive proximity values out of range |
| 3:0 | APERS | 0 (0000) | RW | This register sets the ALS persistence filter. | |
| | | | | 0 (0000) | Every ALS cycle |
| | | | | 1 (0001) | Any value outside ALS thresholds |
| | | | | 2 (0010) | 2 consecutive ALS values out of range |
| | | | | 3 (0011) | 3 consecutive ALS values out of range |
| | | | | 4 (0100) | 5 consecutive ALS values out of range |
| | | | | 5 (0101) | 10 consecutive ALS values out of range |
| | | | | 6 (0110) | 15 consecutive ALS values out of range |
| | | | | 7 (0111) | 20 consecutive ALS values out of range |
| | | | | … | … |
| | | | | 13 (1101) | 50 consecutive ALS values out of range |
| | | | | 14 (1110) | 55 consecutive ALS values out of range |
| | | | | 15 (1111) | 60 consecutive ALS values out of range |

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.

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The frequency of consecutive ALS (CH0) channel results outside of threshold limits are counted; this count value is compared against the APERS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time an ALS (CH0) channel result is inside the threshold values the counter is cleared.

### *CFG0 Register (Address 0x8D)*

**Figure 30:**
**CFG0 Register**

| Addr: 0x8D | | CFG0 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:4 | Reserved | 0101 | RW | Reserved. Must be set to default value. |
| 3 | PWLONG | 0 | RW | When PWLONG (PROX Wait Long) is asserted the wait period as set by PWTIME is increased by a factor of 12. |
| 2 | AWLONG | 0 | RW | When AWLONG (ALS Wait Long) is asserted the wait period as set by AWTIME is increased by a factor of 12. |
| 1:0 | Reserved | 00 | RW | Reserved. Must be set to default value. |

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### *PCFG0 Register (Address 0x8E)*

**Figure 31:**
**PCFG0 Register**

| Addr: 0x8E | | PCFG0 | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | |
| 7:6 | PGAIN1 | 2 (10) | RW | This field along with the PGAIN2 bits in the CFG1 register, sets the gain of the proximity IR sensor. | |
| | | | | **Value** | **Stage 1 Gain** |
| | | | | 0 (00) | 1x |
| | | | | 1 (01) | 2x |
| | | | | 2 (10) | 4x |
| | | | | 3 (11) | 8x |
| 5:0 | PPULSE | 15 (001111) | RW | Maximum number of pulses in a single proximity cycle. | |
| | | | | **Value** | **Maximum Number of Pulses** |
| | | | | 0 (000000) | 1 |
| | | | | 1 (000001) | 2 |
| | | | | 2 (000010) | 3 |
| | | | | … | … |
| | | | | 63 (111111) | 64 |

The PPULSE field sets the maximum number of IR VCSEL pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR VCSEL pulses, up to the value set in PPULSE or if a near-saturation condition occurs if Automatic Pulse Control (APC) is enabled. The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets. This operation also reduces power consumption because proximity integration period is automatically shortened when a target is close to the sensor.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then PPULSE always determines the number of proximity pulses to be transmitted.

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### PCFG1 Register (Address 0x8F)

Figure 32:
PCFG1 Register

| Addr: 0x8F | | PCFG1 | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | |
| 7:6 | PPULSE_LENH | 00 | RW | These bits are the 2 most significant bits of the 10-bit Pulse Length control setting. The lower 8 bits are in the PCFG2 register. See the PCFG2 register for details. | |
| 5:4 | Reserved | 11 | RW | Reserved. Must be set to default value. | |
| 3:0 | PLDRIVE | 2 (0010) | RW | This field sets the drive strength of the IR VCSEL current. Values are approximate; actual current through the VCSEL is factory trimmed to normalize IR intensity. | |
| | | | | **Value** | **VCSEL Current** |
| | | | | 5 (0101) | 7mA |
| | | | | 6 (0110) | 8mA |
| | | | | 7 (0111) | 9mA |
| | | | | 8 (1000) | 10mA |
| | | | | All other values | Reserved |

### PCFG2 Register (Address 0x90)

Figure 33:
PCFG2 Register

| Addr: 0x90 | | PCFG2 | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | |
| 7:0 | PPULSE_LENL | 0x20 | RW | These bits are the 8 least significant bits of the 10-bit Pulse Length control setting. The upper 2 bits are in the PCFG1 register. The minimum pulse length is 32µs. | |
| | | | | **Value** | **Pulse Length** |
| | | | | 30 (0000011110) | 32µs |
| | | | | 31 (0000011111) | 33µs |
| | | | | Pulse Length = (PULSE_LEN + 2) µs | |
| | | | | 1023 (1111111111) | 1025µs |

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### *CFG1 Register (Address 0x91)*

**Figure 34:**
**CFG1 Register**

| Addr: 0x91 | | CFG1 | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | |
| 7 | Reserved | 0 | RW | Reserved. Must be set to default value. | |
| 6:5 | PGAIN2 | 3 (11) | RW | This field along with the PGAIN1 bits in the PCFG0 register, sets the gain of the proximity IR sensor. | |
| | | | | **Value** | **Stage 2 Gain** |
| | | | | 0 (00) | 2.5x |
| | | | | 1 (01) | 5x |
| | | | | 2 (10) | Reserved |
| | | | | 3 (11) | 10x |
| 4:0 | AGAIN | 8 (01000) | RW | This field sets the gain of the ALS sensor. | |
| | | | | **Value** | **ALS Gain** |
| | | | | 5 (00101) | 16x |
| | | | | 8 (01000) | 128x |
| | | | | 11 (01011) | 1024x |
| | | | | All other values | Reserved |

### *REVID Register (Address 0x92)*

**Figure 35:**
**REVID Register**

| Addr: 0x92 | | REVID | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:3 | Reserved | 00000 | R | Reserved. |
| 2:0 | REV_ID | 000 | R | Device revision number. |

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### ID Register (Address 0x93)

Figure 36:
ID Register

| Addr: 0x93 | | ID | | |
|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:2 | ID | 010100 | R | Device type identification. |
| 1:0 | Reserved | 00 | R | Reserved |

### STATUS Register (Address 0x94)

Figure 37:
STATUS Register

| Addr: 0x94 | | STATUS Register | | |
|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | ASAT | 0 | R, SC | Analog saturation flag signals that the ALS results may be unreliable due to saturation of the AFE. |
| 6 | PSAT | 0 | R, SC | Proximity saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. |
| 5 | PINT | 0 | R, SC | Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings. |
| 4 | AINT | 0 | R, SC | ALS interrupt flag indicates that ALS results (CH0) have exceeded thresholds and persistence settings. |
| 3 | CINT | 0 | R, SC | Calibration interrupt flag indicates that calibration has completed. |
| 2 | ZINT | 0 | R, SC | Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1). |
| 1 | PSAT_REFLECTIVE | 0 | R, SC | The Reflective Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL active portion of proximity integration. |
| 0 | PSAT_AMBIENT | 0 | R, SC | The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL inactive portion of proximity integration. |

All flags in this register can be cleared by setting the bit high. Alternatively, if the INT_READ_CLEAR in the CFG3 register bit is set, then simply reading this register automatically clears all eight flags.

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### *ALSL Register (Address 0x95)*

**Figure 38:**
**ALSL Register**

| Addr: 0x95 | | ALSL | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | ALSL | 0x00 | R | This register contains the low byte of the 16-bit ALS channel (CH0) data. |

### *ALSH Register (Address 0x96)*

**Figure 39:**
**ALSH Register**

| Addr: 0x96 | | ALSH | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | ALSH | 0x00 | R | This register contains the high byte of the 16-bit ALS channel (CH0) data. |

### *IRL Register (Address 0x97)*

**Figure 40:**
**IRL Register**

| Addr: 0x97 | | IRL | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | IRL | 0x00 | R | This register contains the low byte of the 16-bit IR channel (CH1) data. |

### *IRH Register (Address 0x98)*

**Figure 41:**
**IRH Register**

| Addr: 0x98 | | IRH | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | IRH | 0x00 | R | This register contains the high byte of the 16-bit IR channel (CH1) data. |

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### PDATAL Register (Address 0x99)

Figure 42:
PDATAL Register

| Addr: 0x99 | | PDATAL | | |
|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | PDATAL | 0x00 | R | This register contains the low byte of the 14-bit proximity ADC data when APC is enabled. If APC is disabled, this register contains the upper 8 most significant bits of the 10-bit proximity value. |

### PDATAH Register (Address 0x9A)

Figure 43:
PDATAH Register

| Addr: 0x9A | | PDATAH | | |
|---|---|---|---|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | PDATAH | 0x00 | R | This register contains the high byte of the 14-bit proximity ADC data when APC is enabled. If APC is disabled, bits 1:0 contain the lower 2 bits of the 10-bit proximity value. |

Proximity data is stored as a 14-bit value (two bytes). Reading the low byte first latches the high byte. Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases. Proximity detection uses a 10-bit ADC that is extended to a 14-bit dynamic range for PDATA using the following formula:

$PDATA = ADC_{value} \times (16 / \text{actual number of pulses transmitted})$

PDATA is therefore proportional to the reflected energy independent of the number of pulses transmitted.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PDATAL contains the 8 most significant bits of the 10-bit value and PDATAH bit locations 1:0 contain the lower 2-bits. When APC is disabled, only the upper 8-bits are compared against the threshold values contained in PILTL and PIHTL.

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### *REVID2 Register (Address 0xA6)*

**Figure 44:**
**REVID2 Register**

| Addr: 0xA6 | | REVID2 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:4 | Reserved | 0000 | R | Reserved. |
| 3:0 | VER_ID | 0000 or 1100 | R | Device version number. |

### *SOFTRST Register (Address 0xA8)*

**Figure 45:**
**SOFTRST Register**

| Addr: 0xA8 | | SOFTRST | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:2 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 1 | POR | 0 | RW | Writing a 1 to this bit will cause a power on reset. This will immediately terminate all device operation and put the device into the sleep state. |
| 0 | SOFTRST | 0 | RW | Writing a 1 to this bit will cause all registers to be reset to their default state. This will immediately terminate all device operation and put the device into the sleep state. |

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### *PWTIME Register (Address 0xA9)*

**Figure 46:**
**PWTIME Register**

| Addr: 0xA9 | | PWTIME | | | | |
|---|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | | |
| 7:0 | PWTIME | 0x00 | RW | Value that specifies the wait time in 2.78ms increments. | | |
| | | | | **Value** | **Increments** | **Wait Time** |
| | | | | 0x00 | 1 | 2.78ms (33.4ms) |
| | | | | 0x01 | 2 | 5.56ms (66.7ms) |
| | | | | 0x11 | 18 | 50.0ms (600ms) |
| | | | | 0x23 | 36 | 100ms (1.20s) |
| | | | | 0x3F | 64 | 178ms (2.14s) |
| | | | | 0xFF | 256 | 712ms (8.54s) |

The wait timer is implemented using a down counter. Wait time = Increment x 2.78ms. If PWLONG is enabled then Wait time = Increment x 2.78ms x 12.

### *CFG8 Register (Address 0xAA)*

**Figure 47:**
**CFG8 Register**

| Addr: 0xAA | | CFG8 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | Reserved | 0x2A | RW | Reserved. Must be set to 0x29. |

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### CFG3 Register (Address 0xAB)

Figure 48:
CFG3 Register

| Addr: 0xAB | | CFG3 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7 | INT_READ_CLEAR | 0 | RW | If set, then flag bits in the STATUS register will be reset whenever the STATUS register is read over $I^2C$. |
| 6:5 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 4 | SAI | 0 | RW | The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion. |

| PON | SAI | INT | Oscillator |
|---|---|---|---|
| 0 | X | X | OFF |
| 1 | 0 | X | ON |
| 1 | 1 | 1 | ON |
| 1 | 1 | 0 | OFF |

| | | | | |
|---|---|---|---|---|
| 3:0 | Reserved | 0001 | RW | Reserved. Must be set to default value. |

The SAI bit sets the device operational mode following the completion of an ALS or proximity cycle. If AINT and AIEN are both set or if PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

### CFG6 Register (Address 0xAE)

Figure 49:
CFG6 Register

| Addr: 0xAE | | CFG6 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 6 | APC_ DISABLE | 0 | RW | Proximity automatic pulse control (APC) disable.<br>0 = APC enable<br>1 = APC disable |
| 5:0 | Reserved | 111111 | RW | Reserved. Must be set to default value. |

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### *POFFSETL Register (Address 0xC0)*

**Figure 50:**
**POFFSETL Register**

| Addr: 0xC0 | | POFFSETL | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | POFFSETL | 0x00 | RW | This register contains the magnitude portion of proximity offset adjust value. |

### *POFFSETH Register (Address 0xC1)*

**Figure 51:**
**POFFSETH Register**

| Addr: 0xC1 | | POFFSETH | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:1 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 0 | POFFSETH | 0 | RW | This register contains the sign portion of proximity offset adjust value. |

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 255 is possible.

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### CALIB Register (Address 0xD7)

Figure 52:
CALIB Register

| Addr: 0xD7 | | CALIB | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7 | CALAVG | 0 | RW | Enables proximity hardware averaging as selected with PROX_AVG during calibration.<br>0 = No hardware averaging<br>1 = Hardware averaging enabled |
| 6 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 5 | ELECTRICAL_ CALIBRATION | 0 | RW | Selects proximity calibration type.<br>0 = Electrical and optical crosstalk.<br>1 = Electrical crosstalk only. |
| 4 | CALPRATE | 0 | RW | Enables PRATE during calibration. Useful when averaging is enabled.<br>0 = PRATE ignored<br>1 = PRATE applied between averaging samples |
| 3:1 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 0 | START_OFFSET_CAL | 0 | RW | Set to 1 to start a calibration sequence. |

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a portion of the VCSEL IR which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and also influences the proximity result. The calibration routine adjusts the value in POFFSETL/H until the proximity result is as close to the binary search target as possible. Optical and electrical calibration function identically, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.
An electrical calibration can be initiated anytime by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CAL bits. To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_ OFFSET_CALIB. The CINT flag will assert after calibration has finished. Upon completion proximity offset registers are automatically loaded with calibration result.

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### CALIB_OFFSET Register (Address 0xD8)

Figure 53:
CALIB_OFFSET Register

| Addr: 0xD8 | | CALIB_OFFSET | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:6 | Reserved | 0 | RW | Reserved. Must be set to default value. |
| 5 | EN_RANGE_ EXTENSION | 0 | RW | Setting this bit to a 1 enables the proximity offset range extension functionality. See the OFFSET_ RANGE_EXTENSION bits. If this bit is set to 0, the offset range extension is disabled. |
| 4:0 | OFFSET_ RANGE_ EXTENSION | 0 (00000) | RW | Offset range extension selection. |

| Value | Selection |
|---|---|
| 0 (00000) | Nominal |
| 1 (00001) | Nominal + 1 Step |
| 2 (00010) | Nominal + 2 Steps |
| 3 (00011) | Nominal + 3 Steps |
| Nominal + (Value) Steps | |
| 31 (11111) | Nominal + 31 Steps |

For applications with high optical proximity crosstalk (the emitted IR optical signal appears at the IR sensor), the offset range can be extended in discrete steps. To determine the best range extension step for the application, a proximity calibration cycle is initiated and the resulting proximity offset is captured in the POFFSETL/H registers.

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### CALIBCFG Register (Address 0xD9)

Figure 54:
CALIBCFG Register

| Addr: 0xD9 | | CALIBCFG | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** | |
| 7:5 | BINSRCH_ TARGET | 2 (010) | RW | Proximity offset calibration result target. | |
| | | | | **Value** | **PDATA Target** |
| | | | | 0 (000) | 3 |
| | | | | 1 (001) | 7 |
| | | | | 2 (010) | 15 |
| | | | | 3 (011) | 31 |
| | | | | 4 (100) | 63 |
| | | | | 5 (101) | 127 |
| | | | | 6 (110) | 255 |
| | | | | 7 (111) | 511 |
| 4 | Reserved | 1 | RW | Reserved. Must be set to default value. | |
| 3 | AUTO_OFFSET_ ADJ | 0 | RW | If set, this bit causes the value in POFFSETL register to be decremented if PDATA ever becomes zero. | |
| 2:0 | PROX_AVG | 0 (000) | RW | PROX_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle. | |
| | | | | **Value** | **Sample Size** |
| | | | | 0 (000) | Disable |
| | | | | 1 (001) | 2 |
| | | | | 2 (010) | 4 |
| | | | | 3 (011) | 8 |
| | | | | 4 (100) | 16 |
| | | | | All other values | Reserved |

The binary search target field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target, and BINSEARCH_TARGET setting of 2 causes the PDATA value to be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

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The PROX_AVG field sets the number of ADC samples that are averaged. Each ADC sample causes the programmed number of proximity pulses to be transmitted. Once all samples have been completed and the average is calculated, the proximity state machine will then pass this value directly to PDATA.

### *CALIBSTAT Register (Address 0xDC)*

**Figure 55:**
**CALIBSTAT Register**

| Addr: 0xDC | | CALIBSTAT | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:3 | Reserved | 0 | R | Reserved. Must be set to default value. |
| 2 | OFFSET_ ADJUSTED | 0 | R | Bit is set when the proximity offset has been automatically decremented if AUTO_OFFSET_ ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting AUTO_ OFFSET_ADJ to 0. |
| 1 | Reserved | 0 | R | Reserved. Must be set to default value. |
| 0 | CALIB_FINISHED | 0 | R | This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared. |

### *INTENAB Register (Address 0xDD)*

**Figure 56:**
**INTENAB Register**

| Addr: 0xDD | | INTENAB | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7 | ASIEN | 0 | RW | ALS Saturation Interrupt Enable |
| 6 | PSIEN | 0 | RW | Proximity Saturation Interrupt Enable |
| 5 | PIEN | 0 | RW | Proximity Interrupt Enable |
| 4 | AIEN | 0 | RW | ALS Interrupt Enable |
| 3 | CIEN | 0 | RW | Calibration Interrupt Enable |
| 2 | ZIEN | 0 | RW | Zero Detect Interrupt Enable |
| 1:0 | Reserved | 0 | RW | Reserved. Must be set to default value. |

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### *FAC_L Register (Address 0xE6)*

**Figure 57:**
**FAC_L Register**

| Addr: 0xE6 | | FAC_L | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | Reserved | 0x00 – 0xFF | R | Reserved for factory use. |

### *FAC_H Register (Address 0xE7)*

**Figure 58:**
**FAC_H Register**

| Addr: 0xE7 | | FAC_H | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | Reserved | 0x00 – 0xFF | R | Reserved for factory use. |

### *TEST9 Register (Address 0xF9)*

**Figure 59:**
**TEST9 Register**

| Addr: 0xF9 | | TEST9 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 7:0 | Reserved | 0x0C | R/W | Reserved. Must be set to 0x02. |

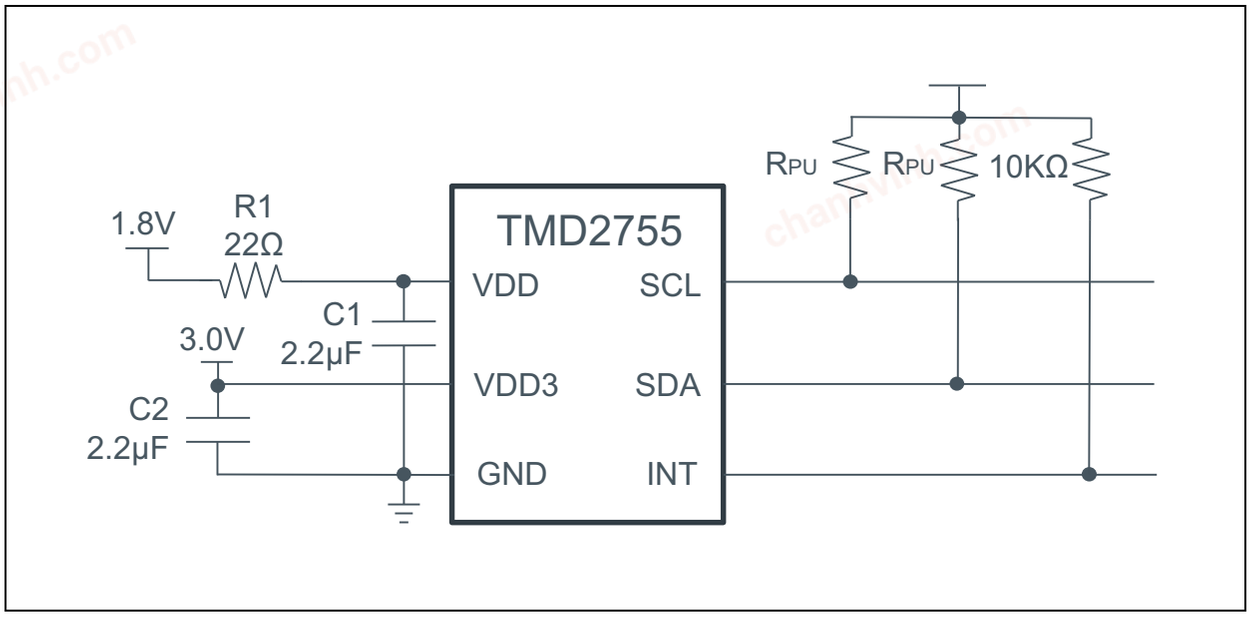
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# Application Information

## Schematic

**Figure 60:**
**Typical Applications Circuit**




**Note(s):**

1. Place the 2.2µF VDD (C1) and 2.2µF VDD3 (C2) capacitors within 5mm of the module.
2. The value of the $I^2C$ pull up resistors ($R_{PU}$) should be based on the 1.8V bus voltage, system bus speed and trace capacitance.
3. C1 and C2 are critical components to protect the device during high voltage ESD strikes.
4. In systems subjected to high voltage ESD strikes, it is recommended to connect VDD to a host GPIO pin to allow the device to be independently power cycled.

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## Recommended Circuit Layout

**Figure 61:**
**With INT Pin Operational**




**Note(s):**

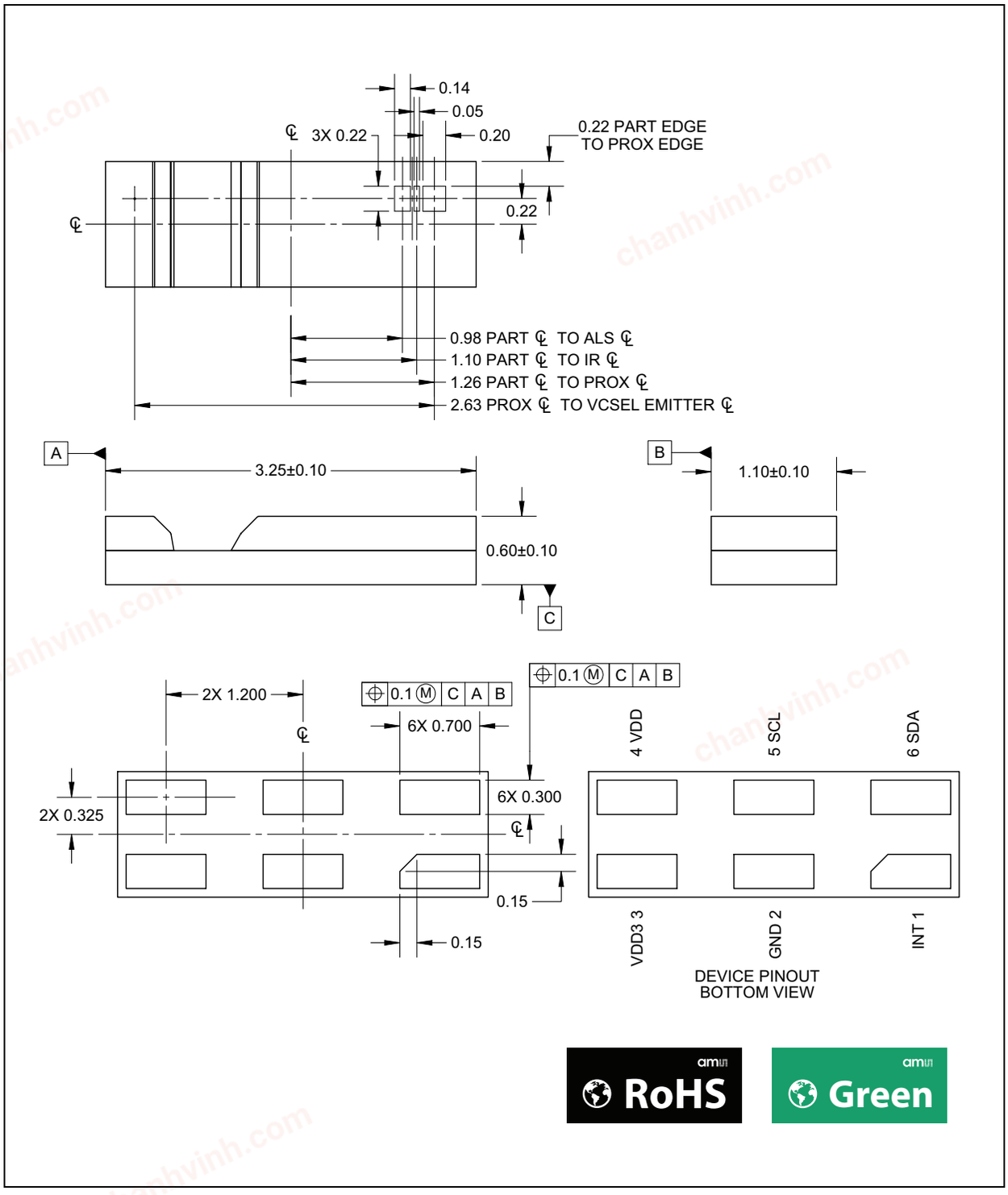
1. The dominant factor governing device performance is the component placement, not necessarily component value. The placement of the decoupling capacitor, C1, is the most critical. Place the component on the same side of PCB as device as shown in the figure above. Make connection as close as possible to minimize series inductance and resistance. This is critical.

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# Package Drawings & Markings

**Figure 62:**
**Package Drawings**




**Note(s):**

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. Contact finish is Au.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

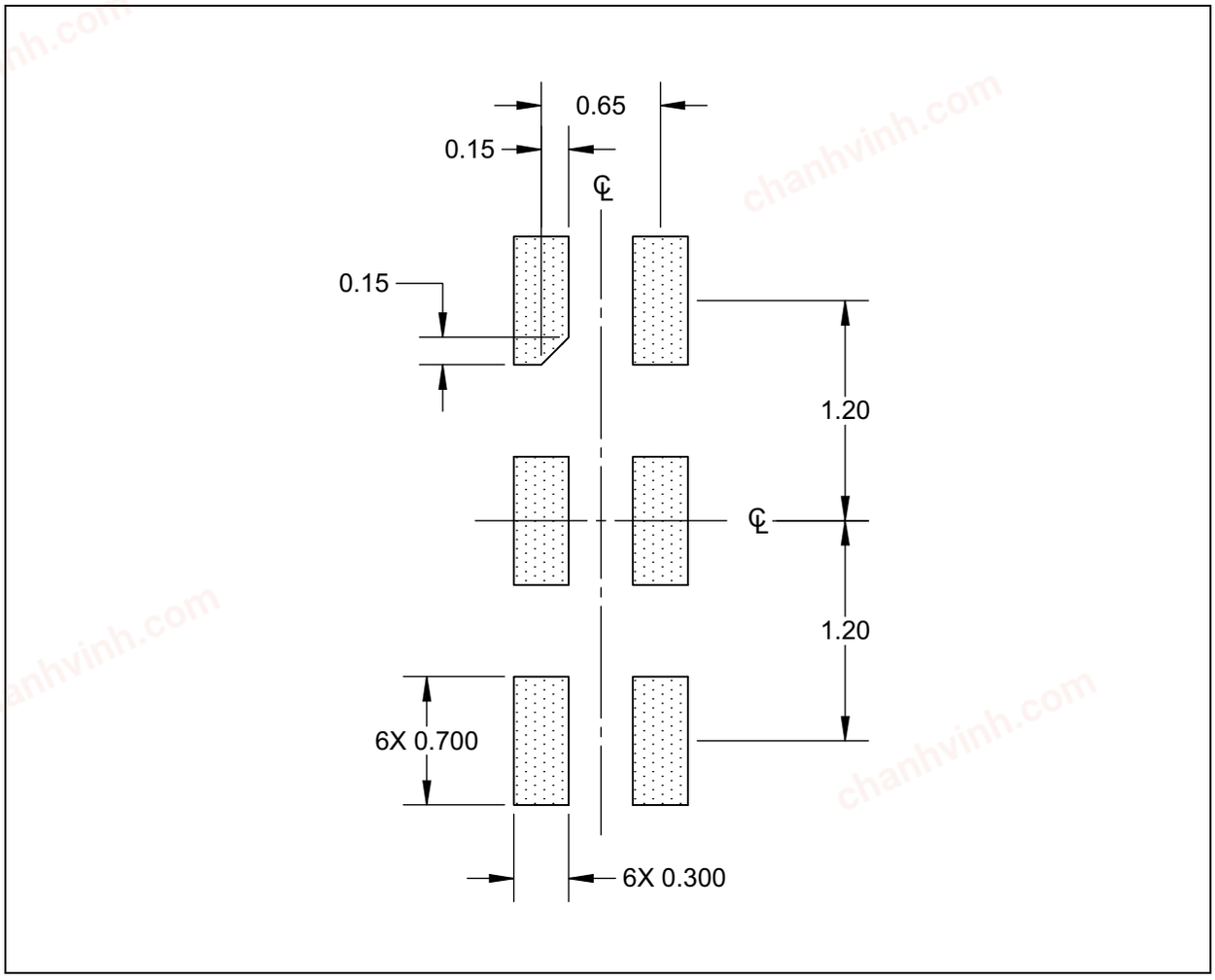
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## Recommended PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

**Figure 63:**
**Recommended PCB Pad Layout**




**Note(s):**

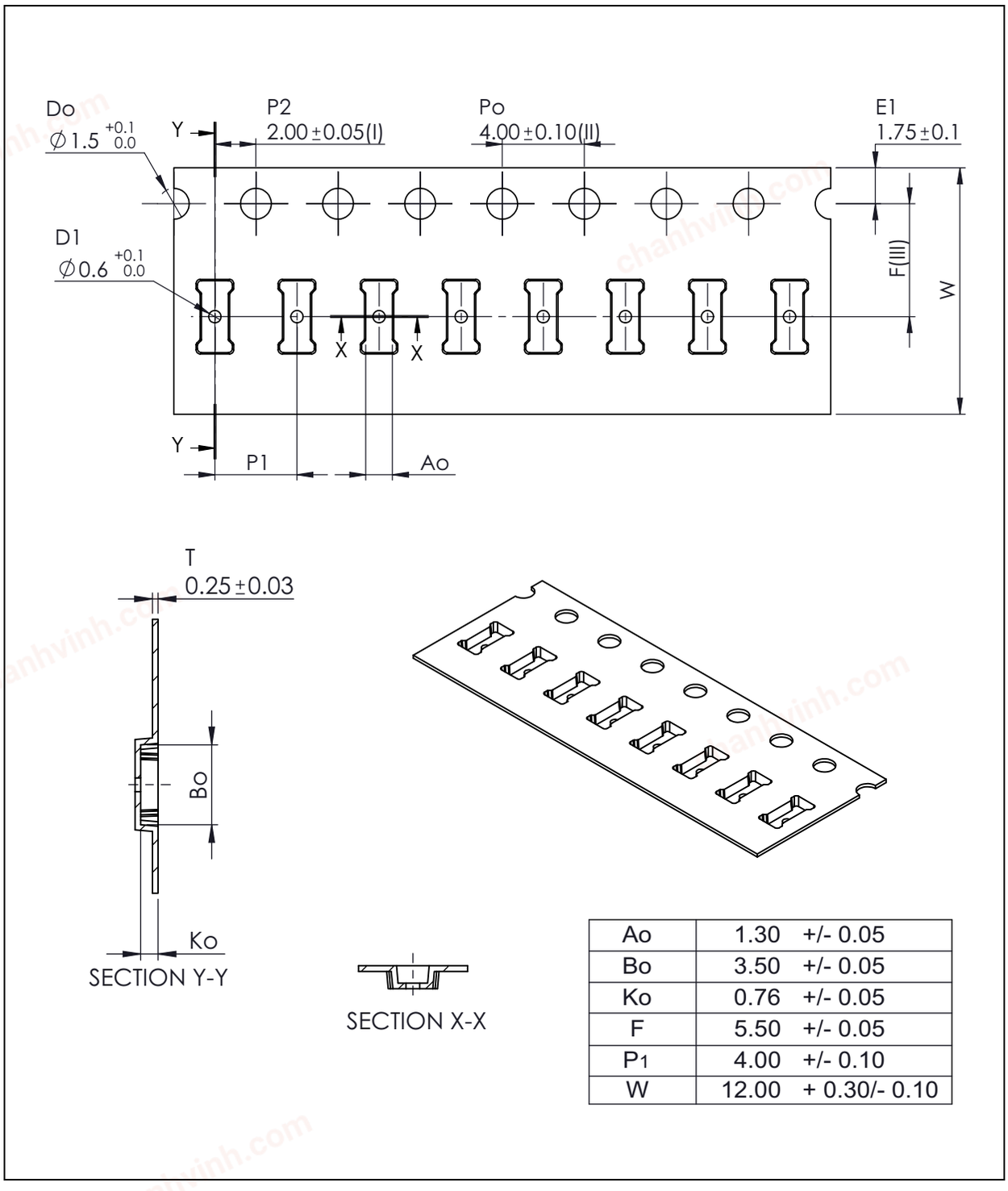
1. All Linear Dimensions are in millimeters.
2. Dimension tolerances are 0.05mm unless otherwise noted.
3. Contact finish is Au.
4. This drawing is subject to change without notice.

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# Tape & Reel Information

**Figure 64:**
**Tape and Reel Information**




| | |
|---|---|
| Ao | 1.30 +/- 0.05 |
| Bo | 3.50 +/- 0.05 |
| Ko | 0.76 +/- 0.05 |
| F | 5.50 +/- 0.05 |
| $P_1$ | 4.00 +/- 0.10 |
| W | 12.00 + 0.30/- 0.10 |

**Note(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001.
4. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
5. In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
6. This drawing is subject to change without notice.

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## Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure 65:**
**Solder Reflow Profile**

| Profile Feature Preheat/ Soak | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| Temperature Min ($T_{smin}$) | 100 °C | 150 °C |
| Temperature Max ($T_{smax}$) | 150 °C | 200 °C |
| Time ($t_s$) from ($T_{smin}$ to $T_{smax}$) | 60-120 seconds | 60-120 seconds |
| Ramp-up rate ($T_L$ to $T_P$) | 3 °C/second max. | 3 °C/second max. |
| Liquidous temperature ($T_L$)<br>Time ($t_L$) maintained above $T_L$ | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body temperature ($T_P$) | For users $T_P$ must not exceed the classification temp. of 235 °C.<br>For suppliers $T_P$ must equal or exceed the classification temp. of 235 °C | For users $T_P$ must not exceed the classification temp. of 260 °C.<br>For suppliers $T_P$ must equal or exceed the classification temp. of 260 °C |
| Time ($t_P$) (1) within 5 °C of the specified classification temperature ($T_C$) | 20 (1) seconds | 30 (1) seconds |
| Ramp-down rate ($T_P$ to $T_L$) | 6 °C/second max. | 6 °C/second max. |
| Time 25 °C to peak temperature | 6 minutes max. | 8 minutes max. |

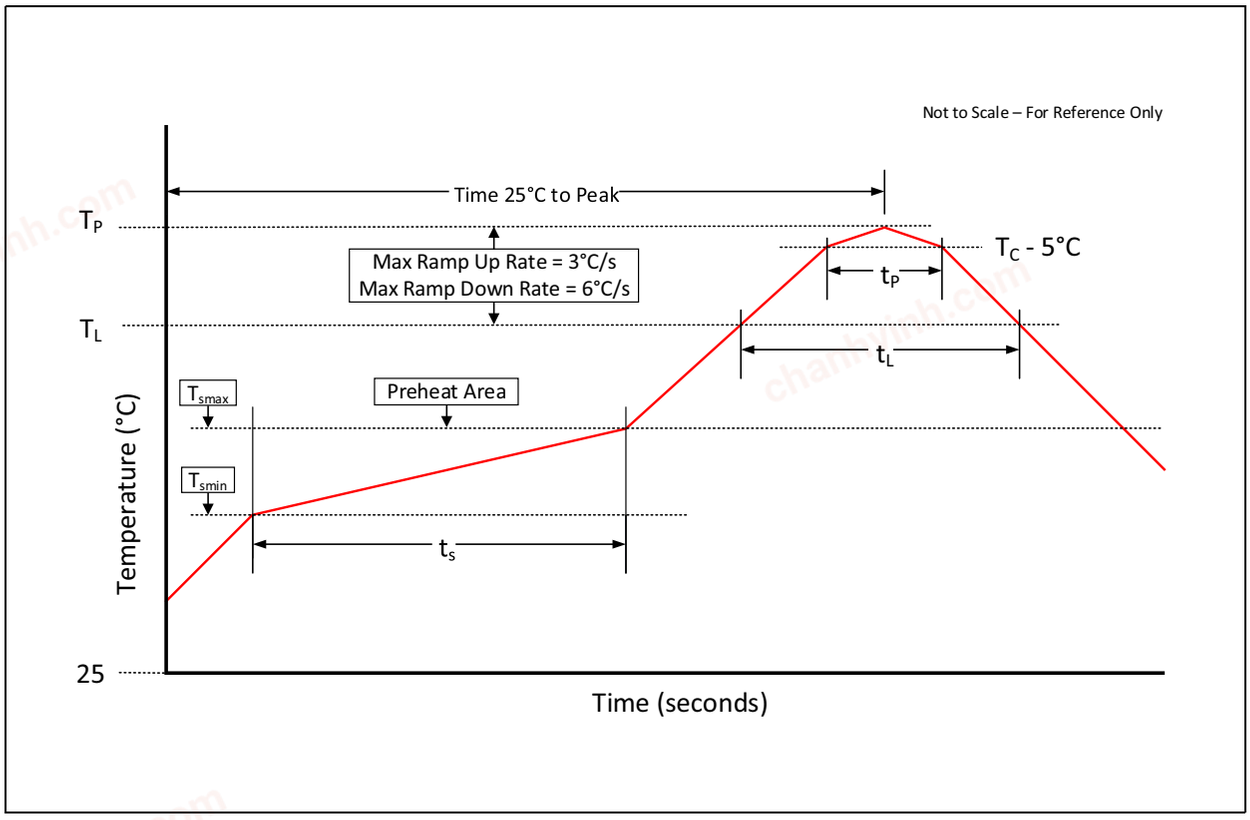
**Note(s):**

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

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**Figure 66:**
**Solder Reflow Profile Graph**




## Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

## Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

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## Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

## Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

## Laser Eye Safety

Complies with IEC/EN 60825-1:2014 and 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007

The TMD2755 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC/EN 60825-1:2014. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions or any physical modification to the module during development could result in hazardous levels of radiation exposure.



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# Ordering & Contact Information

**Figure 67:**
**Ordering Information**

| Ordering Code | I²C Bus | I²C Address | Delivery Form | Delivery Quantity |
|---|---|---|---|---|
| TMD27553 | 1.8V | 0x39 | Tape & Reel (13") | 10000 pcs/reel |
| TMD27553M | | | Tape & Reel (7") | 1000 pcs/reel |

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## Document Status

| Document Status | Product Status | Definition |
|---|---|---|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
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# Revision Information

| Changes from 1-03 (2020-Sep-15) to current revision 2-00 (2021-Sep-10) | Page |
|---|---|
| Removed “Confidential” | |

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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## Content Guide


**1 General Description**
1 Key Benefits & Features
2 Applications
2 Block Diagram

**3 Pin Assignments**
**4 Absolute Maximum Ratings**
**5 Electrical Characteristics**
**8 Typical Operating Characteristics**

**10 Detailed Description**
10 Proximity
10 Ambient Light Sensing, ALS
11 Operational State Diagram
12 $I^2C$ Characteristics
12 $I^2C$ Write Transaction
12 $I^2C$ Read Transaction
13 Timing Diagrams

**14 Register Description**
16 Detailed Register Description
16 Enable Register (Address 0x80)
17 ATIME Register (Address 0x81)
17 PRATE Register (Address 0x82)
18 AWTIME Register (Address 0x83)
18 AILTL Register (Address 0x84)
18 AILTH Register (Address 0x85)
19 AIHTL Register (Address 0x86)
19 AIHTH Register (Address 0x87)
20 PILTL Register (Address 0x88)
20 PILTH Register (Address 0x89)
21 PIHTL Register (Address 0x8A)
21 PIHTH Register (Address 0x8B)
22 PERS Register (Address 0x8C)
23 CFG0 Register (Address 0x8D)
23 PCFG0 Register (Address 0x8E)
25 PCFG1 Register (Address 0x8F)
25 PCFG2 Register (Address 0x90)
26 CFG1 Register (Address 0x91)
26 REVID Register (Address 0x92)
27 ID Register (Address 0x93)
27 STATUS Register (Address 0x94)
28 ALSL Register (Address 0x95)
28 ALSH Register (Address 0x96)
28 IRL Register (Address 0x97)
28 IRH Register (Address 0x98)
29 PDATAL Register (Address 0x99)
29 PDATAH Register (Address 0x9A)
30 REVID2 Register (Address 0xA6)
30 SOFTRST Register (Address 0xA8)
31 PWTIME Register (Address 0xA9)
31 CFG8 Register (Address 0xAA)
32 CFG3 Register (Address 0xAB)
32 CFG6 Register (Address 0xAE)

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33 POFFSETL Register (Address 0xC0)
33 POFFSETH Register (Address 0xC1)
34 CALIB Register (Address 0xD7)
35 CALIB_OFFSET Register (Address 0xD8)
36 CALIBCFG Register (Address 0xD9)
37 CALIBSTAT Register (Address 0xDC)
37 INTENAB Register (Address 0xDD)
38 FAC_L Register (Address 0xE6)
38 FAC_H Register (Address 0xE7)
38 TEST9 Register (Address 0xF9)

**39 Application Information**
39 Schematic (preliminary)
40 Recommended Circuit Layout

**41 Package Drawings & Markings**
42 Recommended PCB Pad Layout

**43 Tape & Reel Information**

**44 Soldering & Storage Information**
45 Storage Information
45 Shelf Life
46 Floor Life
46 Rebaking Instructions
46 Laser Eye Safety

**47 Ordering & Contact Information**
**48 RoHS Compliant & ams Green Statement**
**49 Copyrights & Disclaimer**
**50 Document Status**
**51 Revision Information**