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AS7261N

XYZ Tri-Stimulus and NIR Sensor with Electronic Shutter

General Description

The AS7261N provides direct XYZ sensor data which conforms to the tri-stimulus standard observer color response of the human eye. A near-IR channel enables additional application flexibility. LED drivers with programmable currents are provided for electronic shutter applications.

The AS7261N integrates Gaussian filters into standard CMOS silicon via nano-optic deposited interference filter technology and is packaged in an LGA package that provides a built in aperture to control the light entering the sensor array.

Control and spectral data access is implemented through an I^2C register set.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS7261N, XYZ Tri-Stimulus and NIR Sensor with Electronic Shutter are listed below:

Figure 1:
AS7261N Benefits and Features

Benefits	Features
• XYZ channel data conforming to human eye response to color information	• XYZ tri-stimulus standard observer filter set
• High accuracy ambient light measurements	• Ambient light sensing (photopic response)
• Direct register read and write with interrupt on sensor ready	• I^2C slave digital Interface with optional interrupt operation
• High stability over lifetime with minimal drift over temperature	• Filter set realized by silicon interference filters
• No additional signal conditioning required	• 16-bit ADC with digital access
• Direct register read and write with interrupt on sensor ready	• I^2C slave digital Interface with optional interrupt operation

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Benefits	Features
• Electronic shutter control/synchronization	• Programmable LED drivers
• Low voltage operation	• 2.7V to 3.6V with I²C interface
• Small, robust package, with built-in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm -40°C to 85°C temperature range

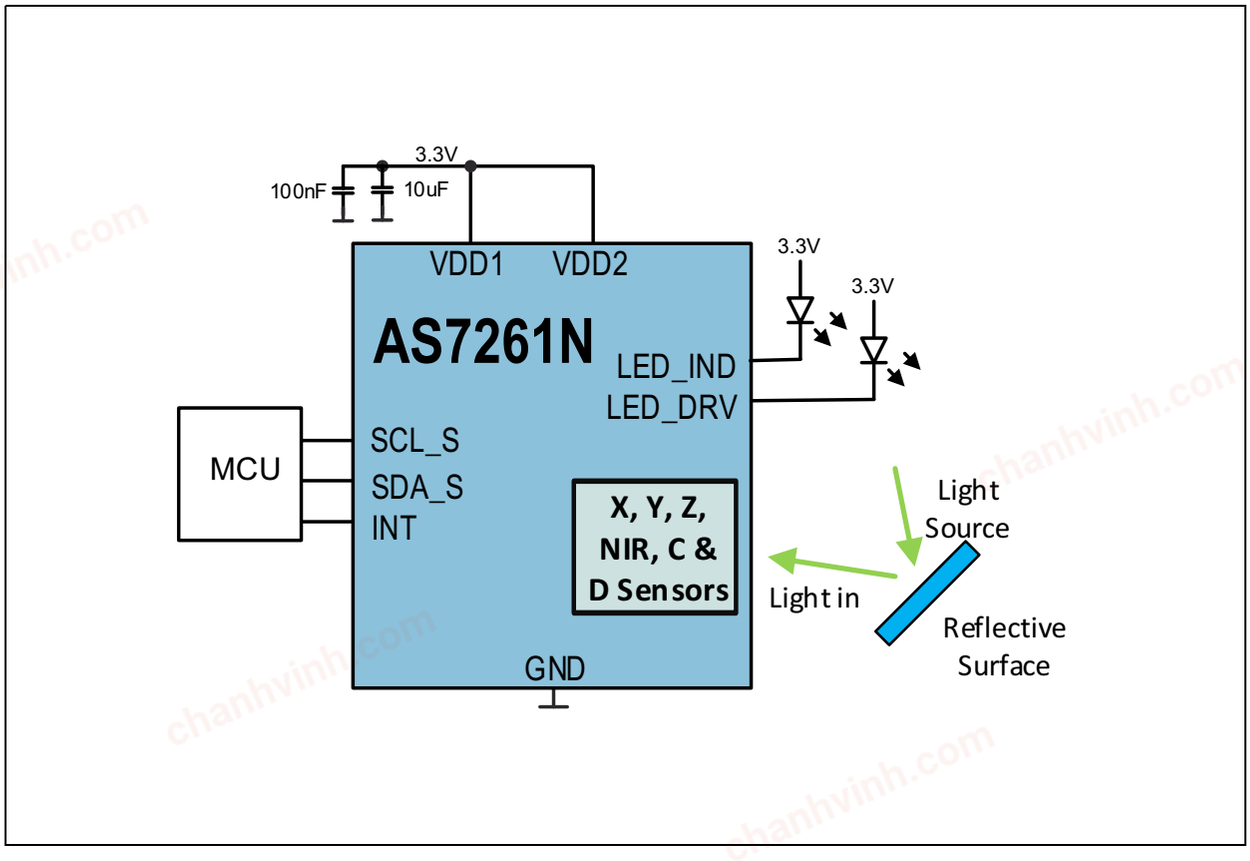
Application

The AS7261N applications include:

- Color measurement and absorbance
- Color matching and identification
- Precision color tuning/calibration

System Block Diagram

Figure 2:
AS7261N Sensor System

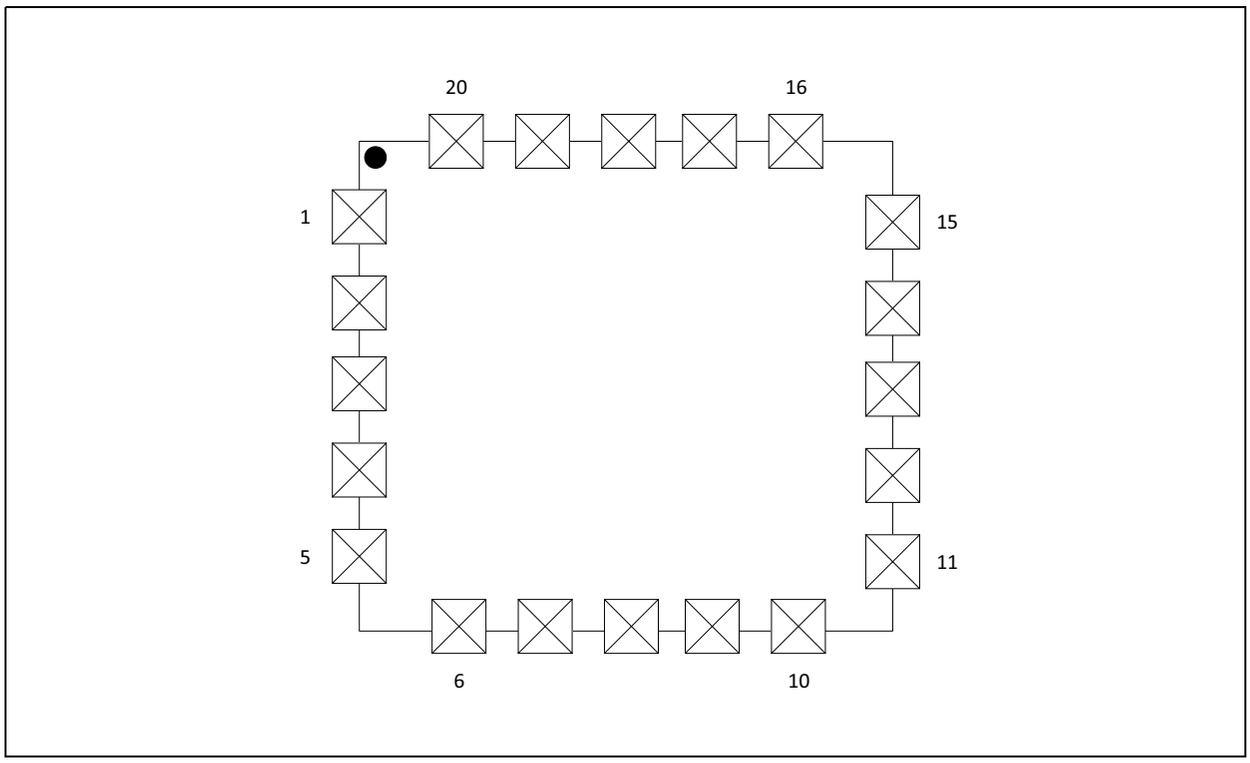


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Pin Assignments

The device pin assignments are described below.

Figure 3:
Pin Diagram of AS7261N (Top View)



Pin Description

Figure 4:
Pin Description of AS7261N

Pin Number	Pin Name	Description
1	NF	Not Functional. Do not connect.
2	RESN	Reset, Active LOW
3	NF	Not Functional. Do not connect.
4	NF	Not Functional. Do not connect.
5	NF	Not Functional. Do not connect.
6	NF	Not Functional. Do not connect.
7	NF	Not Functional. Do not connect.
8	NF	Not Functional. Do not connect.
9	SCL_S	I^2C Slave Clock pin
10	SDA_S	I^2C Slave Data pin
11	NF	Not Functional. Do not connect.

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Pin Number	Pin Name	Description
12	NF	Not Functional. Do not connect.
13	INT	Interrupt, active high
14	VDD2	Voltage Supply
15	LED_DRV	LED Driver Output for Driving LED Current Sink
16	GND	Ground
17	VDD1	Voltage Supply
18	LED_IND	LED Driver Output for Indicator LED Current Sink
19	NF	Not Functional. Do not connect.
20	NF	Not Functional. Do not connect.

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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD_MAX}	Supply Voltages VDD1, VDD2	-0.3	5	V	Pins VDD1 & VDD2 must be sourced from the same supply voltage
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD+0.3	V	Input/Output Pin to GND
I_{SCR}	Input Current (latch-up immunity)	±100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±500		V	JSD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168 hours

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Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. VDD1 and VDD2 must be sourced from the same power supply.

Figure 6:
Electrical Characteristics of AS7261N

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD	Voltage Operating Supply	I²C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
$I_{STANDBY}$ (1)	Standby Current			12		µA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER} (2)	Internal Clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current	1, 2, 4 or 8	1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED Current	12.5, 25, 50 or 100	12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
$I_{IL\ RESN}$	Logic Input Current (RESN pin)	Vin=0V	-1		-0.2	mA
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD - 0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE} (2)	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL} (2)	Current Fall Time	C(Pad)=30pF			5	ns

Note(s):

1. 15µA over temperature
2. Guaranteed, not tested in production

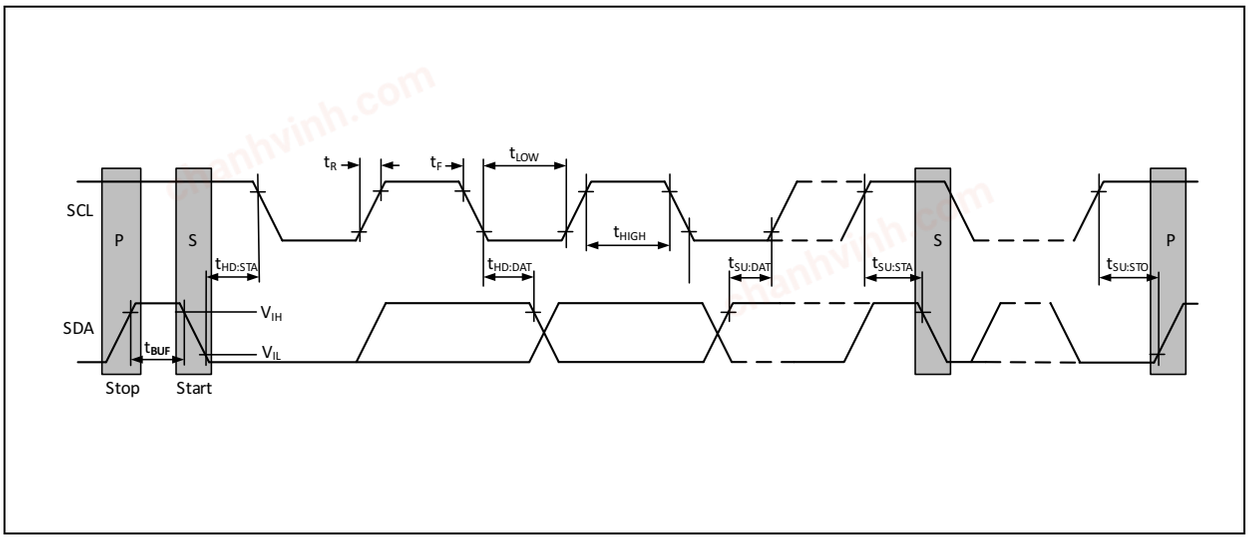
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Timing Characteristics

Figure 7:
AS7261N I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HS:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HS:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Slave Timing Diagram



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Operation Characteristics

Figure 9:
Spectral Responsivity

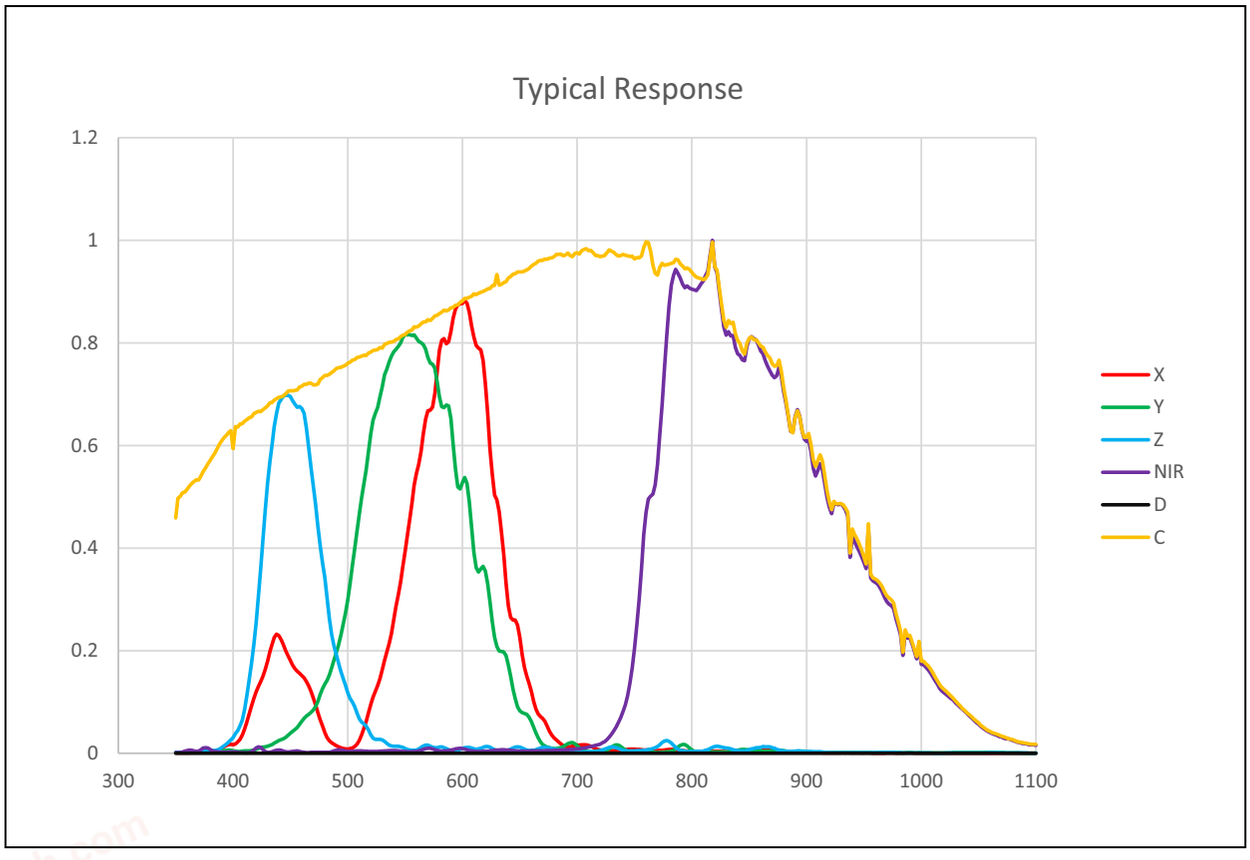


Figure 10:
AS7261N Optical Characteristics (Pass Band)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
X	Channel X	White LED 5700K source, Ee=116µW/cm^2		7.7		counts/ (µW/cm^2)
Y	Channel Y	White LED 5700K source, Ee=116µW/cm^2		8.6		counts/ (µW/cm^2)
Z	Channel Z	White LED 5700K source, Ee=116µW/cm^2		4.7		counts/ (µW/cm^2)
NIR	Channel NIR	Incandescent light source, Ee=465µW/cm^2		14.0		counts/ (µW/cm^2)
C	Channel C	White LED 5700K source, Ee=116µW/cm^2		18.1		counts/ (µW/cm^2)
D_LED	Channel D	White LED 5700K source, Ee=116µW/cm^2		0	15	counts
D_INCAN	Channel D	Incandescent light source, Ee=465µW/cm^2			15	counts

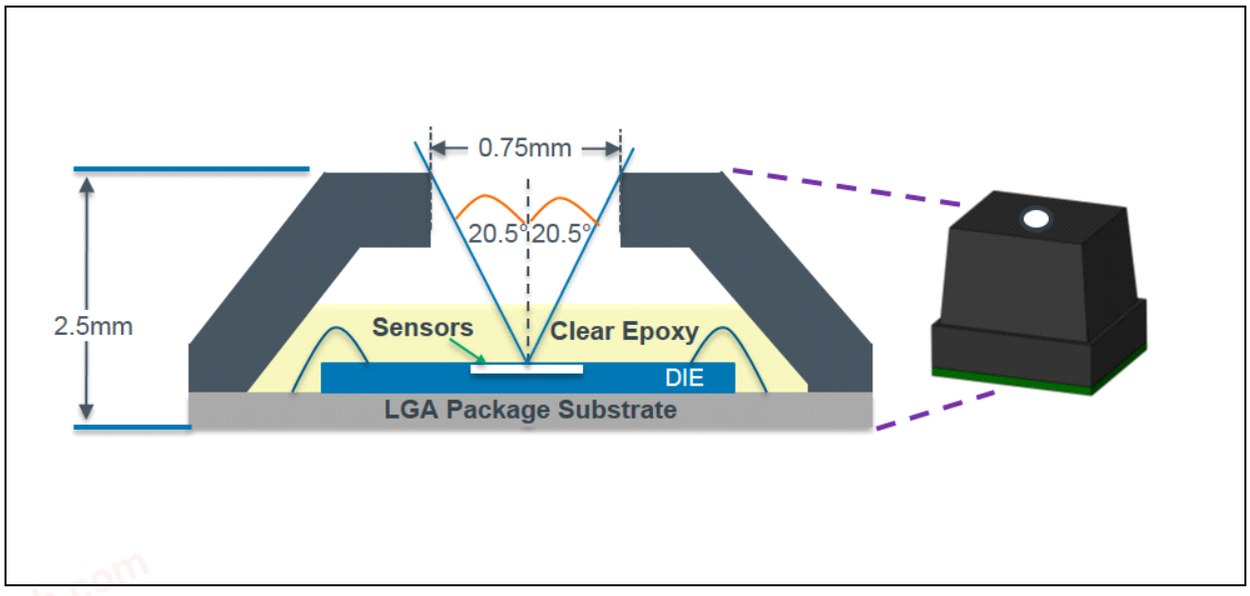
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Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PFOV	Package Field of View			±20.5		deg

Note(s):

1. Each channel is tested with GAIN = 3.7x, Integration Time (INT_T) = 166ms and T_{AMB}=25°C
2. The accuracy of each channel count is ±25%

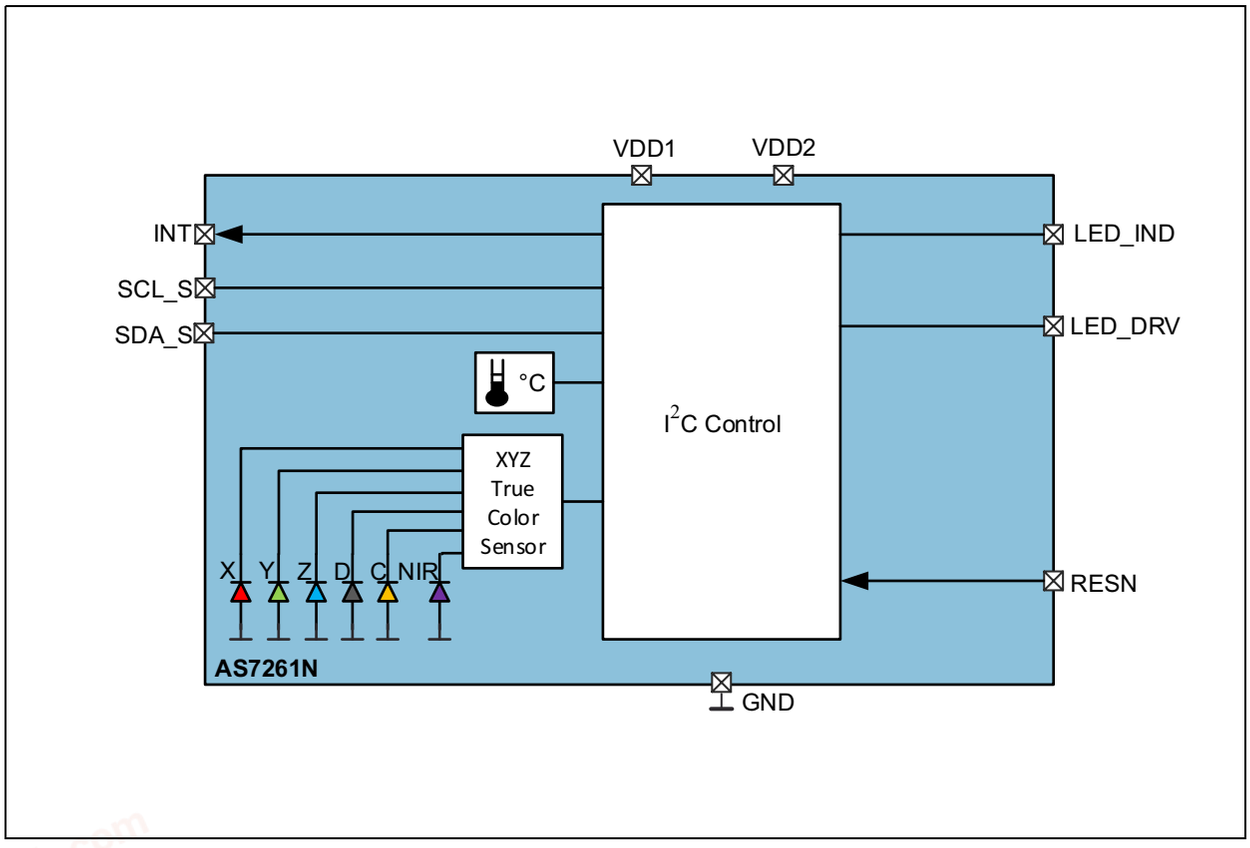
Figure 11:
AS7261N LGA Package Field of View



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Detailed Descriptions

Figure 12:
Internal Block Diagram



XYZ Sensor

The AS7261N XYZ sensor is a next-generation digital color sensor device. It senses X, Y, Z standard observer filters compliant with the CIE 1931 standard observer color response in addition to near IR (NIR), Clear (C) and Dark (D) spectrum filters.

The sensor contains analog-to-digital converters (16-bit resolution ADC), which integrate current from each channel's photodiode. Upon completion of conversion cycle, the integrated result is transferred to the corresponding data register. Transfers are double-buffered to ensure integrity of the data is maintained.

Interference filters realize all filter responses and enable minimal life-time drift and very high temperature stability. Filter accuracy is affected by the optical angle of incidence which itself is limited by an integrated aperture and an internal micro-lens structure in the AS7261N. The package field of view (PFOV) is ±20.5° to deliver the specified accuracy. External optics can be used as needed to expand or reduce this built in PFOV.

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Data Conversion

AS7261N spectral conversion is implemented via two photodiode banks. The first bank provides data from the X, Y, Z and NIR (near-IR) photodiodes. The second bank provides data from the same X and Y photodiodes as well as D (Dark) and C (Clear) photodiodes.

The spectral conversion process is controlled with two BANK Mode settings. Bank Mode 0 uses I²C registers for X, Y, D and C data. Bank Mode 1 uses I²C registers for X, Y, Z and NIR data. Sensor data is available in four I²C registers (NDATAL/NDATAH, XDATAL/XDATAH, YDATAL/YDATAH and ZDATAL/ZDATAH) as shown in the figures below.

Figure 13:
Bank Modes

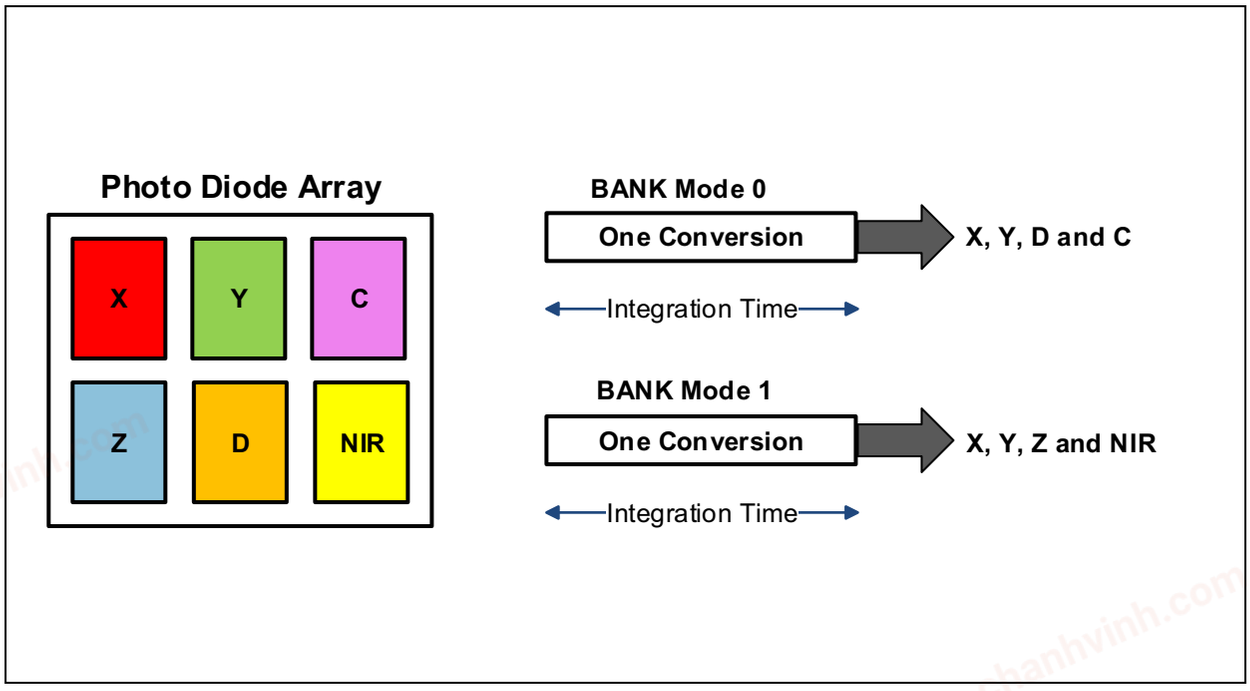


Figure 14:
AS7261N Sensor Data I²C Registers

I²C Register	Bank Mode 0	Bank Mode 1
NDATAL/NDATAH	C	NIR
XDATAL/XDATAH	X	X
YDATAL/YDATAH	Y	Y
ZDATAL/ZDATAH	D	Z

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Spectral Conversion and Data Acquisition

Spectral conversion uses a register set for integration time (register INT_T). If both photodiode banks are required to complete the conversion, the second bank requires an additional integration time. Minimum conversion time for a single bank is 2.8 milliseconds. If data is required from all 6 photodiodes the device must perform 2 full conversions (2 x integration time). The user has control of gain for the photodiode current, programmed into bits 0 and 1 of the GAIN_IDRV register where gain can be set to 1x, 3.7x, 16x or 64x. A wait time between integration cycles can be programmed into register WTIME using the same units as the INT_T register.

An auto zero function is automatically performed before the first data conversion after a power-on or reset, in order to achieve the best data quality. Auto zero corrects for internal device temperature. But since it's automatically done only once, it can also be manually run. Typically, if the temperature changes by 15 degrees C or more the auto zero should be manually run by writing to the Auto_Zero register (temperature is user calculated based on TMPL & TMPH registers values). But auto zero can also be manually done before every conversion. When auto zero function is complete the DONE bit (bit7) of Auto_Zero register will be set to 1.

The BANK bit (bit7) in the BANK register can be changed as needed before data conversion to acquire the desired channels. While conversion is continuous, timing is done using registers. Both polling and interrupt operation are then supported for "conversion complete" timing. Both require programming the INTR_POLL_EN register bit 2 to a 1. The conversion process is started by writing a 0x01 to the DATA_EN register followed by clearing any previous Data Valid bit in the INTR_POLL_CLR register. This is followed by a separate write of 0x03 to the DATA_EN register.

If the AS7261N interrupt output is to be used for data conversion timing the INTR_PIN_Config register should be programmed to 0xCA. The INT pin will then be asserted high at the completion of the conversion cycle. A 0x04 should be written to the INTR_POLL_CLR register to clear this interrupt which also clears polling bit 2 in the register.

If only polling is to be used for conversion timing, an external interrupt is not required and the INTR_PIN_Config register should be programmed to 0x00. Polling of bit 2 in the INTR_POLL_CLR register will return 0x00 if the conversion is not complete, and 0x04 if complete. Once complete a 0x04 should be written to the INTR_POLL_CLR register to clear bit 2, the polled bit.

For acquisition, done after conversion, data needs to be latched by writing 0x83 to the DATA_EN register. The purpose of latching the data by the user is to provide a mechanism for data to be coherent and under user control. Now, the data bank register can be read (one bank per single conversion-acquisition cycle). The CLR bit (bit2) should be

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cleared by writing a 1 to the CLR bit (bit2) of the INTR_POLL_CLR register (0xF8) after each conversion-acquisition cycle is completed.

Temperature Sensor

The Temperature Sensor measures on-chip temperature on demand, and enables temperature compensation procedures. The basic equation for calculating the internal temperature of the device is:

(EQ1)
$$\frac{0.7604 - \frac{TMP_\ VALUE \bullet 2.048}{1024}}{2.046 \bullet 10^{-3}} - 40$$

TMP_VALUE is the derived from TMPL & TMPH (0xD2 [1:0] and 0xD1 [7:0]) register data. Temperature conversions are performed by writing 0x24 to the TMP_Config register. Polling the TMP_Config register will indicate data acquisition is complete upon reading 0x84. After reading 0x84 the TMP_Config register should be written to either 0x00 for idle or 0x24 to perform another temperature measurement. The result of the calculation is the device temperature in degree Celsius (°C).

Electronic Shutter with LED_IND or LED_DRV Driver Control

Under user control there are two LED driver outputs that can be used to control LEDs on the two driver pins. This allows different wavelength light sources to be used in the same system. The LED output sink currents are programmable and can drive external LED sources. After programming for current the sources can be turned off and on via registers to provide the AS7261N with an electronic shutter capability. If turning LEDs on, they should be fully on optically before a conversion begins and not shut off until after the conversion-acquisition cycle completes

The LED_IND pin can be turned on/off via the LED_IND register with values 0x01, 0x05, 0x09 and 0x0D for sink currents of 1mA, 2mA, 4mA and 8mA respectively.

For the LED_DRV pin, the GAIN_IDRV Register (0xB9) bits 7 and 6 control the drive strength of the pin for current values 12.5mA, 25mA, 50mA and 100mA. This register also controls the gain of all light acquisitions so care should be taken when writing to it. The LED_DRV pin can be turned on/off via the LED_DRV register bit 2.

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Low Power Mode

AS7261N can be put into the low power mode by writing 0x02 to the POWER MODE Register (0x73). Write 0x00 to set it back to normal mode. Wait at least 50µs before doing further AS7261N operations after powering back to normal.

The sequence to configure AS7261N into low power mode:

- Write 0x00 to Register 0xFA
- Write 0x02 to Register 0x73
- AS7261N is in low power mode

The sequence to configure AS7261N out of low power mode:

- Write 0x00 to Register 0x73
- Wait for at least 50µS
- Write 0x03 to Register 0xFA
- AS7261N is in normal mode

Device Initialization and Pin Assignment

On power up device needs to be initialized as follows before programming registers to do data conversion and acquisition:

- Device Config 1 register: 0x70 written to 0x8A
- Device Config 2 register: 0x71 written to 0x02
- Device Config 3 register: 0xB0 written to 0x02
- Device Config 4 register: 0x88 written to 0x00
- Device Config 5 register: 0x9A written to 0x02
- Interrupt Operation: The only user defined pin functionality is whether to use pin 13 as an interrupt signal at the completion of data conversion. This is done by programming the INTR_PIN_Config register (0x22) to 0xCA. To disable interrupt function the INTR_PIN_Config register should be programmed to 0x00, which is the power-on and reset default.

RC Oscillator

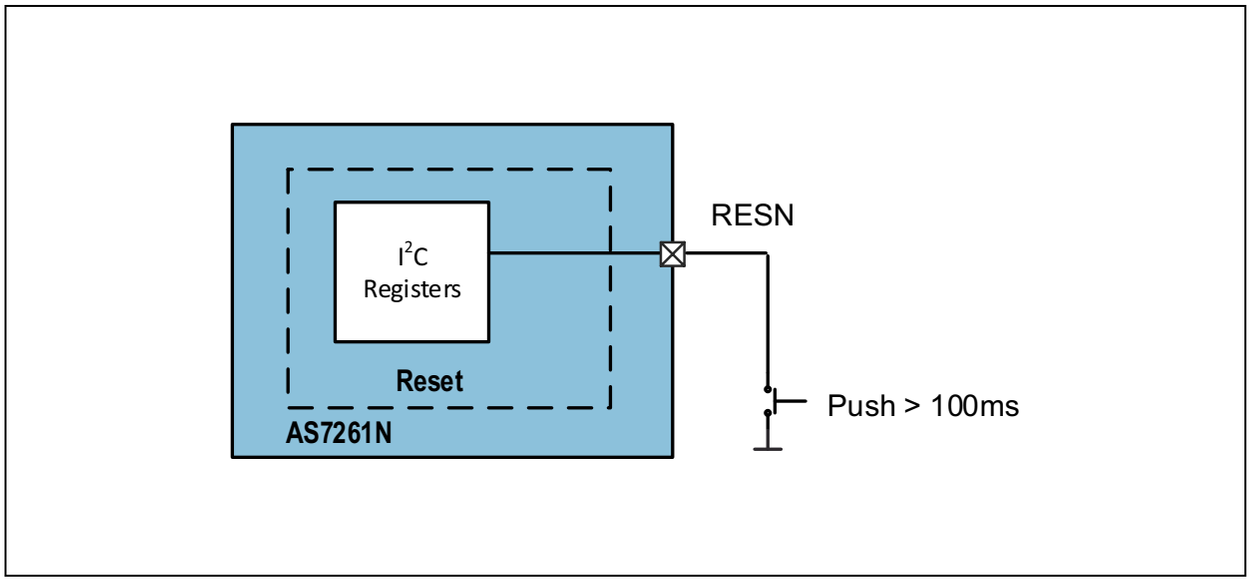
An internal on-chip timing generation circuit provides a 16MHz temperature compensated oscillator for the AS7261N master clock.

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Reset

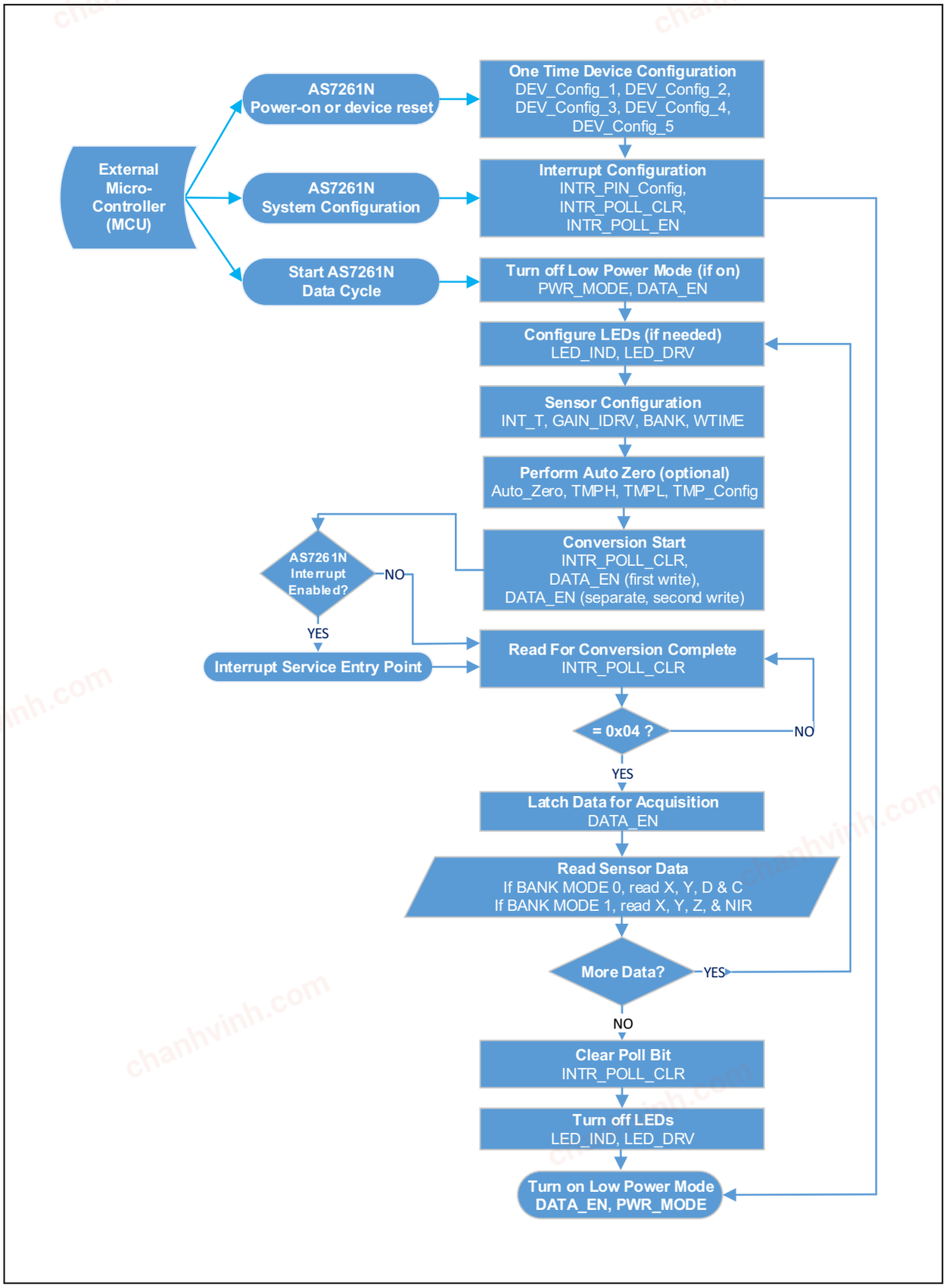
Pulling down the RESN pin for longer than 100ms resets the AS7261N.

Figure 15:
Reset Circuit



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Figure 16:
I²C Register Programming Flow Chart



Note(s):

1. When using shuttered LEDs, the LED source(s) should be at desired brightness before conversion starts.

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I²C Slave Interface

Interface, control and reading sensor data is accomplished through an I²C compatible slave interface via a set of registers.

I²C Feature List

- Fast mode (400 kHz) and standard mode (100 kHz) support
- 7+1-bit addressing mode
- Write format: Byte
- Read format: Byte

I²C Register Set

The 7-bit I²C slave address of AS7261N is 0x49 plus one bit for read/write. When reading from I²C registers, the 7 + 1-bit address should be 0x93. When writing to I²C registers, the 7+1-bit address should be 0x92.

The figure below provides a summary of the AS7261N I²C register set. Figures after that provide additional details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lower register address).

I²C register addresses not listed should be treated as reserved and not used.

Figure 17:
I²C Register Set Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Device Version Registers									
0x10	DEV_ID	Device Identification							
0x11	DEV_VER	Device Version							
Device Configuration Registers									
0x70	DEV_Config_1	Device Configuration 1							
0x71	DEV_Config_2	Device Configuration 2							
0xB0	DEV_Config_3	Device Configuration 3							
0x88	DEV_Config_4	Device Configuration 4							
0x9A	DEV_Config_5	Device Configuration 5							
Power Mode Register									
0x73	PWR_MODE	RESV						PM	RESV

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Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Interrupt and Polling Control Registers									
0x22	INTR_PIN_Config	OPIN		FUNCT					
0xF8	INTR_POLL_CLR	RESV					CLR	RESV	
0xF9	INTR_POLL_EN	RESV					EN	RESV	
LED Control Registers									
0xEA	LED_DRV	RESV					ON_OFF	RESV	
0x84	LED_IND	RESV				CURRENT		RESV	ON_OFF
Auto Zero and Temperature Control Registers									
0xBA	Auto_Zero	RESV				C_EN	X_EN	Y_EN	Z_EN
0xD1	TMPH	Most Significant bits (9:2) of Temperature Measurement							
0xD2	TMPL	RESV						TMPL	
0xD3	TMP_Config	ISTAT	RESVSTRT		RESV	SRC			
Sensor Control Registers									
0xDB	BANK	BANK	RESV						
0xB9	GAIN_IDRV	IDRV		RESV				GAIN	
0xD9	INT_T	Integration Time							
0xDA	WTIME	Wait Time							
0xFA	DATA_EN	DL	RESV			WAIT	RESV	CON	PON
Sensor Data Registers									
0xDC	NDATA_L	N Channel Low Byte							
0xDD	NDATA_H	N Channel High Byte							
0xDE	YDATA_L	Y Channel Low Byte							
0xDF	YDATA_H	Y Channel High Byte							
0xEC	ZDATA_L	Z Channel Low Byte							
0xED	ZDATA_H	Z Channel High Byte							
0xEE	XDATA_L	X Channel Low Byte							
0xEF	XDATA_H	X Channel High Byte							

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Detailed Register Description

Figure 18:
Device ID and Version Registers

Addr: 0x01		Device Identification		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_ID	01110010	R	Device identification number
Addr: 0x11		**Device Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_VER		R	Device version number

Figure 19:
Device Configuration Registers

Addr: 0x70		Device Configuration 1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_Config_1		R/W	Device Configuration 1, must be initialized to 0x8A by external MCU
Addr: 0x71		**Device Configuration 2**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_Config_2		R/W	Device Configuration 1, must be initialized to 0x02 by external MCU
Addr: 0xB0		**Device Configuration 3**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_Config_3		R/W	Device Configuration 1, must be initialized to 0x02 by external MCU
Addr: 0x88		**Device Configuration 4**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_Config_4		R/W	Device Configuration 1, must be initialized to 0x00 by external MCU
Addr: 0x9A		**Device Configuration 5**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DEV_Config_5		R/W	Device Configuration 1, must be initialized to 0x02 by external MCU

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Figure 20:
Power Mode Register

Addr: 0x04/0x84		PWR_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	RESV	0	R/W	Reserved, set to 000000 if writing the register
1	PM	1	R/W	1= Normal Operation Power Mode 0= Low Power Mode
0	RSVD	0	R/W	Reserved, set to 0 if writing the register

Figure 21:
Interrupt Pin Configuration Register

Addr: 0x22		INTR_PIN_Config		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INTR_PIN_Config	0x00	R/W	0x00 = INT pin disabled 0xCA = INT pin enabled

Figure 22:
Interrupt and Polling Clear Register

Addr: 0xF8		INTR_POLL_CLR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	RESV	00000	R/W	Reserved, set to 00000 if writing the register
2	CLR	0	R/W	Set to 1 to clear any asserted interrupt pin INT (the interrupt channel ready must be enabled). If the interrupt channel ready is enabled this bit will read a 1.
1:0	RSVD	00	R/W	Reserved, set to 00 if writing the register

Figure 23:
Interrupt and Polling Enable Register

Addr: 0xF9		INT_POLL_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	RESV	0	R/W	Reserved, set to 00000 if writing the register
2:1	EN	0	R/W	Set to 1 to enable the channel data ready for polling or interrupt.
0	RSVD	0	R/W	Reserved, set to 0 if writing the register

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Figure 24:
LED Driver Register

Addr: 0xEA		LED_DRV		
Bit	Bit Name	Default	Access	Bit Description
7:3	RESV	0	R/W	Reserved, set to 00000 if writing the register
2	ON_OFF	0	R/W	Set to 1 to enable the LED_DRV pin to the current level specified by the register GAIN_IDRV (0xB9). Set to 0 to turn off.
0:1	RSVD	0	R/W	Reserved, set to 00 if writing the register

Figure 25:
LED Indicator Register

Addr: 0x84		LED_IND		
Bit	Bit Name	Default	Access	Bit Description
7:4	RESV	0	R/W	Reserved, set to 0 if writing the register
3:2	CURRENT	00	R/W	For LED_IND pin current value (when on). Set to: ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8mA;
1	RSVD	0	R/W	Reserved, set to 0 if writing the register
0	ON_OFF	0	R/W	Set to 1 to enable the LED_DRV pin to the current level specified by the CURRENT bits. Set to 0 to turn off.

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Figure 26:
Auto Zero Register

Addr: 0xBA		Auto_Zero		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DONE	0	R/W	Will be set to 1 when any auto zero function is completed. Set to 0 if writing to the register.
6:4	RESV	0	R/W	Reserved, set to 000 if writing the register
3	C_EN	0	R/W	Set to 1 to manually run auto zero on the C channel. Will be automatically set to 0 when DONE bit is set.
2	X_EN	0	R/W	Set to 1 to manually run auto zero on the X channel. Will be automatically set to 0 when DONE bit is set.
1	Y_EN	0	R/W	Set to 1 to manually run auto zero on the Y channel. Will be automatically set to 0 when DONE bit is set.
0	Z_EN	0	R/W	Set to 1 to manually run auto zero on the Z channel. Will be automatically set to 0 when DONE bit is set.

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Temperature Measurement High Register (bits 9:2)

TMP_VALUE is the value from TMPL & TMPH (0xD2 [1:0] and 0xD1 [7:0]) registers (see the Temperature Sensor section of this datasheet). Temperature conversion controlled by the TEMP_ Config register.

Figure 27:
Temperature Measurement High Register

Addr: 0xD1		TMPH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TMPH		R	Most significant 8 bits (9:2) of the Temperature Measurement.

Temperature Measurement Low Register (bits 1:0)

TMP_VALUE is the value from TMPL & TMPH (0xD2 [1:0] and 0xD1 [7:0]) registers (see the Temperature Sensor section of this datasheet). Temperature conversion controlled by the TEMP_ Config register.

Figure 28:
Temperature Measurement Low Register

Addr: 0xD2		TMPL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TMPL		R	Least significant 2 bits (1:0) of the Temperature Measurement.

Figure 29:
Temperature Configure Register

Addr: 0xD3		TEMP_Config		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ISTAT	0	R/W	Will be set to 1 when internal temperature measurement is complete. Set to 0 if writing to the register.
6	RESV	0	R/W	Reserved, set to 0 if writing the register
5	START	0	R/W	Set to 1 to start a temperature conversion cycle. Set to 0 for IDLE state.
4	RESV	0	R/W	Reserved, set to 0 if writing the register
3:0	SRC	0	R/W	Set to 0100 to start a temperature conversion cycle. Set to 0000 for IDLE state.

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Figure 30:
Bank Register

Addr: 0xDB		BANK		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BANK	0	R/W	Sets Bank mode for sensor channel selection: 0= Mode 0 for X, Y, D and D sensor data 1= Mode 1 for X, Y, Z and NIR sensor data
6:0	RESV	0	R/W	Reserved, set to 0000000 if writing the register

Figure 31:
Sensor Gain and LED_DRV Current Drive Register

Addr: 0xB9		GAIN_IDRV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	IDRV	0	R/W	For LED_DRV pin current limit (when on). Set to: 'b00=100mA; 'b01=50mA; 'b10=25mA; 'b11=12.5mA;
5:2	RESV	0	R/W	Reserved, set to 0000 if writing the register
1:0	GAIN	0	R/W	Sensor Channel Gain Setting (all channels) 'b00=1x; 'b01=3.7x; 'b10=16x; 'b11=64x;

Figure 32:
Integration Time Register

Addr: 0xD9		INT_T		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_T	0xFF	R/W	Sets sensor integration time Integration time = (256 - value) * 2.8ms

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Figure 33:
Integration Wait Time Register

Addr: 0xDA		INT_WT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_WT	0xFF	R/W	Sets time between sensor integrations Integration wait time = (256 - value) * 2.8ms

Figure 34:
Data Enable Register

Addr: 0xFA		DATA_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DL	0	R/W	Data Latch. Set to 1 to latch the data after acquisition completes
6:4	RESV	0	R/W	Reserved, set to 000 if writing the register
3	WAIT	0	R/W	Set to 1 to enable the wait timer between data channel acquisitions
2	RESV	0	R/W	Reserved, set to 0 if writing the register
1	CON	0	R/W	Set to 1 to enable data channel acquisitions
0	PON	0	R/W	Set to 1 if writing the register

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Figure 35:
Sensor Data Registers

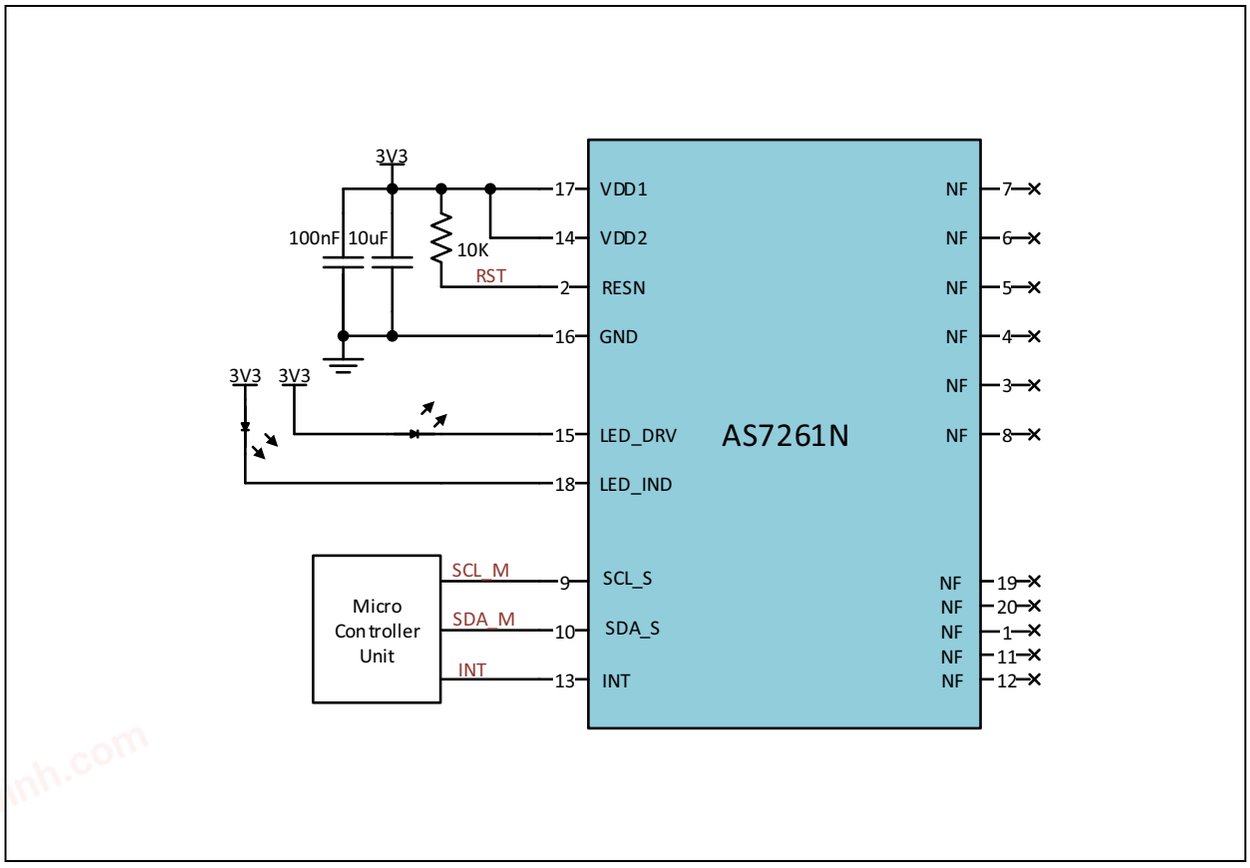
Addr: 0xDC		NDATA_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	NDATA_L		R	Channel N Low Data Byte
Addr: 0xDD		NDATA_H		
Bit	Bit Name	Default	Access	Bit Description
7:0	NDATA_H		R	Channel N High Data Byte
Addr: 0xDE		YDATA_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	YDATA_L		R	Channel Y Low Data Byte
Addr: 0xDF		YDATA_H		
Bit	Bit Name	Default	Access	Bit Description
7:0	YDATA_H		R	Channel Y High Data Byte
Addr: 0xEC		ZDATA_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	ZDATA_L		R	Channel Z Low Data Byte
Addr: 0xED		ZDATA_H		
Bit	Bit Name	Default	Access	Bit Description
7:0	ZDATA_H		R	Channel Z High Data Byte
Addr: 0xEE		XDATA_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	XDATA_L		R	Channel X Low Data Byte
Addr: 0xEF		XDATA_H		
Bit	Bit Name	Default	Access	Bit Description
7:0	XDATA_H		R	Channel X High Data Byte

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Application Information

Schematic

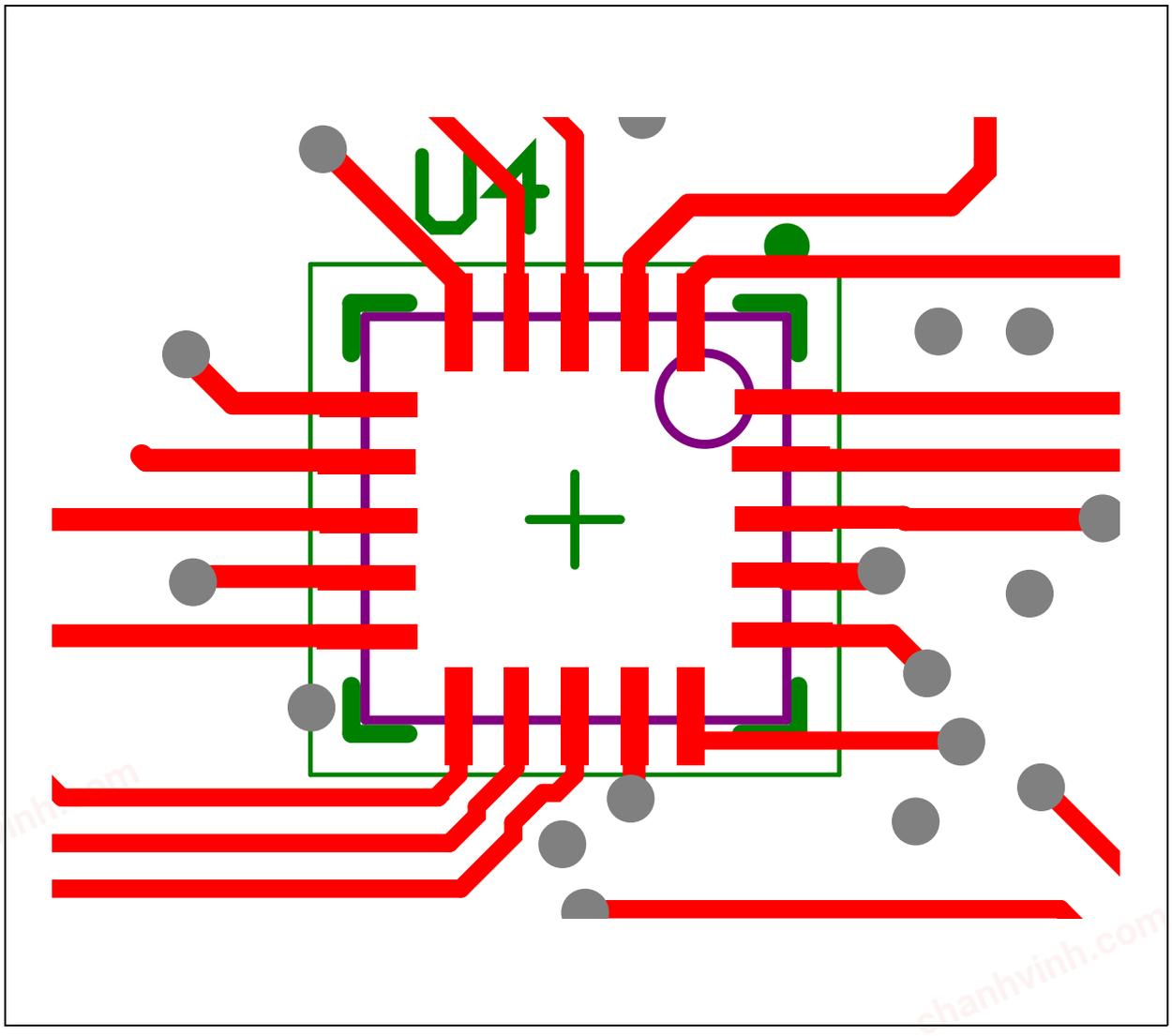
Figure 36:
AS7261N Typical Application Circuit



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PCB Layout

Figure 37:
Typical Layout Routing

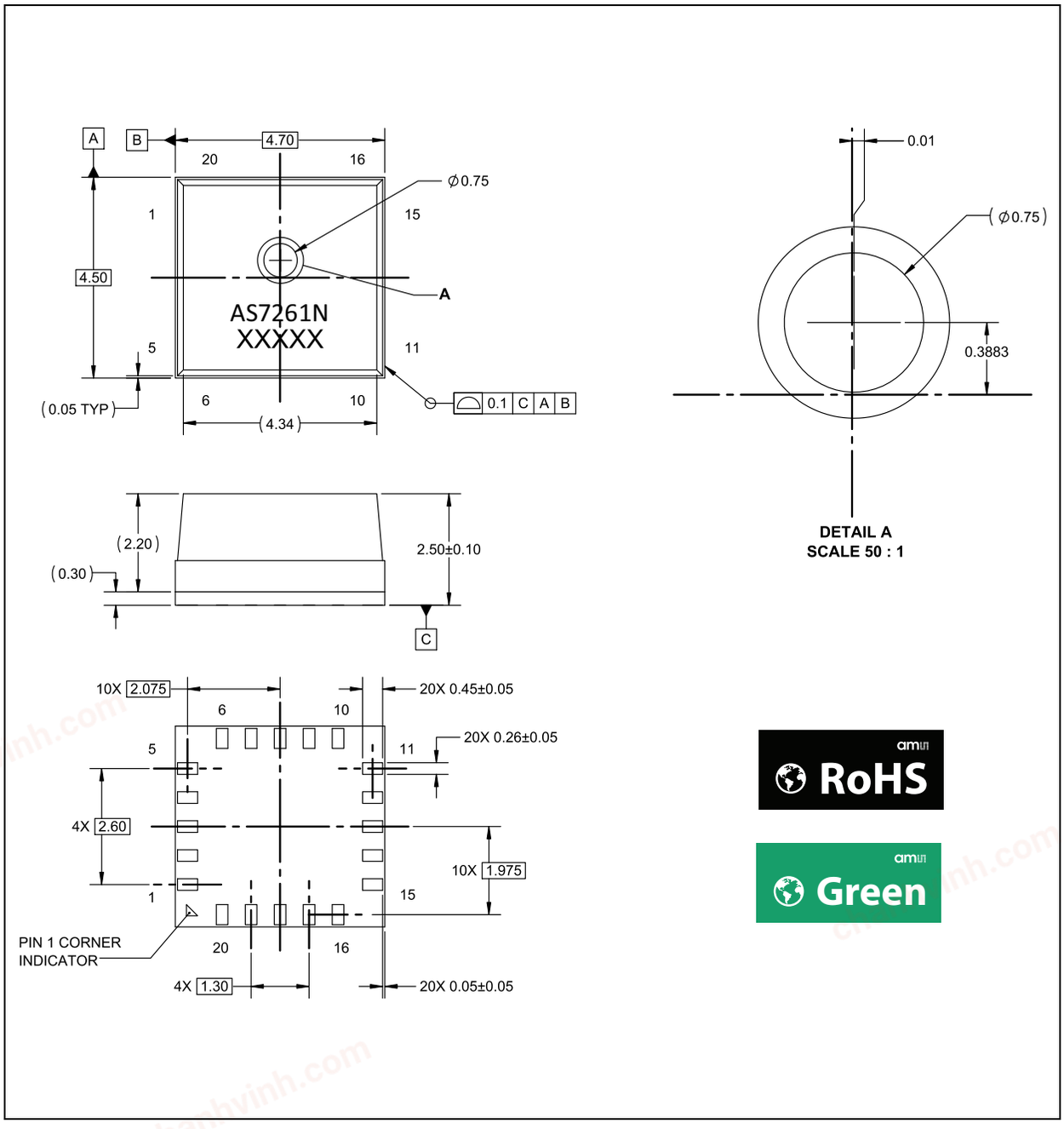


In order to prevent interference, avoid trace routing feedthroughs with exposure directly under the AS7261N. An example routing is illustrated in the diagram.

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Package Drawings & Markings

Figure 38:
Package Drawing



Note(s):

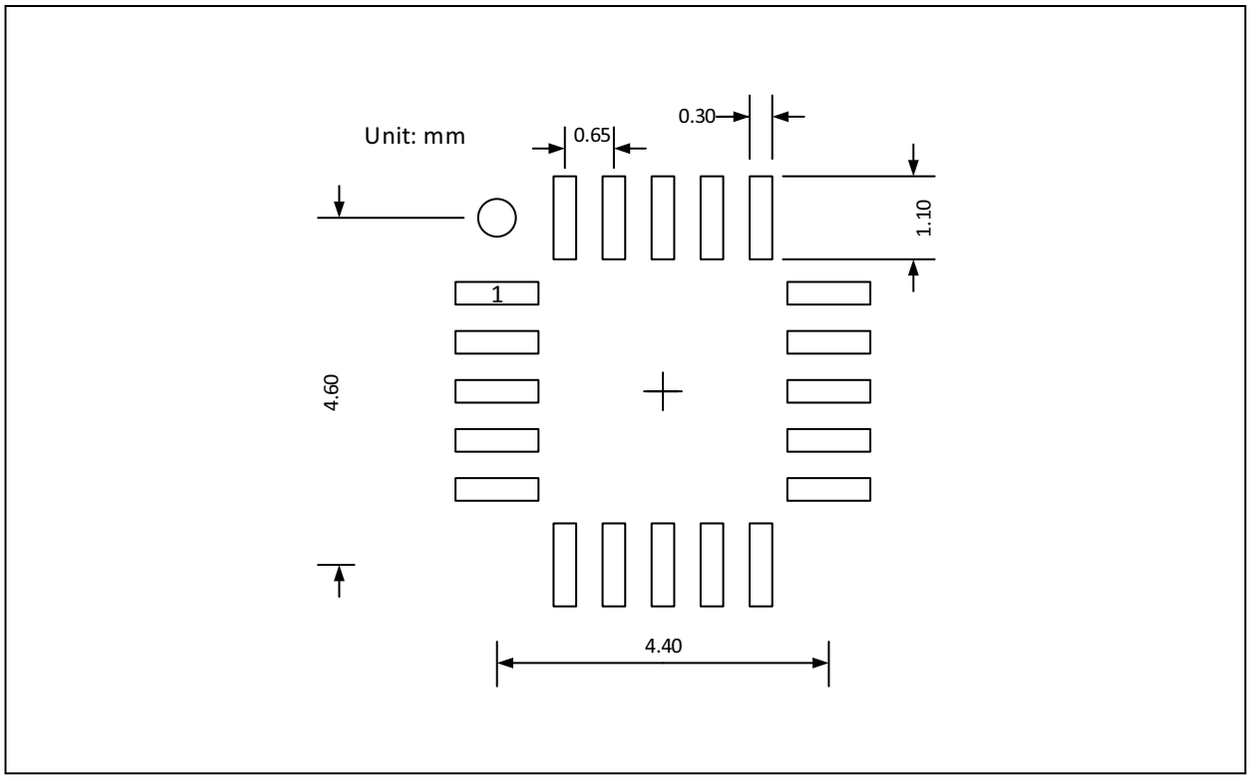
1. All linear dimensions are in millimeters
2. XXXXX = tracecode

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PCB Pad Layout

Suggested PCB pad layout guidelines for the LGA device are shown.

Figure 39:
Recommended PCB Pad Layout



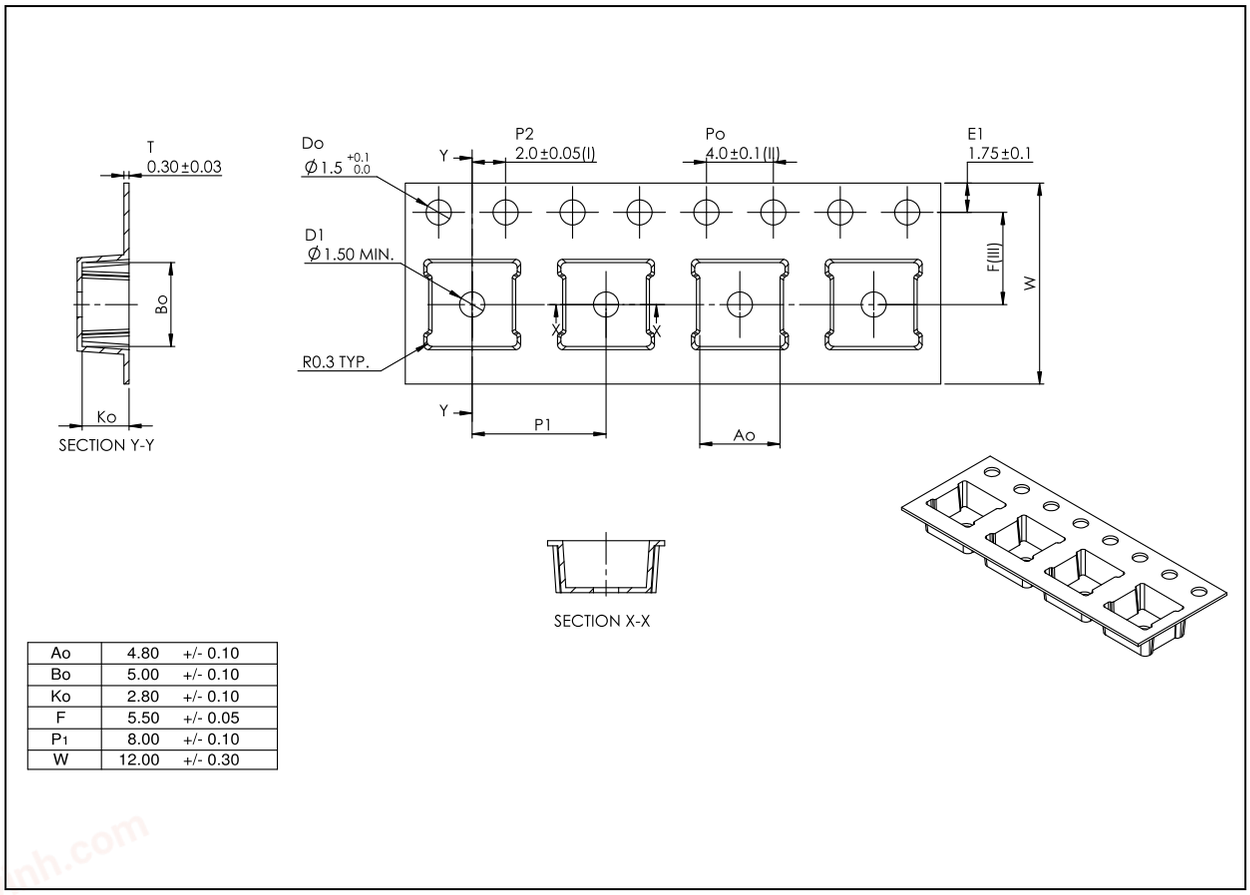
Note(s):

1. Unless otherwise specified, all dimensions are in millimeters.
2. Dimensional tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

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Mechanical Data

Figure 40:
Tape & Reel Information



Ao	4.80	+/- 0.10
Bo	5.00	+/- 0.10
Ko	2.80	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Note(s):

1. All dimensions in millimeters unless of otherwise stated.
2. Measured from centreline of sprocket hole to centreline of pocket.
3. Cumulative tolerance of 10 sprocket holes is ±0.20.
4. Measured from centreline of sprocket hole to centreline of pocket.
5. Other material available.

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Soldering & Storage Information

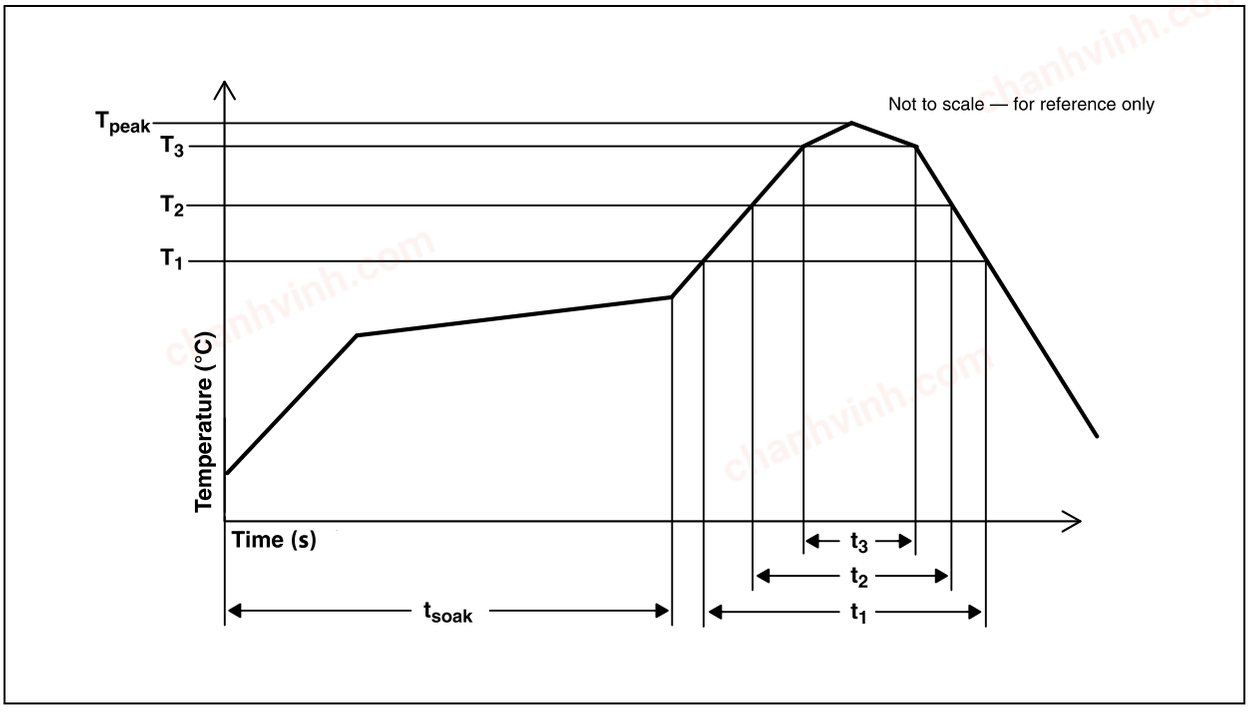
Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 41:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{SOAK}	2 to 3 minutes
Time above 217°C(T_1)	t_1	Max 60s
Time above 230°C(T_2)	t_2	Max 50s
Time above T_{peak} - 10°C(T_3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max -5°C/s

Figure 42:
Solder Reflow Profile Graph



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Manufacturing Process Considerations

The AS7261N package is compatible with standard reflow no-clean and cleaning processes including aqueous, solvent or ultrasonic techniques. However, as an open-aperture device, precautions must be taken to avoid particulate or solvent contamination as a result of any manufacturing processes, including pick and place, reflow, cleaning, integration assembly and/or testing. Temporary covering of the aperture is allowed. To avoid degradation of accuracy or performance in the end product, care should be taken that any temporary covering and associated sealants/debris are thoroughly removed prior to any optical testing or final packaging.

Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

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Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

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Ordering & Contact Information

Figure 43:
Ordering Information

Ordering Code	Package	Marking	Description	Delivery Form	Delivery Quantity
AS7261N-BLGT	20-pin LGA	AS7261N	XYZ and NIR Sensor with Electronic Shutter	Tape & Reel	2000 pcs/reel

Buy our products or get free samples online at:
www.ams.com/ICdirect

Technical Support is available at:
www.ams.com/Technical-Support

Provide feedback about this document at:
www.ams.com/Document-Feedback

For further information and requests, e-mail us at:
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For sales offices, distributors and representatives, please visit:
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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
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Revision Information

Changes from 1-01 (2017-Feb-08) to current revision 1-02 (2017-Feb-27)	Page
Updated Figure 10	9

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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