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AS5048A/AS5048B

Magnetic Rotary Encoder (14-Bit Angular Position Sensor)

General Description

The AS5048 is an easy to use 360° angle position sensor with a 14-bit high resolution output.

The IC measures the absolute position of the magnet's rotation angle and consists of Hall sensors, analog digital converter and digital signal processing. The absolute position information of the magnet is directly accessible over a PWM output and can be read out over a standard SPI or a high speed I^2C interface. AS5048A has a SPI interface, AS5048B I^2C interface. Both devices offer a PWM output.

The zero position can be programmed via SPI or I^2C command. This simplifies the assembly of the complete system because the zero position of the magnet does not need to be mechanically aligned. The sensor tolerates misalignment, air gap variations, temperature variations and as well external magnetic fields. This robustness and wide temperature range (-40°C up to 150°C) of the AS5048 makes the IC ideal for rotation angle sensing in harsh industrial and medical environments. Several AS5048 ICs can be connected in daisy chain for serial data read out. An internal voltage regulator allows the AS5048 to operate at either 3.3V or 5V supplies.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5048A/AS5048B, Magnetic Rotary Encoder (14-Bit Angular Position Sensor) are listed below:

Figure 1:
Added Value of Using AS5048

Benefits	Features
• No external programmer needed	• Standard SPI or I^2C interface and PWM
• High precision	• 14-bit resolution (0.0219°/LSB)
• Easy to use	• Zero position programmable via SPI or I^2C
• Low material costs (no shielding)	• Immune to external magnetic stray fields

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- Contactless rotary position sensor over 360°
- Temperature range: -40°C to 150°C
- 3.3V / 5V compliant
- Package: 14-pin TSSOP (5 x 6.4mm)

Applications

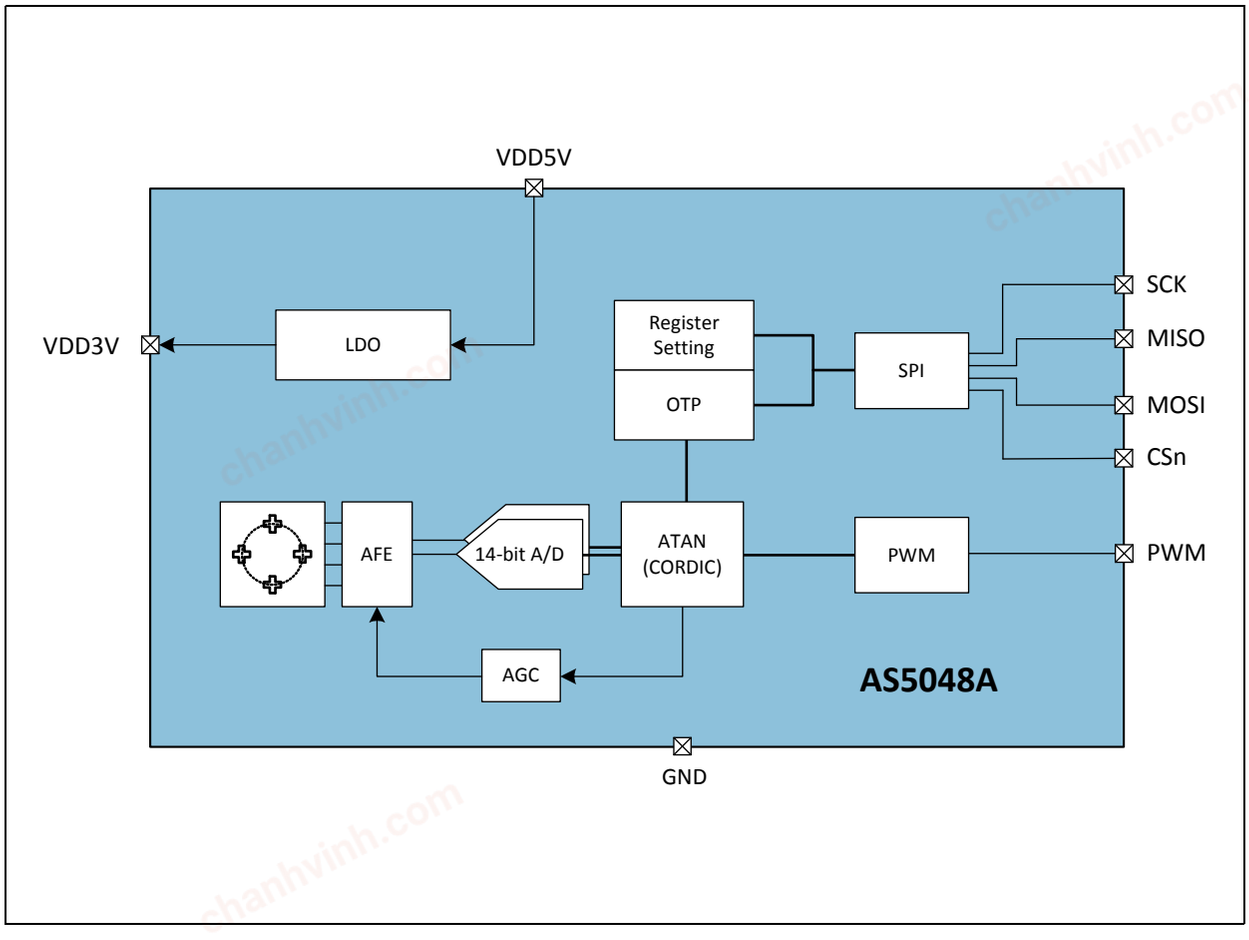
The applications of AS5048 include:

- Robotic joint position detection
- Industrial motor position control
- Medical robots and fitness equipment

Block Diagram

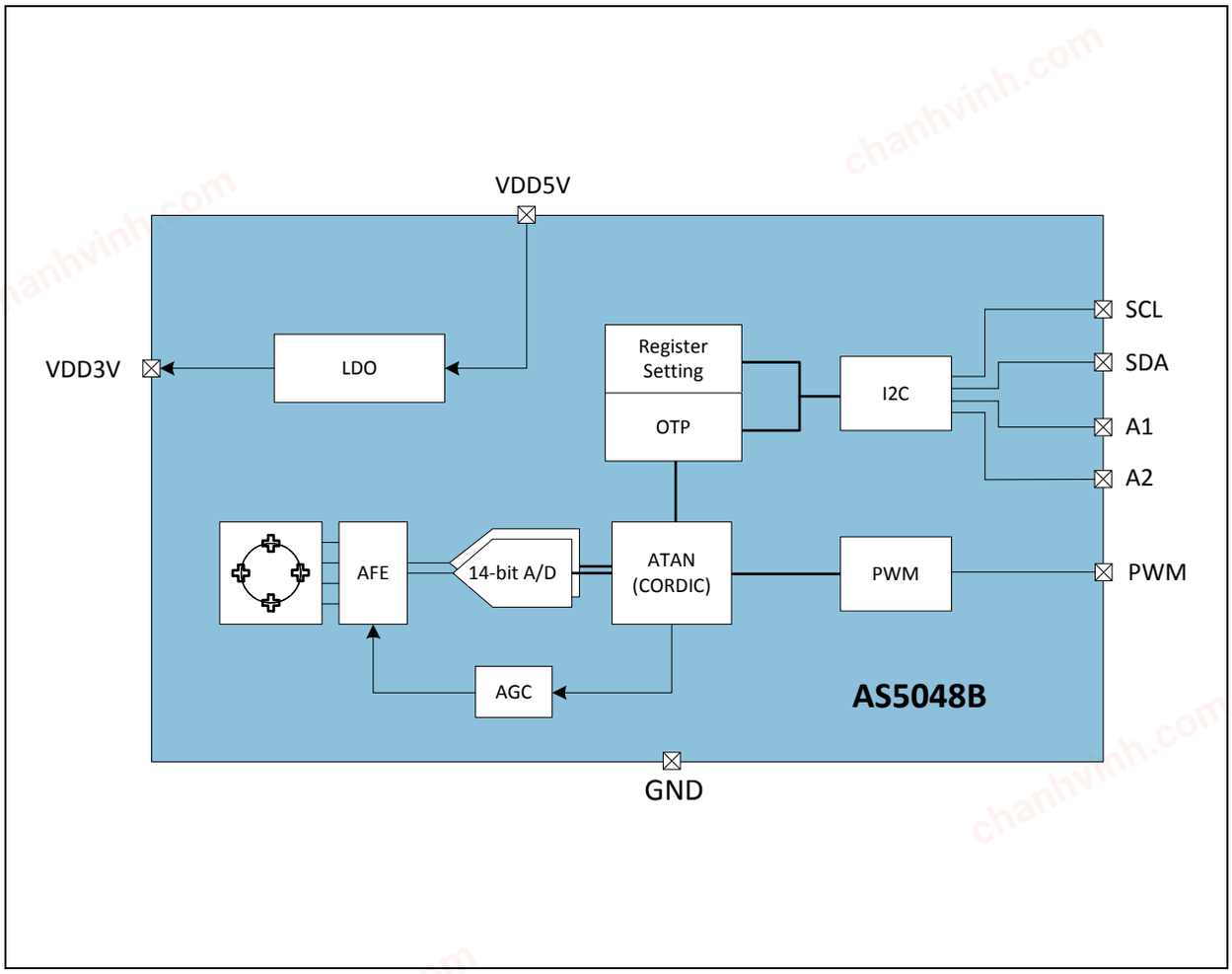
The functional blocks of this device are shown below:

Figure 2:
AS5048A Block Diagram



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Figure 3:
AS5048B Block Diagram



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Pin Assignments

The AS5048A/AS5048B pin assignments are described below.

Figure 4:
TSSOP14 Pin Configurations

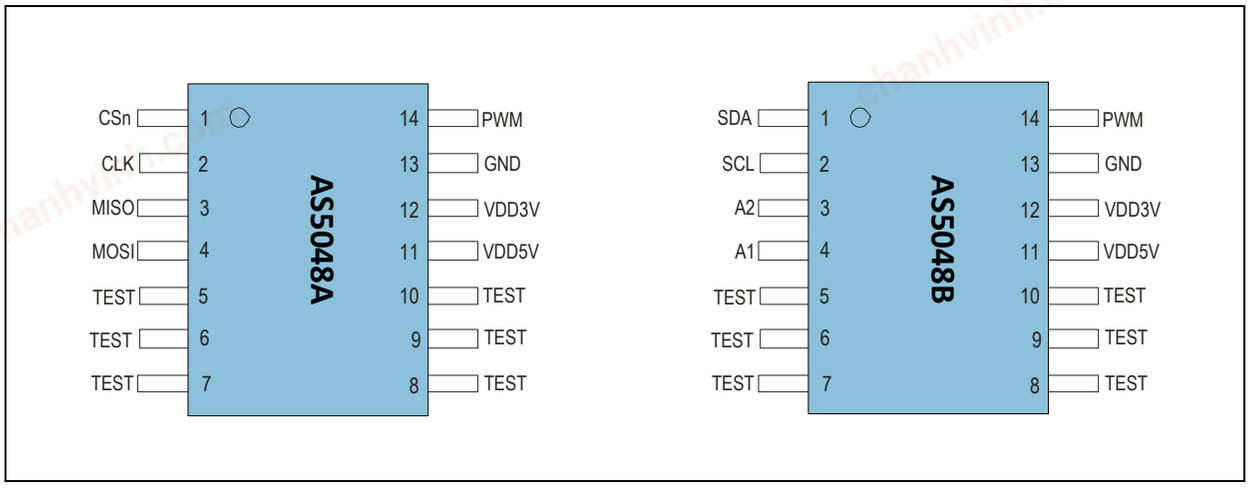


Figure 5:
TSSOP14 Pin Descriptions for AS5048A

Pin	AS5048A	Pin Type	Description
1	CSn	Digital input with Schmitt trigger	SPI chip select - active low
2	CLK		SPI clock input
3	MISO	Digital I/O with Schmitt trigger in the input path	SPI master in/slave out
4	MOSI	Digital input with Schmitt trigger	SPI master out/slave in
5	TEST	Analog I/O	Test pin should be connected to GND.
6	TEST	Analog I/O	Test pins should be left open during normal operation.
7	TEST		
8	TEST		
9	TEST		
10	TEST		
11	VDD5V	Supply pad	Positive Supply Voltage, 3.0 to 5.5 V
12	VDD3V		3.3V Regulator output; internally regulated from VDD. Connect to VDD for 3V supply voltage. 10µF capacitor to GND required in 5V operation mode
13	GND		Negative Supply Voltage (GND)
14	PWM	Digital output – push-pull	Pulse Width Modulation output

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Figure 6:
TSSOP14 Pin Description for AS5048B

Pin	AS5048B	Type	Description
1	SDA	Digital I/O with open drain output	Data pin I^2C interface
2	SCL	Digital input with Schmitt trigger	I^2C clock input
3	A2		I^2C address selection pin 3
4	A1		I^2C address selection pin 4
5	TEST	Analog I/O	Test pin should be connected to GND.
6	TEST	Analog I/O	Test pins should be left open during normal operation.
7	TEST		
8	TEST		
9	TEST		
10	TEST		
11	VDD5V	Supply pad	Positive Supply Voltage, 3.0 to 5.5 V
12	VDD3V		3.3V Regulator output; internally regulated from VDD. Connect to VDD for 3V supply voltage. 10µF capacitor to GND required in 5V operation mode
13	GND		Negative Supply Voltage (GND)
14	PWM	Digital output – push-pull	Pulse Width Modulation output

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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
Electrical Parameters					
VDD5V	DC supply voltage at VDD pin	-0.3	7	V	
VDD3V	DC voltage at VDD3V pin	-0.3	5	V	
GND	DC voltage at GND pin	-0.3	0.3	V	
V_{IN}	Input pin voltage		VDD+0.3	V	
I_{SCR}	Input current (latchup immunity)	-100	100	mA	Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	± 2		kV	MIL 883 E method 3015
Power Dissipation					
P_T	Total power dissipation (all supplies and outputs)		150	mW	
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature	-55	150	°C	
T_{BODY}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 “Moisture Solid State Surface Mount Devices”. The lead finish from Pb-free leaded packages is matte tin (100%Sn)
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor life time of 168h

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Electrical Characteristics

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Operating Conditions

Figure 8:
Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
VDD5V	Positive supply voltage	4.5	5.5	V	5V Operation via LDO
VDD3V		3	3.6	V	LDO output voltage
VDDCORE	Positive core supply voltage	3	3.6	V	
T_{AMB}	Ambient temperature	-40	150	°C	Only for 5V operation. T_amb_max for 3V is 125°C
I_{SUP}	Supply current		15	mA	

DC/AC Characteristics for Digital Inputs and Outputs

Figure 9:
DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit
CMOS Digital Input with Schmitt Trigger: CSn, CLK, MOSI and SCL, A1, A2				
V_{IH}	High level input voltage	0.7 * VDDCORE		V
V_{IL}	Low level input voltage		0.3 * VDDCORE	V
I_{LEAK}	Input leakage current		1	µA
CMOS Output: PWM, MISO, SDA				
V_{OH}	High level output voltage	VDDCORE - 0.5		V
V_{OL}	Low level output voltage		GND+0.4	V
C_L	Capacitive load		50	pF
I_{OUT}	Output current		4	mA

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Electrical System Specifications

VDD5V = 5V, T_{AMB} = -40 to 150°C unless noted otherwise.

Figure 10:
System Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bz	Magnetic input field		30	50	70	mT
f_{sample}	Output sampling rate		10.2	11.25	12.4	kHz
RES	Output resolution			14		Bit
Noise	Sensor output noise	2.73LSB@14bit, rms value			0.06	deg
t_{prop}	System propagation delay		90.7	100	110.2	µs
f_{PWM}	PWM frequency		0.907	1	1.102	kHz
INL_{OPT} @25°C	Non-linearity, optimum placement of the magnet				± 0.8	deg
INL OPT+TEMP	Non-linearity optimum placement of the magnet over the full temperature range				±1	deg
INL DIS+TEMP	Non-linearity @ displacement of magnet and temperature -40°C to 150°C	Assuming N35H magnet (D=8mm, H=3mm) 500µm displacement in x and y z-distance @ 2000µm			±1.2	deg
$t_{startup}$	Startup time				10	ms

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Functional Description

The AS5048 is a magnetic Hall sensor system manufactured in a CMOS process. A lateral Hall sensor array is used to measure the magnetic field components perpendicular to the surface of the chip. The AS5048 is uses self-calibration methods to eliminate signal offset and sensitivity drifts.

The integrated Hall sensors are placed around the center of the device and deliver a voltage representation of the magnetic flux Bz.

Through Sigma-Delta Analog-to-Digital Converter (ADC) and Digital Signal-Processing (DSP) algorithms, the AS5048 provides accurate high-resolution absolute angular position information. This is executed by a Coordinate Rotation Digital Computer (CORDIC) which calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs that indicate movements of the magnet towards or away from the device's surface, in the z-axis.

A small diametrically magnetized (two-pole) standard magnet provides the angular position information. Depending on the system requirements different magnet diameters are possible. Additional flexibility is given by the wide range of the magnetic input range. The AS5048 can be combined with NeFeB, SmCo and alternative magnet materials e.g. hard ferrites. The AS5048 provides a 14-bit binary code representing the angular position of the magnet. The type of output is pre-programmed as SPI version A or I^2C version B. Simultaneously a PWM output signal is available in 12 bit format.

A simple programming of the zero position is possible over the interface. No additional programmer is needed. The AS5048 uses one time programmable (OTP) fuses for permanent programming of the user settings. The verification is possible over a simple digital readout of the OTP content.

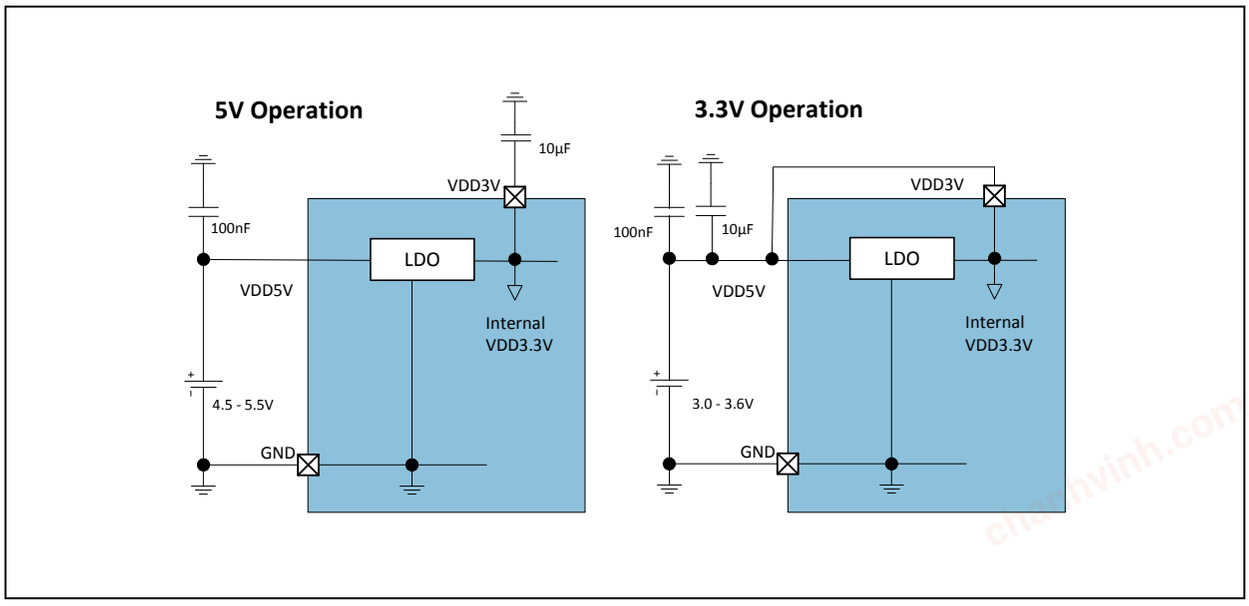
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Operation

Supply Voltage Configuration

The AS5048 operates at 5V ±10%, using an internal Low-Dropout (LDO) voltage regulator. In addition a 3.3V operation is possible. The **VDD3V** output is intended for internal use only. **It must not be loaded with an external load.**

Figure 11:
Connections for 5V and 3.3V Supply Voltages



Note(s):

1. The pin **VDD3V** must always be buffered by a 10 µF capacitor in 5V operation. It must not be left floating, as this may cause unstable internal supply voltages which may lead to larger output jitter of the measured angle.
   In 3V operation the **VDD3V** must be shorted to **VDD5V.** The ambient temperature T_{AMB} is limited to 125°C in this mode.

SPI Interface

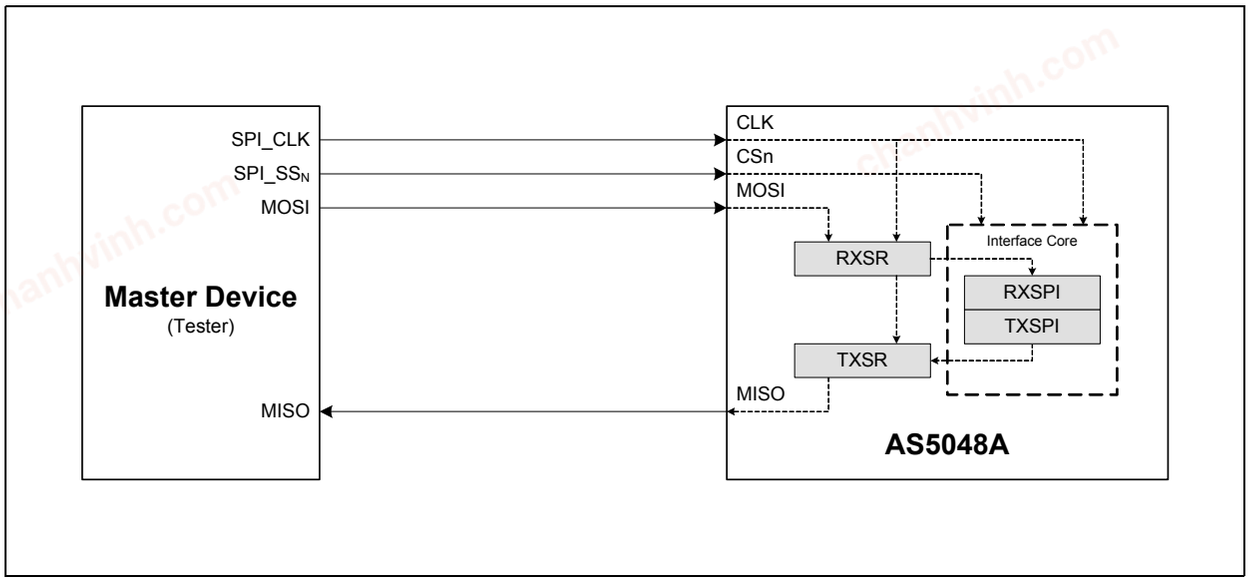
The 16 bit SPI Interface enables read / write access to the register blocks and is compatible to a standard micro controller interface. The SPI is active as soon as **CSn** is pulled low. The AS5048A then reads the digital value on the **MOSI** (master out slave in) input with every falling edge of **CLK** and writes on its **MISO** (master in slave out) output with the rising edge. After 16 clock cycles **CSn** has to be set back to a high status in order to reset some parts of the interface core.

SPI Interface Signals (4-Wire Mode, Wire_mode = 1)

The AS5048A only supports slave operation mode. Therefore **CLK** for the communication as well as the **CSn** signal has to be provided by the test equipment. The following picture shows a basic interconnection diagram with one master and an AS5048A device and a principle schematic of the interface core.

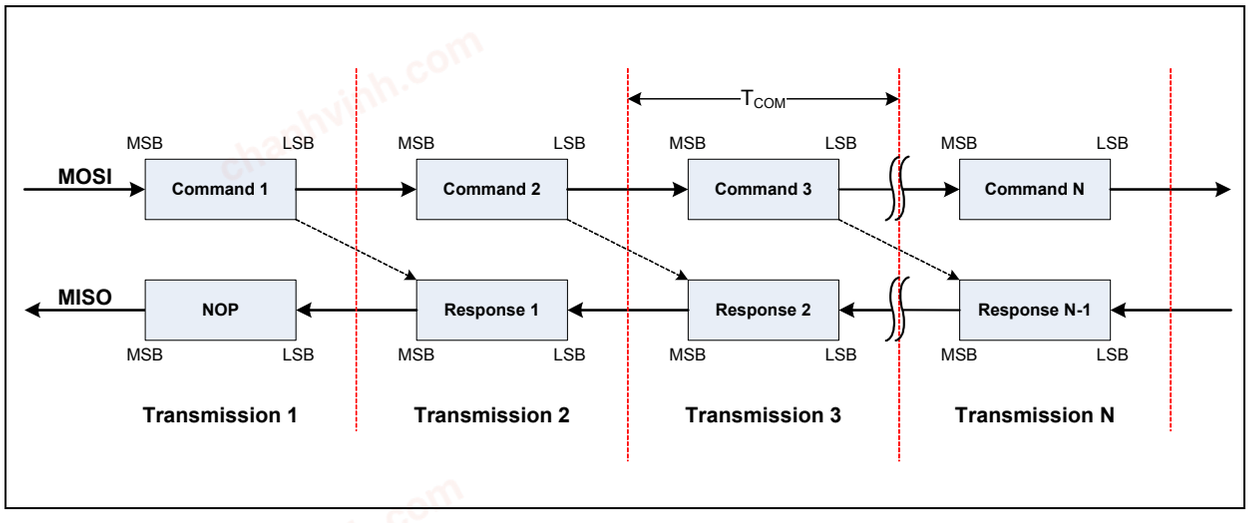
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Figure 12:
SPI Connection AS5048A with µC



Because the interface has to decode the sent command before it can react and provide data the response of the chip to a specific command applied at a time T can be accessed in the next transmission cycle ending at T + TCOM. The data are sent and read with **MSB first**. Every time the chip is accessed it is sending and receiving data.

Figure 13:
SPI Command/Response Data Flow



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SPI Timing

Figure 14:
SPI Timing Diagram

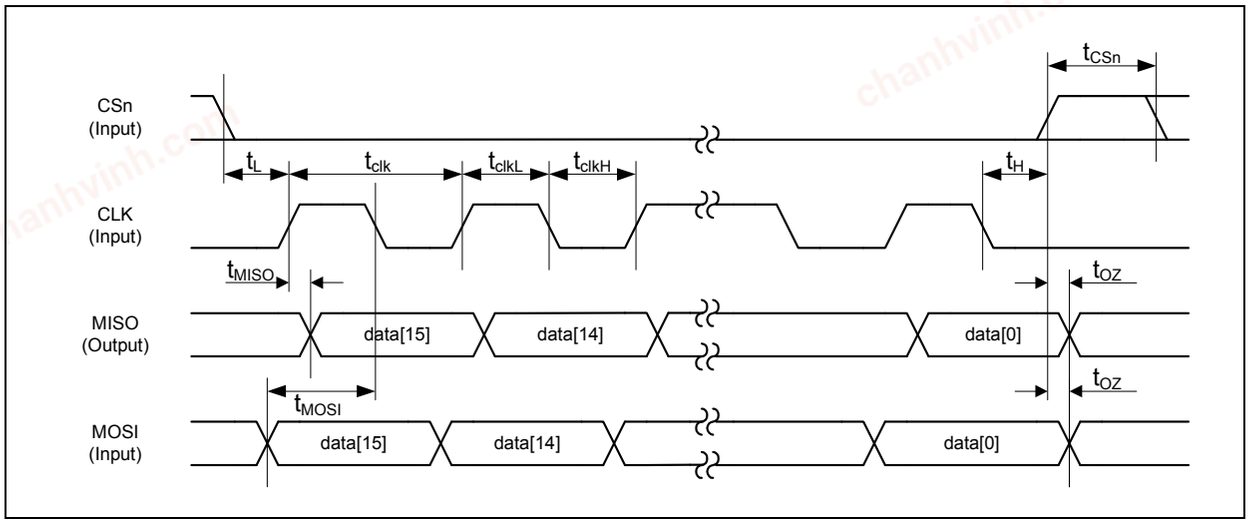


Figure 15:
SPI Timing Characteristics

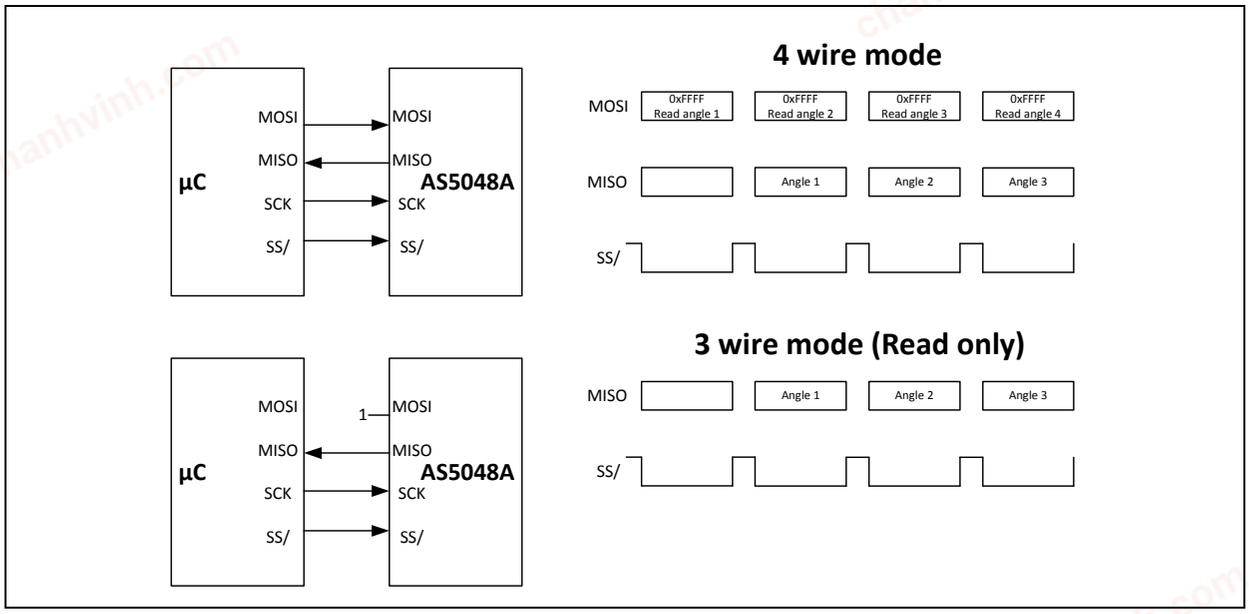
Parameter	Description	Min	Max	Unit
t_L	Time between CSn falling edge and CLK rising edge	350		ns
T_{CLK}	Serial clock period	100		ns
t_{CLKL}	Low period of serial clock	50		ns
t_{CLKH}	High period of serial clock	50		ns
t_H	Time between last falling edge of CLK and rising edge of CSn	50		ns
T_{CSnH}	High time of CSn between two transmissions	350		ns
t_{MOSI}	Data input valid to clock edge	20		ns
t_{MISO}	CLK edge to data output valid		20	ns

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SPI Connection to the Host µC

Single Slave Mode

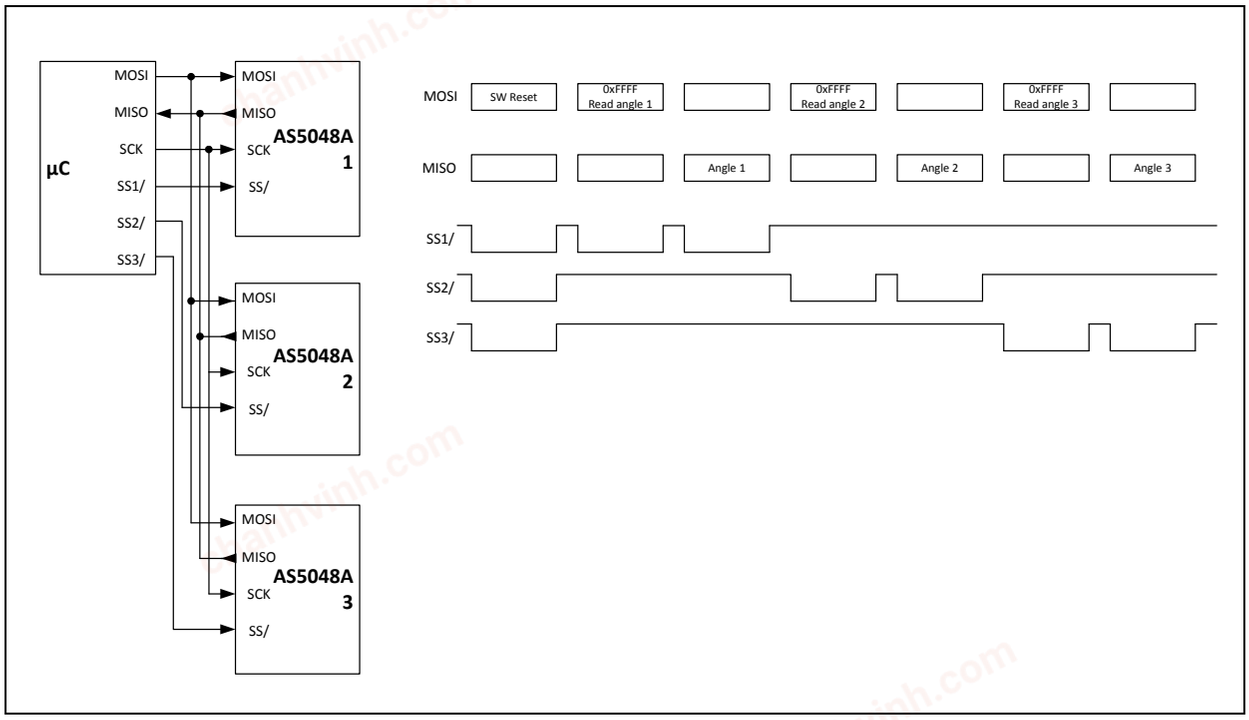
Figure 16:
Single Slave Mode



Single Slave Mode: This figure shows the SPI connection to the host µC using Single Slave Mode.

3 Wire Mode (read only)

Figure 17:
Multiple Slave, n+3 Wire (Separate ChipSelect)

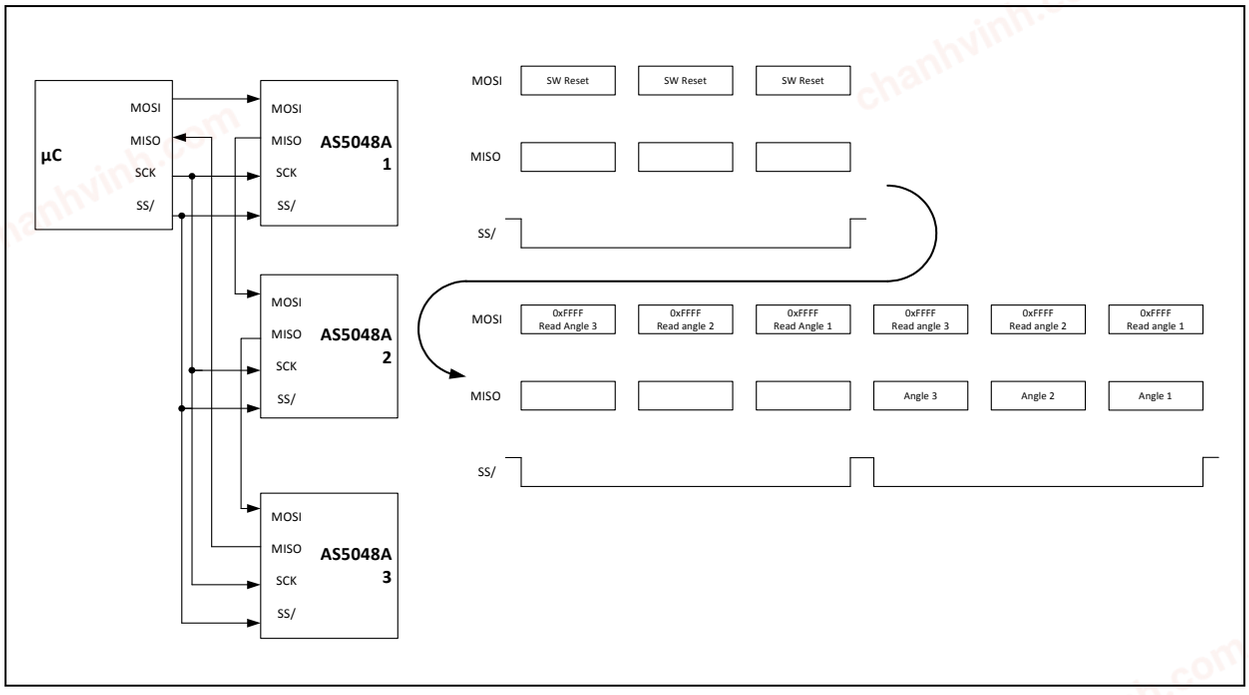


Multiple Slave, n+3 Wire (Separate ChipSelect): This figure shows the SPI connection to the host µC using 3 Wire mode.

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Daisy Chain, 4 Wire

Figure 18:
Daisy Chain, 4 Wire



Daisy Chain, 4 Wire: This figure shows the SPI connection to the host µC using Daisy Chain, 4 wire mode.

SPI Communication Command Package

Every command sent to the AS5048A is represented with the following layout.

Figure 19:
SPI Command Package

Command Package															
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	RWn	Address<13:0>													

Bit Definition & Description	
PAR	Parity bit (EVEN)
RWn	Indicates read(1) or write(0) command
Address	14 bit address code

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Read Package (Value Read from AS5048A)

The read frame always contains two alarm bits, the parity and error flags and the addressed data of the previous read command.

Figure 20:
SPI Read Package

Read Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	EF	Data<13:0>													
Bit Definition & Description																
PAR			Parity bit (EVEN)													
EF			Error flag indicating a transmission error in a previous host transmission													
Data			14 bit addressed data													

Write Data Package (Value Written to AS5048A)

The write frame is compatible to the read frame and contains two additional bits, parity flag and R flag.

If the previous command was a write command a second package has to be transmitted.

Figure 21:
SPI Write Data Package

Data Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	R	Data <13:0>													
Bit Definition & Description																
PAR			Parity bit (EVEN)													
R			Has to be 0													
Data			14 bit data to write to former selected address													

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Register Description

Figure 22:
SPI Register Map

Address hex	Name	Access Type	Bit	Symbol	Default	Description
Control and Error Registers						
x0000	NOP	R	13 : 0	NOP	0	No operation dummy information
x0001	Clear Error Flag	R	13 : 3	Not used	n.a.	Error register. All errors are cleared by access
			2	Parity Error	0	
			1	Command Invalid		
			0	Framing Error		
x0003	Programming Control	R/W	13 : 7	Not used	0	Programming control register. Programming must be enabled before burning the fuse(s). After programming is a verification mandatory. See programming procedure.
			6	Verify		
			5 4	Not used		
			3	Burn		
			2 1	Reserved		
			0	Programming Enable		

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Address hex	Name	Access Type	Bit	Symbol	Default	Description
Programmable Customer Settings						
x0016	OTP Register Zero Position Hi	R/W + Program	13	Not used	0	Zero Position value high byte
			:			
			8			
			7	Zero Position <13>	0	
			:	:	:	
			0	Zero Position <6>	0	
x0017	OTP Register Zero Position Low 6 LSBs	R/W + Program	13	Not used	0	Zero Position remaining 6 lower LSB's
			:			
			6			
			5	Zero Position <5>	0	
			:	:	:	
			0	Zero Position <0>	0	
Readout Registers						
x3FFD	Diagnostics + Automatic Gain Control (AGC)	R	13	Not used	n.a.	Diagnostics flags
			12			
			11	Comp High	0	
			10	Comp Low	0	
			9	COF	0	
			8	OCF	1	
			7	AGC value<7>	1	Automatic Gain Control value. 0 decimal represents high magnetic field, 255 decimal represents low magnetic field
			:	:	:	
			0	AGC value<0>	0	
x3FFE	Magnitude	R	13	Magnitude<13>	0	Magnitude output value of the CORDIC
			:	:	:	
			0	Magnitude<0>	0	
x3FFF	Angle	R	13	Angle <13>	0	Angle output value including zero position correction
			:	:	:	
			0	Angle<0>	0	

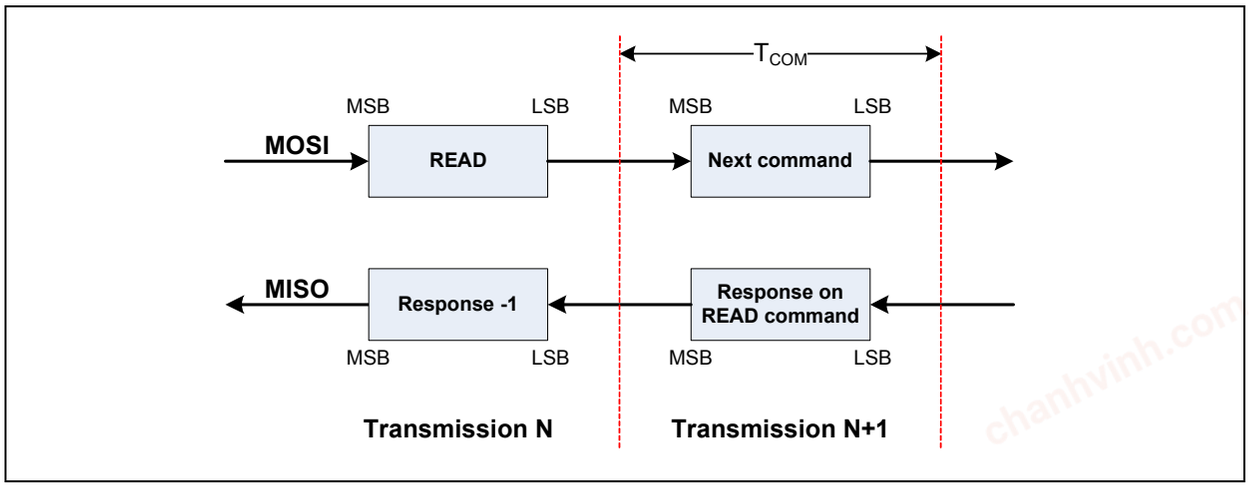
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SPI Interface Commands

READ Command

For a single *READ* command two transmission sequences are necessary. The first package written to the AS5048 contains the *READ* command **(MSB-1 high)** and the address the chip has to access, the second package transmitted to the AS5048 device can be *any command* the chip has to process next. The content of the desired register is available in the *MISO* register of the *master device* at the end of the second transmission cycle.

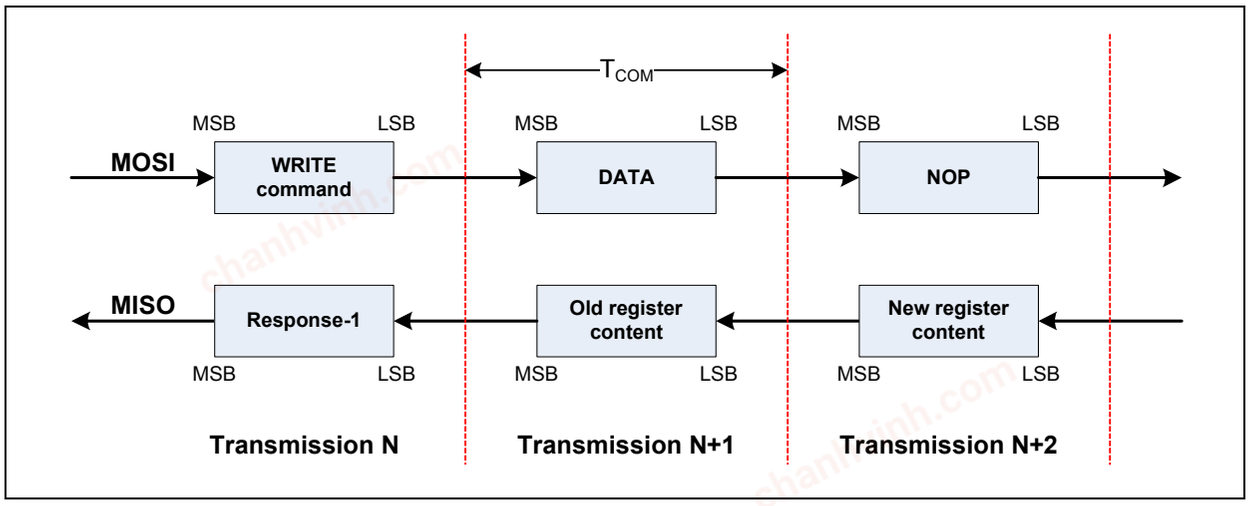
Figure 23:
READ Command



WRITE Command

A single *WRITE* command takes two transmission cycles. With a NOP command after the WRITE command you can verify the sent data with three transmission cycles because the data will be send back during the following command.

Figure 24:
WRITE Command

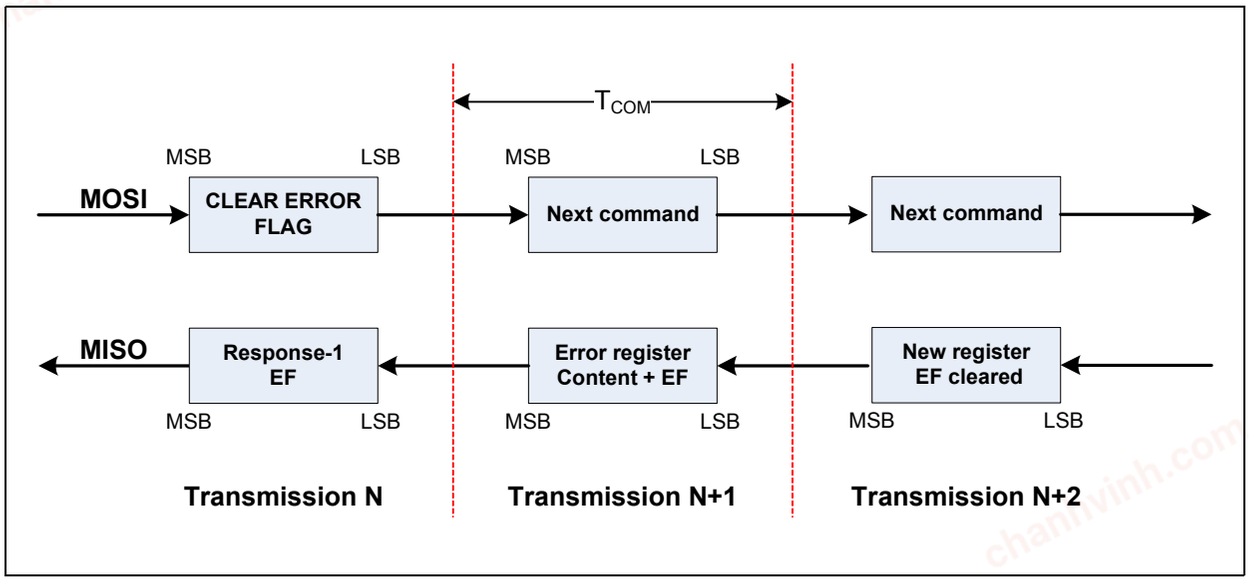


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CLEAR ERROR FLAG Command

The *CLEAR ERROR FLAG* command is implemented as *READ* command. This command clears the *ERROR FLAG* which is contained in every *READ* frame. Before the *ERROR FLAG* is cleared the error register content comes back with the information which error type was occurred. On the next new *READ* register the *ERROR FLAG* is cleared.

Figure 25:
CLEAR ERROR FLAG Command



The package necessary to perform a *CLEAR ERROR FLAG* is built up as follows.

Figure 26:
Clear Error Flag Command

CLEAR ERROR FLAG Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Possible conditions which force the ERROR FLAG to be set:

- Wrong parity
- Wrong number of clocks (no full transmission cycle or too many clocks)
- Invalid command
- Frame error

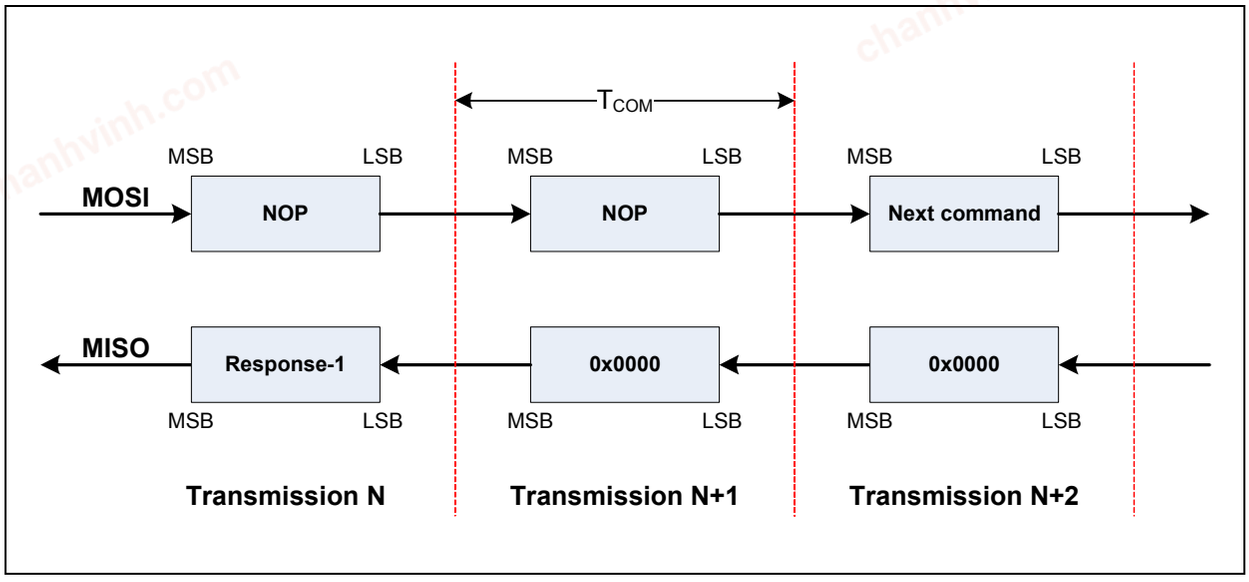
Note(s): If the error flag is set to high because of a communication problem the flag remains set until it will be cleared by the *CLERAR ERROR FLAG* command.

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NOP Command

The *NOP* command represents a dummy write to the AS5048.

Figure 27:
NOP Command



The NOP command frame looks like follows.

Figure 28:
NOP Command

NOP Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The chip's response on this command is 0x0000

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I²C Interface

The AS5048B supports 2-wire high-speed I²C protocol in device mode. The host MCU (master) has to initiate the data transfers. The 7-bit device address of the slave depends on the state of the OTP I²C register 21 (0x15) bit 0… 4 + 2 I²C address selection pin 3 and 4.

Supported modes:

- Random/Sequential Read
- Byte/Page Write
- Standard : 0 to 100kHz clock frequency (slave mode)
- Fast Mode : 0 to 400kHz clock frequency (slave mode)
- High Speed: 0 to 3.4MHz clock frequency (slave mode)

The SDA signal is bidirectional and is used to read and write the serial data. The SCL signal is the clock generated by the host MCU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 3.4MHz, data are triggered on the rising edge of SCL.

I²C Electrical Specification

Figure 29:
I²C Electrical Specification

Symbol	Parameter	Condition	FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF		Unit
			Min	Max	Min	Max	Min	Max	
V_{IL}	LOW-Level Input Voltage		-0.5	$0.3V_{DDCORE}$	-0.5	$0.3V_{DDCORE}$	-0.5	$0.3V_{DDCORE}$	V
V_{IH}	HIGH-Level Input Voltage		$0.7V_{DDCORE}$	V_{DDCORE} + 0.5	$0.7V_{DDCORE}$	V_{DDCORE} + 0.5	$0.7V_{DDCORE}$	V_{DDCORE} + 0.5	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs	V_{DDCORE}< 2V	$0.1V_{DDCORE}$	--	$0.1V_{DDCORE}$	--	$0.1V_{DDCORE}$	--	V
V_{OL}	LOW-Level Output Voltage (open-drain or open-collector) at 3mA Sink Current	V_{DDCORE}< 2V	--	$0.2V_{DDCORE}$	--	$0.2V_{DDCORE}$	--	$0.2V_{DDCORE}$	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4V	20		--	--	--	--	mA
I_{CS}	Pull-up current of SCLH current source		--	--	3	12	3	12	mA
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		--	50 (1)	--	10	--	10	ns

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Symbol	Parameter	Condition	FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF		Unit
			Min	Max	Min	Max	Min	Max	
I_i	Input Current at each I/O Pin	Input Voltage between	-10	+10 (2)	--	10	--	10	µA
C_B	Total Capacitive Load for each Bus Line		--	550	--	100	--	400	pF
$C_{I/O}$	I/O Capacitance (SDA,SCL)		--	10	--	10	--	10	pF

Note(s):

1. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
2. I/O pins of Fast-mode and Fast-mode Plus devices must not obstruct the SDA and SCL lines if VDD is switched OFF.

I²C Timing

Figure 30:
I²C Timing

Symbol	Parameter	Condition	FS-mode		HS-mode C_B=100pF		HS-mode C_B=400pF (5)		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCLK}	SCL clock Frequency		--	400	--	3400	--	1700	kHz
t_{BUF}	Bus Free Time; time between STOP and START Condition		500	--	500	--	500	--	ns
$t_{HD;STA}$	Hold Time; (Repeated) START Condition (1)		260	--	160	--	160	--	ns
t_{LOW}	LOW Period of SCL Clock		500	--	160	--	320	--	ns
t_{HIGH}	HIGH Period of SCL Clock		260	--	60	--	120	--	ns
$t_{SU;STA}$	Setup Time for a Repeated START condition		260	--	160	--	160	--	ns
$t_{HD;DAT}$	Data Hold Time (2)		0	450	0	70	0	150	ns
$t_{SU;DAT}$	Data Setup Time (3)		50	--	10	--	10	--	ns
t_R	Rise Time of SDA and SCL Signals		20+0.1C_b	120	--	--	--	--	ns

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Symbol	Parameter	Condition	FS-mode		HS-mode C_B=100pF		HS-mode C_B=400pF (5)		Unit
			Min	Max	Min	Max	Min	Max	
t_F	Fall time of SDA and SCL signals		20+0.1C_b	120 (4)	--	--	--	--	ns
t_{rCL}	Rise time of SCLH signal	Ext. pull-up source of 3mA	--	--	10	40	20	80	ns
t_{rCL1}	Rise time of SCLH signal after repeated START condition and after an acknowledge bit	Ext. pull-up source of 3mA	--	--	10	80	20	160	ns
t_{fCL}	Output rise time of SCLH signal	Ext. pull-up source of 3mA	--	--	10	40	20	80	ns
t_{rDA}	Output rise time of SDAH signal		--	--	10	80	20	160	ns
t_{fDA}	Output rise time of SDAH signal		--	--	10	80	20	160	ns
$t_{SU;STO}$	Setup Time for STOP Condition		260	--	160	--	160	--	ns
V_{nL}	Noise margin at LOW level		0.1V_{DDp}	--	0.1V_{DDp}	--	0.1V_{DDp}	--	V
V_{nH}	Noise margin at HIGH level		0.2V_{DDp}	--	0.2V_{DDp}	--	0.2V_{DDp}	--	V

Note(s):

1. After this time the first clock is generated.
2. A device must internally provide a minimum hold time (120ns / max 250ns for Fast-mode Plus, 80ns / max 150ns for High-speed mode) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
3. A fast-mode device can be used in standard-mode system, but the requirement $t_{SU;DAT}$ = 250ns must then e met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{Rmax} + $T_{SU;DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
4. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.
5. For capacitive bus loads between 100pF and 400pF, the timing parameters must be linearly interpolated

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Register Table

The following registers / functions are accessible over the serial I²C interface.

Figure 31:
Register Map I²C

Address hex	Name	Access Type	Bit	Symbol	Default	Description
Control OTP						
x03	Programming Control	R/W	7	Not used	0	Programming control register. Programming must be enabled before burning the fuse(s). After programming is an verification mandatory. See programming procedure.
			6	Verify		
			5	Not used		
			4			
			3	Burn		
			2	Reserved		
			1			
			0	Programming Enable		
Programmable Customer Settings						
x15	I²C slave address	R/W	7	Not used	n.a.	I²C slave address slave address consist of 5 bits (MSBs) and the hardware setting of Pins A1 and A2 I²C address <4> is the inversion defined as '1'
			:			
			5			
			4	I²C address<4>	internally inverted	
			:	:	:	
			0	I²C address<0>	0	
x16	OTP Register Zero Position Hi	R/W + Program	7	Zero Position <13>	0	Zero Position value high byte
			:	:	:	
			0	Zero Position <6>	0	
x17	OTP Register Zero Position Low 6 LSBs	R/W + Program	7	Not used	n.a.	Zero Position remaining 6 lower LSB's
			6			
			5	Zero Position <5>	0	
			:	:	:	
			0	Zero Position <0>	0	

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Address hex	Name	Access Type	Bit	Symbol	Default	Description
Readout Registers						
xFA	Automatic Gain Control	R	7	AGC value<7>	1	Automatic Gain Control value. 0 decimal represents high magnetic field 255 decimal represents low magnetic field
			:	:	:	
			0	AGC value<0>	0	
xFB	Diagnostics	R	7	Not used	n.a.	Diagnostic flags
			:			
			4			
			3	Comp High	0	
			2	Comp Low	0	
			1	COF	0	
			0	OCF	1	
xFC	Magnitude	R	7	Magnitude<13>	0	Magnitude output value of the CORDIC
			:	:	:	
			0	Magnitude<6>	0	
xFD		R	7	Not used	n.a.	
			6			
			5	Magnitude<5>	0	
			:	:	:	
			0	Magnitude<0>	0	
xFE	Angle	R	7	Angle<13>	0	Angle output value including zero position correction
			:	:	:	
			0	Angle<6>	0	
xFF		R	7	Not used	n.a.	
			6			
			5	Angle<5>	0	
			:	:	:	
			0	Angle<0>	0	

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I²C Slave address

Figure 32:
Slave Address Construction



Note(s):

1. It's important to use a STOP condition only after a complete read or write sequence.

The slave address consists of the hardware setting on pins A1, A2. The MSB of the slave address (yellow) is internally inverted. This means that by default the resulting data is '1'. A read of the I²C slave address register 21 will return a '0' at the MSB.

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PWM Interface

The AS5048 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. The PWM frequency is internally trimmed to an accuracy of ±10% over full temperature range. This tolerance can be cancelled by measuring the complete duty cycle.

The PWM signal consists of different sections:

- Init:
  12 clocks → PWM = 'high'
- Error_n:
  4 clocks → PWM = 'not(system_error)'
- Data:
  4095 clocks → PWM = 'angle_zero' / 'low' (in case of error)
- Exit:
  8 clocks → PWM = 'low'

In case of an error the data section is set to zero.

Figure 33:
PWM Format

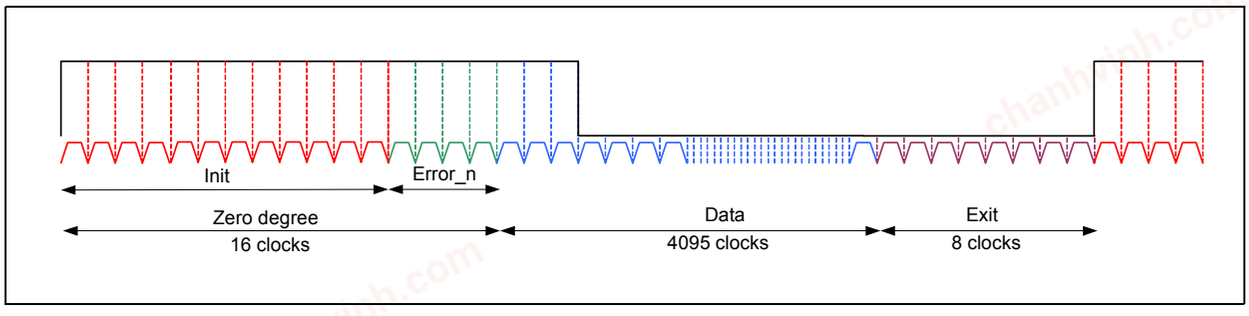


Figure 34:
PWM Period and Resolution

Parameter	Symbol	Value	Unit
PWM Frequency	F_PWM	1	KHz
PWM Pulse period	T_PWM	4119	bit

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Application Information

Programming of the AS5048

Programming of the Zero Position: The absolute angle position can be permanent programmed over the interface. This could be useful for random placement of the magnet on the rotation axis. A readout at the mechanical zero position can be performed and written back into the IC. With permanent programming the position is non-reversible stored in the IC. This programming can be performed only once.

To simplify the calculation of the zero position it is only needed to write the value in the IC which was read out before from the angle register.

Programming Sequence with Verification: To program the zero position is needed to perform following sequence:

1. Write 0 into OTP zero position register to clear
2. Read angle information
3. Write previous read angle position into OTP zero position register

Now the zero position is set.
If you want to burn it to the OTP register send:

4. Set the Programming Enable bit in the OTP control register
5. Set the Burn bit to start the automatic programming procedure
6. Read angle information (equals to 0)
7. Set the Verify bit to load the OTP data again into the internal registers
8. Read angle information (equals to 0)

The programming can either be performed in 5V operation using the internal LDO, or in 3V operation but using a minimum supply voltage of 3.3V. In case of 3V operation, also a 10µF capacitor is required on the VDD3 pin.

Programming the I^2C Slave address: For informations of programming the I^2C Slave address please refer to our application note covering this topic.

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Diagnostic Functions of the AS5048

The AS5048 provides diagnostics functions of the IC and also diagnostic functions of the magnetic input field

Following diagnostic flags are available:

See Figure 22 register address x3FFD (AS5048A) or Figure 31 register address 251 dec (AS5048B)

- **OCF** (**O**ffset **C**ompensation **F**inished), logic high indicates the finished Offset Compensation Algorithm. After power up the flag remains always to logic high.
- **COF** (**C**ORDIC **O**ver**f**low), logic high indicates an out of range error in the CORDIC part. When this bit is set, the angle and magnitude data is invalid. The absolute output maintains the last valid angular value.
- **COMP low**, indicates a high magnetic field. It is recommended to monitor in addition the magnitude value.
- **COMP high**, indicated a weak magnetic field. It is recommended to monitor the magnitude value.

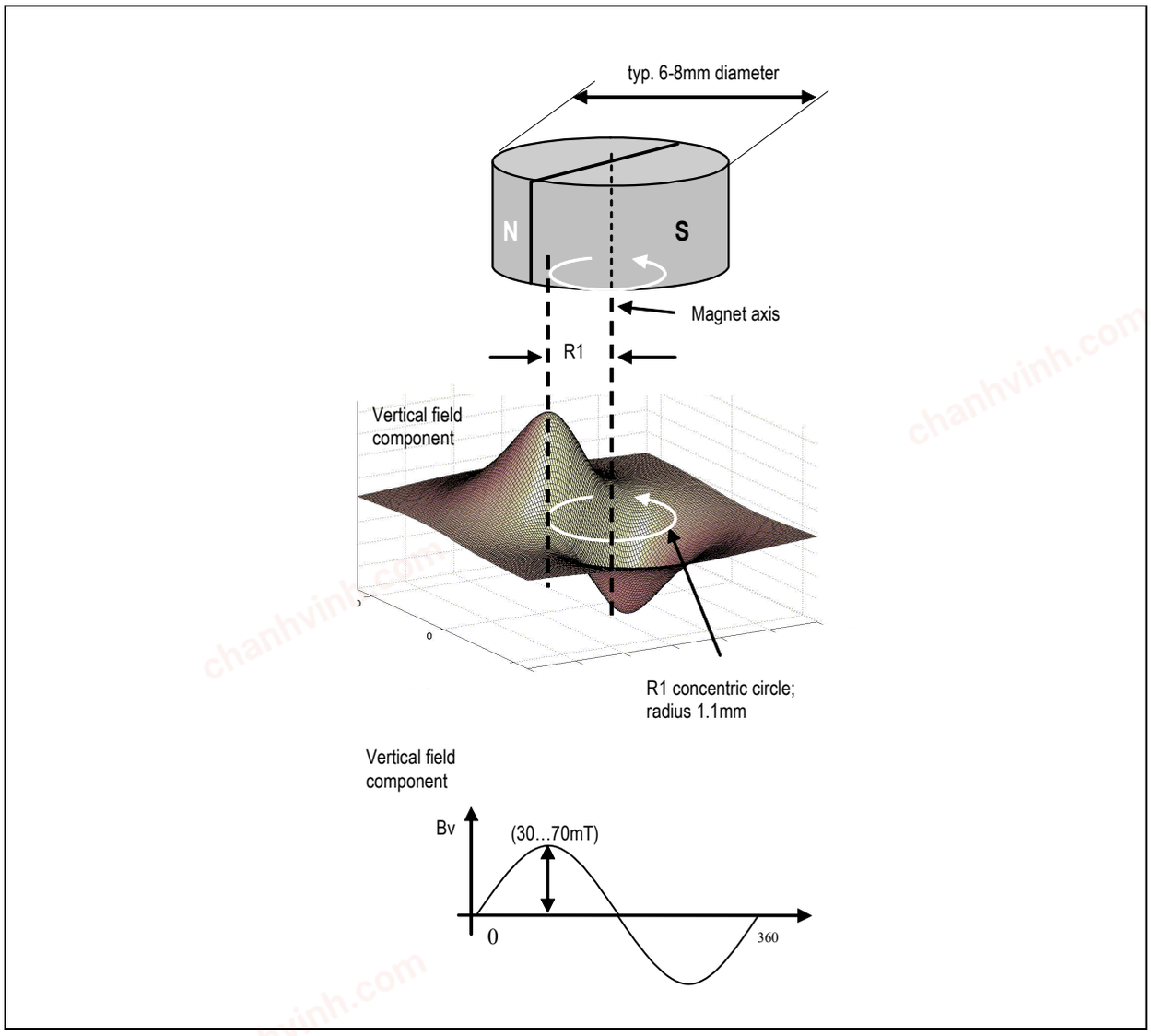
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Choosing the Proper Magnet

The AS5048 works with a variety of different magnets in size and shape. A typical magnet could be 6-8 mm in diameter and ≥2.5mm in height The magnetic field strength perpendicular to the die surface has to be in the range of ±30mT … ±70mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic flux B_Z at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±30mT… ±70mT.

Figure 35:
Typical Magnet and Magnetic Flux Distribution

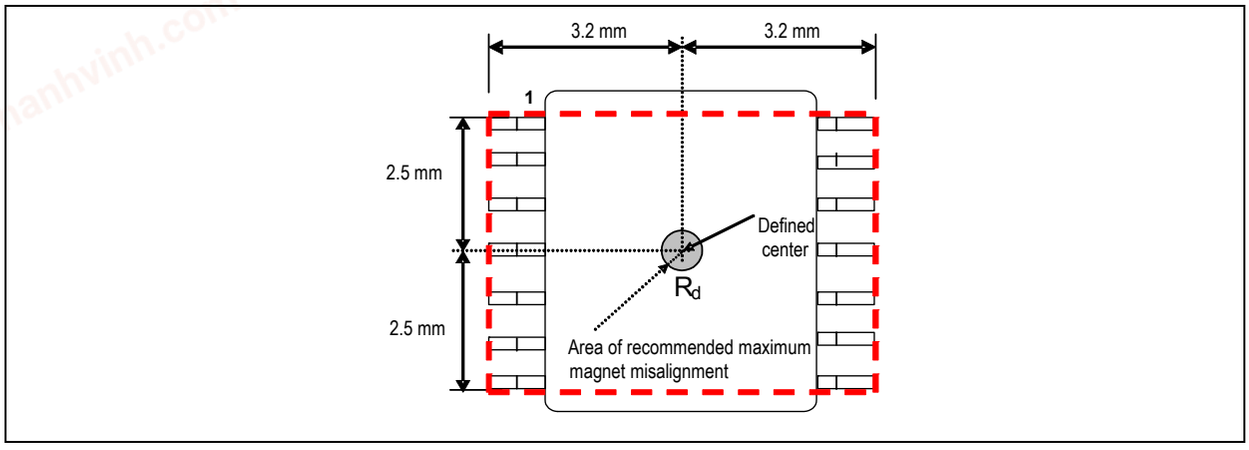


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Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below:

Figure 36:
Defined Chip Center and Magnet Displacement Radius



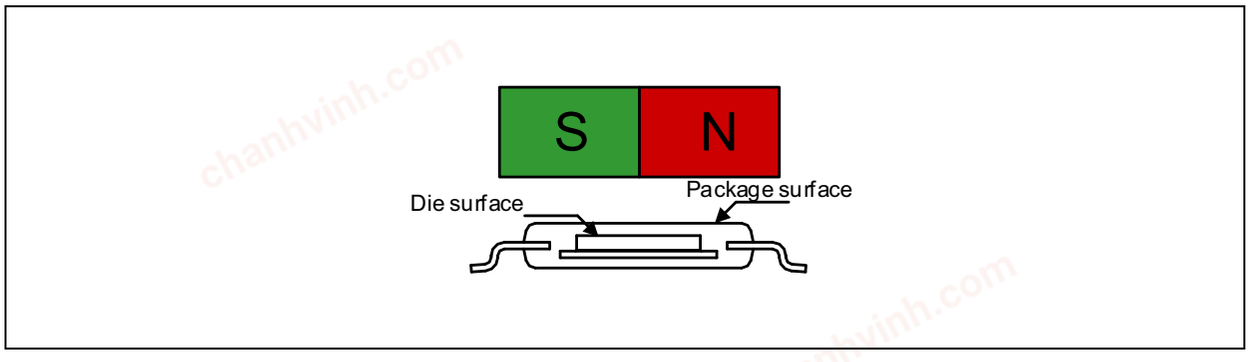
Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25 mm (larger magnets allow more displacement e.g. 0.5 mm) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits The typical distance "z" between the magnet and the package surface is 0.5mm to 2.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by indication flags.

Figure 37:
Vertical Placement of the Magnet

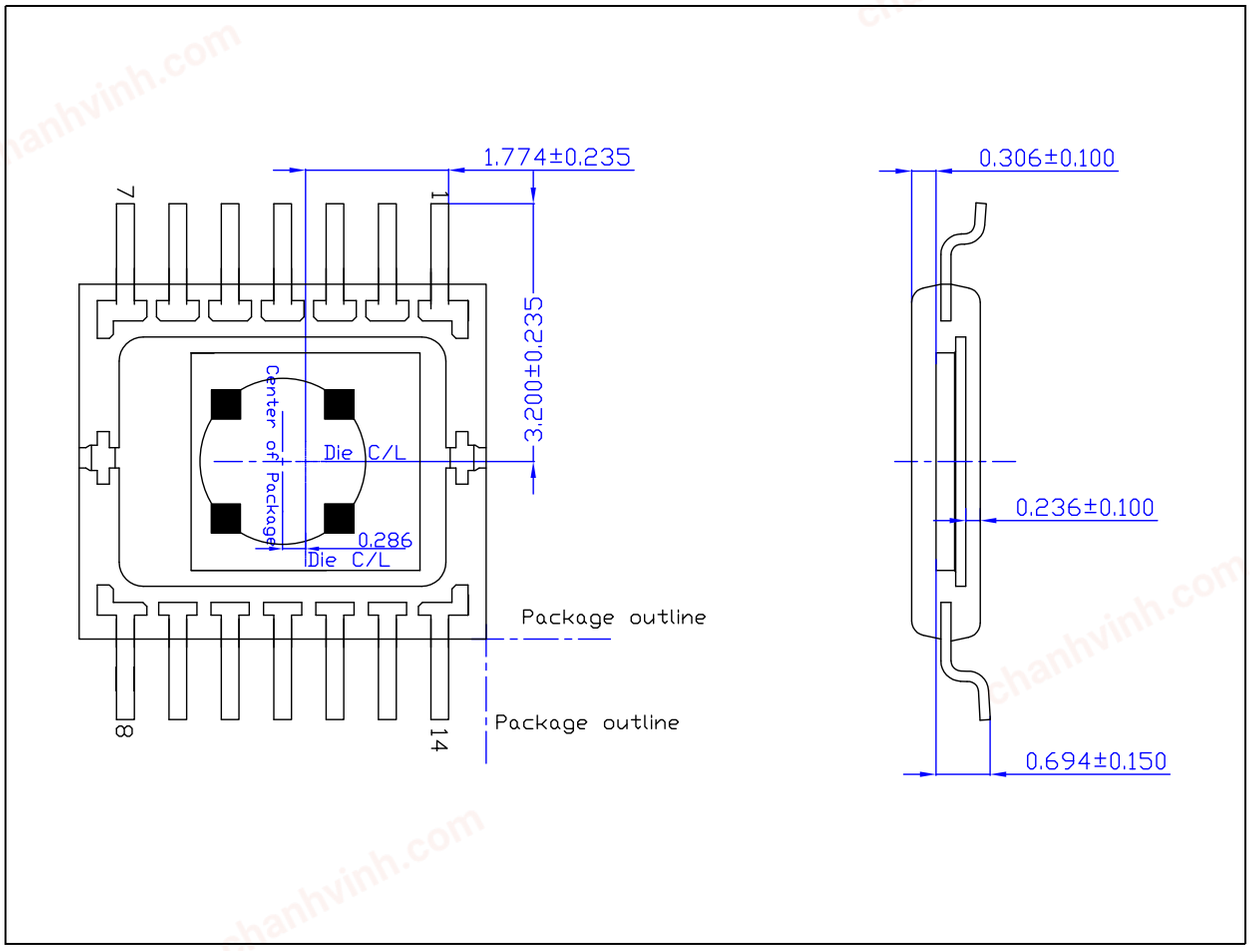


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Mechanical Data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1.1 mm.

Figure 38:
Hall Element Positions



Note(s):

1. All dimensions in mm.
2. Die thickness 203µm nom.
3. Adhesive thickness 30 ± 15µm.
4. Leadframe downset 152 ± 25 µm.
5. Leadframe thickness 125 ± 8 µm.

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Package Drawings & Markings

Package type: TSSOP14

Figure 39:
Package Markings for AS5048A & AS5048B

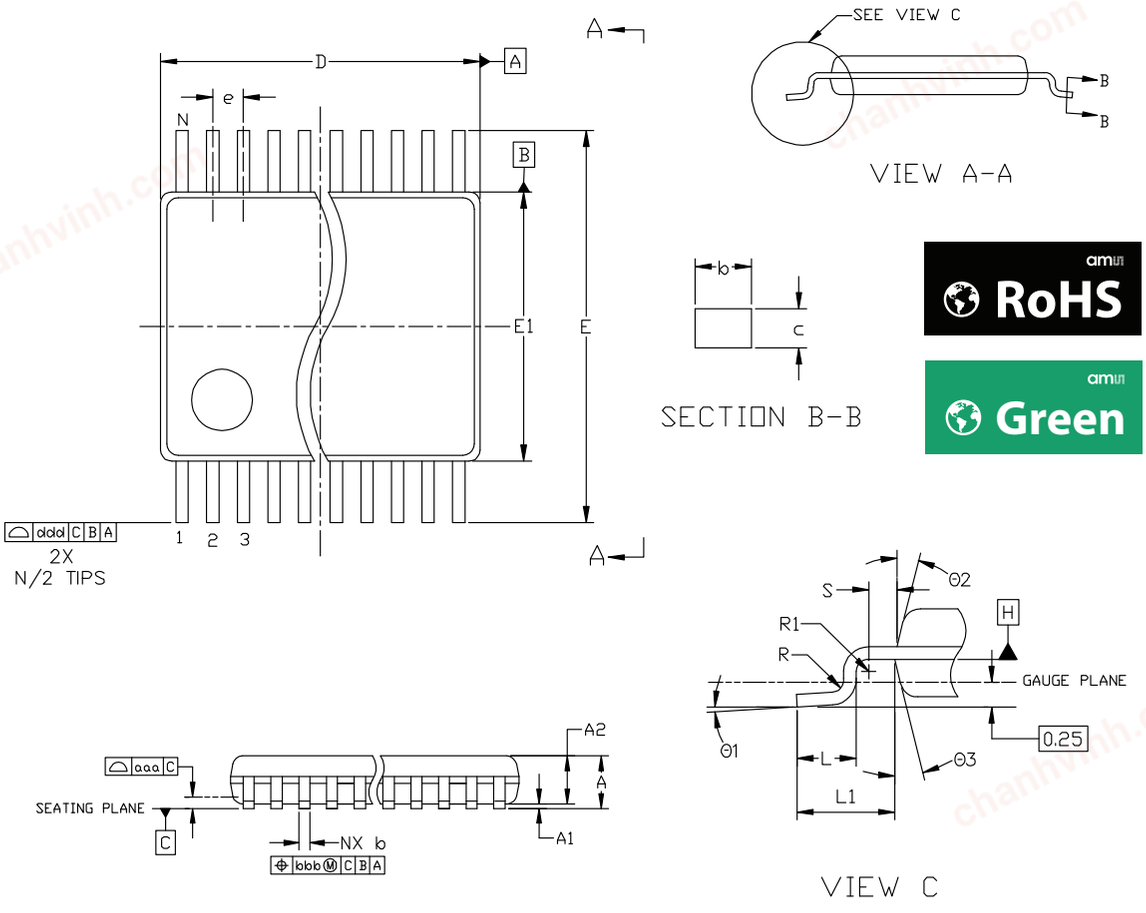


Figure 40:
Package Code YYWWMZZ

YY	WW	M	ZZ
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Letters for free traceability

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Figure 41:
14-Lead Thin Shrink Small Outline Package TSSOP-14



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	-	6.40 BSC	-
E1	4.30	4.40	4.50
e	-	0.65 BSC	-
L	0.45	0.60	0.75
L1	-	1.00 REF	-

Symbol	Min	Nom	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	-	12 REF	-
θ3	-	12 REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N		14	

Note(s):

1. Dimensioning & toleranceing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.

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Ordering & Contact Information

The devices are available as standard products.

Figure 42:
Ordering Information

Ordering Code	Package	Description	Delivery Form
AS5048A-HTSP	TSSOP 14	14 –Bit Programmable Magnetic Rotary Encoder with SPI-Interface	Tape & Reel
AS5048B-HTSP	TSSOP 14	14 –Bit Programmable Magnetic Rotary Encoder with I^2C-Interface	Tape & Reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from 1-09 (2016-Nov-15) to current revision 1-11 (2018-Jan-29)	Page
1-09 (2016-Nov-15) to 1-10 (2018-Jan-25)	
Updated Figure 5	4
1-10 (2018-Jan-25) to 1-11 (2018-Jan-29)	
Updated Figure 6	5

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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