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Revision History

5GB & 10GB 3D pSLC eMMC v5.1 153ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release - Preliminary	May. 2024

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ASFC 3D pSLC Series – Industrial embedded MMC 5.1 5 GBytes and 10 GBytes

1. ProductSummary

- **Capacities:** 5GBytes & 10 GBytes
- **OperatingTemperatureRange[1]:**
  - Industrial Operating Temperature -40 to 85°C

2. ProductFeatures

- Fully compliant with JEDEC e·MMC 5.1 Standard (JESD84-B51)
- 153-ball BGA, 0.5mm pitch, 11.5 x 13mm, RoHS compliant
- 3D TLC NAND base technology in Enhanced Mode (pSLC)
- High performance e·MMC 5.1 specification
  - Eleven-wire bus (clock, Data Strobe, 1 bit command, 8 bit data bus) and a hardware reset
  - Three different data bus width modes: 1-bit (default), 4-bit, and 8-bit
  - Clock frequencies 0-200MHz, High Speed Mode HS400
  - Command Queue Feature according to e·MMC Spec 5.1
  - Up to 330MB/s sequential read and up to 250MB/s sequential write
- Power Supply: (Low-power CMOS technology)
  - VCCQ 1.7V to 1.95V or 2.7V to 3.6V e·MMC supply / VCC 2.7V to 3.6V NAND Flash supply
- Optimized FW algorithms
  - Power-fail data loss protection
  - Wear Leveling technology
    Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is ensured
  - Read Disturb Management
    The read commands per region are monitored and the content is conditionally refreshed when critical levels have occurred
  - Auto Read Refresh
    The interruptible background process maintains the user data for Read Disturb effects or Retention degradation due to high temperature effects
  - Diagnostic features with Device Health Report according to e·MMC Spec 5.1, and detailed Lifetime Monitor data (Alliance proprietary, accessible through standard e·MMC commands).
  - Field Firmware update[2] according to e·MMC Spec 5.1
  - Discard and Sanitize, Trim
  - Boot Operation Mode and Alternative Boot Operation Mode
  - Replay Protected Memory Block (RPMB)

Note:

[1] Adequate airflow is required to ensure the temperature does not exceed 85°C (industrial temperature drive)
[2] The support of In-Field FW update capabilities on host systems is recommended.

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3. Ordering Information

Table 1. Ordering Information

Capacities (GB)	Part Number	eMMC Version	NAND Die	Temperature	Package Size (mm)	Package Type
5GB	**ASFC5G31P3-51BIN**	5.1	128Gb x 1	Industrial Grade -40°C ~ 85°C	11.5x13.0x1.0	153ball FBGA
10GB	**ASFC10G31P3-51BIN**	5.1	256Gb x 1	Industrial Grade -40°C ~ 85°C	11.5x13.0x1.0	153ball FBGA

4.Product Description

The Alliance e·MMC is a managed non-volatile storage consisting of a single chip MMC controller and a NAND flash memory chip inside a JEDEC defined standard BGA package. It is specially designed as a small form factor memory product for storage of data and as a boot media. The performance is optimized to a mostly read operation mode at low power consumption. The utilization of 3D pSLC NAND technology targets higher demanding and write intensive industrial applications, which is supported by the industrial temperature grade specification.

The e·MMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing. The 3D pSLC firmware features support high throughput for large data transfers and performance for small random data more commonly found in code usage. It also contains several security features as well as multiple boot partitions. Uses advanced refresh features for retention optimization for read intensive applications.

e·MMC communication is based on an advanced 11-signal bus. The communication protocol is defined as a part of the JEDEC e·MMC standard and referred to as the e·MMC mode.

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4.1 Performance Specifications

The read/write sequential and random CDM performance benchmarks are detailed in Table 2.

Table 2: Read/Write Performance

ASFC5G31P3-51BIN						
Capacity	**Max. Sequential Read HS400 (MBPS)**	**Max. Sequential Write HS400 (MBPS)**	**Max. Random Read 4K HS400 (IOPS)**		**Max. Random Write 4K HS400 (IOPS)**	
	measuring tool CDM	measuring tool CDM	Proprietary tool[3]	measuring tool CDM	Proprietary tool[3]	measuring tool CDM
5 GBytes	270	120	17,500	4,200	17,500	2000
Capacity	**Max. Sequential Read HS200 (MBPS)**	**Max. Sequential Write HS200 (MBPS)**	**Max. Random Read 4K HS200 (IOPS)**		**Max. Random Write 4K HS200 (IOPS)**	
	measuring tool CDM	measuring tool CDM	Proprietary tool[3]	measuring tool CDM	Proprietary tool[3]	measuring tool CDM
5 GBytes	180	95	17,500	n.a	17,500	n.a

Table 3: Read/Write Performance

ASFC10G31P3-51BIN						
Capacity	**Max. Sequential Read HS400 (MBPS)**	**Max. Sequential Write HS400 (MBPS)**	**Max. Random Read 4K HS400 (IOPS)**		**Max. Random Write 4K HS400 (IOPS)**	
	measuring tool CDM	measuring tool CDM	Proprietary tool[3]	measuring tool CDM	Proprietary tool[3]	measuring tool CDM
10 GBytes	280	120	17,500	4,300	20,500	2,050
Capacity	**Max. Sequential Read HS200 (MBPS)**	**Max. Sequential Write HS200 (MBPS)**	**Max. Random Read 4K HS200 (IOPS)**		**Max. Random Write 4K HS200 (IOPS)**	
	measuring tool CDM	measuring tool CDM	Proprietary tool[3]	measuring tool CDM	Proprietary tool[3]	measuring tool CDM
10 GBytes	180	115	17,500	n.a	20,000	n.a

Please note that Gen3 Flash variants were measured with Crystal Disk Mark x64 5x 1GiB (CDM 7.0.0) only

Note:

3. Controller supplier proprietary reader board: measuring without OS

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4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in Table 4.

Table 4: Current Consumption

ASFC5G31P3-51BIN/ASFC10G31P3-51BIN							
Capacity	Typ. Read Current		Typ. Write Current		Typ. Sleep Current		Unit
	V_{CCQ} 1.8V	V_{CC} 3.3V	V_{CCQ} 1.8V	V_{CC} 3.3V	V_{CCQ} 1.8V	V_{CC} 3.3V	
5 GBytes	131	77	89	43	0.06	0.02	mA
10 GBytes	132	77	89	40	0.06	0.02	

Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, V_{CC}= 3.3V±5%, V_{CCQ}=1.8V±5%

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

The recommended operating conditions are provided in Table 5.

Table 5: Recommended Operating Conditions[4]

Parameter	Value
Industrial Operating Temperature	-40°C to 85°C
Power Supply V_{CC} Voltage	2.7-3.6V
Power Supply V_{CCQ} Voltage	1.7-1.95V or 2.7-3.6V

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in Table 6.

Table 6: Recommended Storage Conditions

Parameter	Value
Industrial Storage Temperature	-40°C to 85°C

Note:

4. Adequate airflow is required to ensure the temperature does not exceed 85°C (industrial temperature drive)

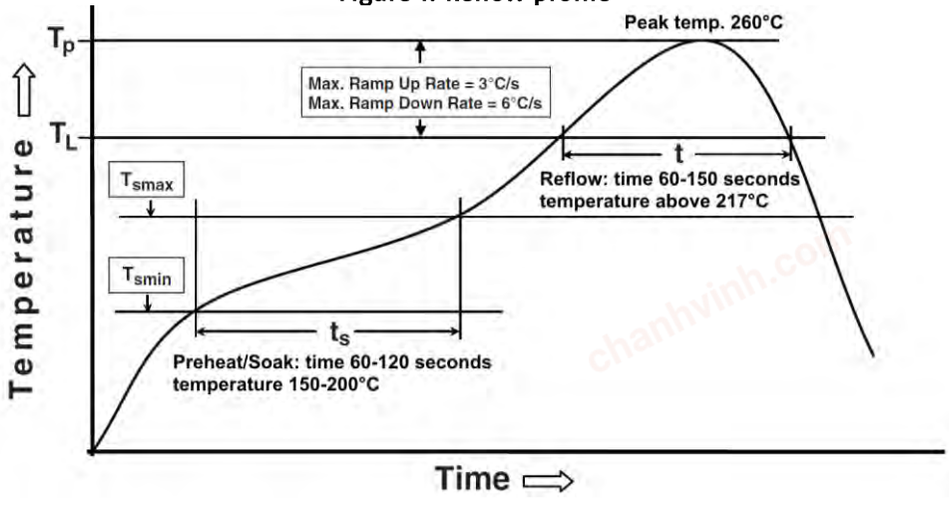
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4.3.3 Reflow profile and MSL

Table 7: Reflow and MSL conditions

Parameter	Condition
MSL	Level 3 (storage condition 168 hours, ≦30°C/ 60% RH)
Reflow	According to IPC/JEDEC J-STD-020D.1: Peak temp 260°C, 217°C endurance 60~150 seconds

Figure 1: Reflow profile



4.3.4 EMC

Table 8: EMC / EMI

Parameter	Value
EMC / EMI	Human Body Model: up to ±2 kV according to MIL-STD-883G, Method 3015.7
	Charged Device Model: up to ±500 V according to JESD22-C101

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4.4 Mechanical Specifications

Physical dimensions are detailed in Table 9. Also refer to Figure 2.

Table 9: Physical Dimensions

Physical Dimensions		Unit
Length	13±0.1	mm
Width	11.5±0.1	
Thickness (Max)	1.2 max.	
Weight (Max Capacity)	< 1g	g

4.5 Reliability and Endurance

Data retention at the beginning and end of life is provided in following Table 10.

Table 10: Reliability

Parameter[5]	Value
Data Retention at beginning @ 40°C	10 years
Data Retention at life end (30k PE cycles) @ 40°C	1 year

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) is provided as maximum values in the following Table 11.

Table 11: Endurance[6]

ASFC5G31P3-51BIN/ASFC10G31P3-51BIN		
Capacity	Max. Endurance	
	TBW	DWPD[7]
5 GBytes	168	29.7
10 GBytes	330	29.2

Note:

5.NAND Flash data retention and endurance characteristics are defined according to JEDEC JESD47 and JESD22. The endurance limits of the storage shall be monitored by the life time information and simulated before field usage by the customer.

6.According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume reduces the specified TBW. The values listed are estimates and are subject to change without notice.

7.DWPD values are based on a service life of 3 years

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4.6 Drive Geometry Specification

The user capacities are shown in following Table 12.

Table 12: Drive Geometry

Raw Capacity	User Capacity	Total LBA	User Addressable Bytes
		Decimal	(Unformatted)
16 GBytes	5 GBytes	10,059,776	5,150,605,312
32 GBytes	10 GBytes	20,135,936	10,309,599,232

Table 13: Partition capacity specification

Capacity	Boot partition 1	Boot partition 2	RPMB
5 to 10 GBytes	32,256KB	32,256KB	4,096KB

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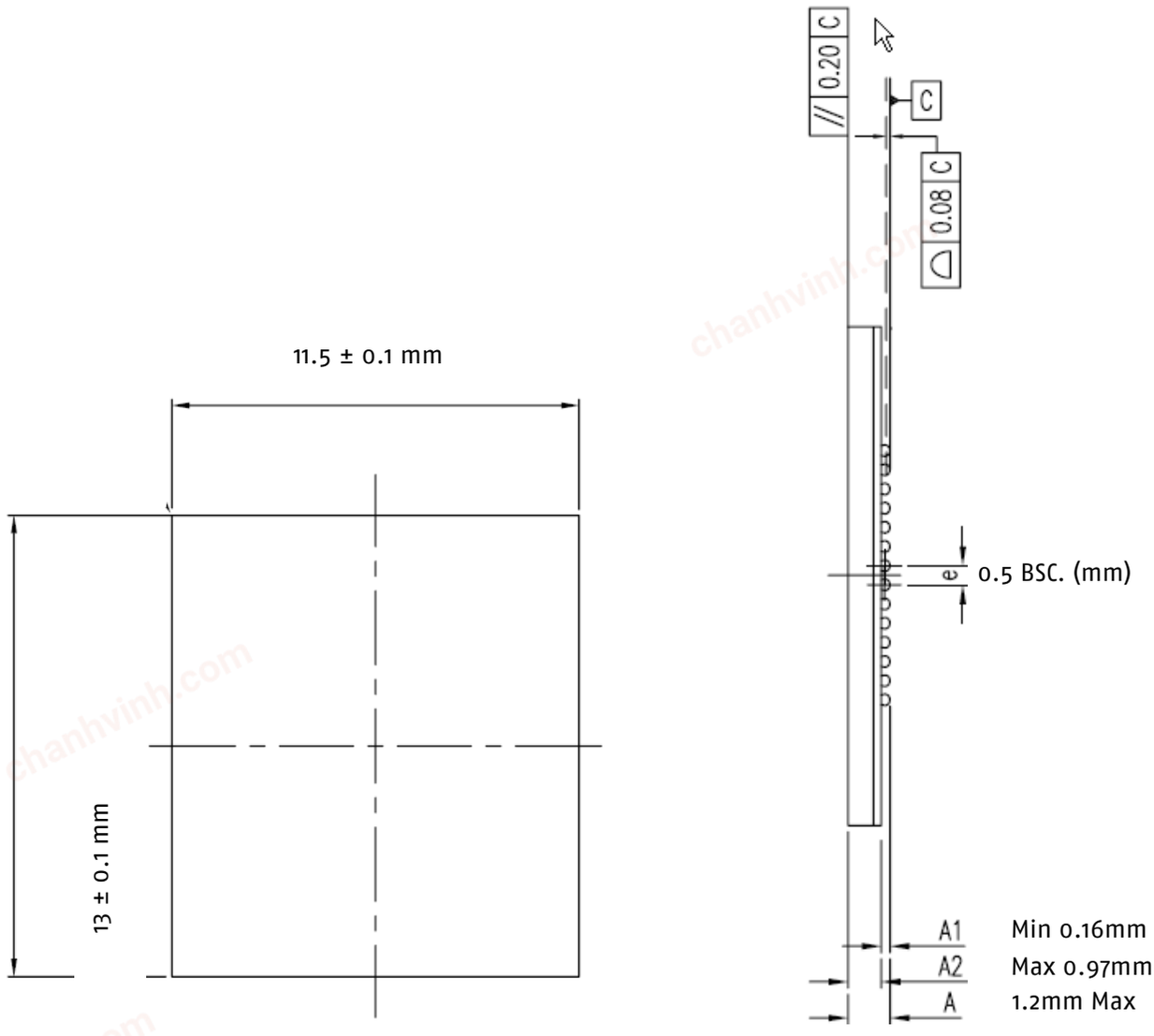
5. Package Mechanical

5.1 Physical description

The e·MMC contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 2 and Figure 3 show card dimensions.

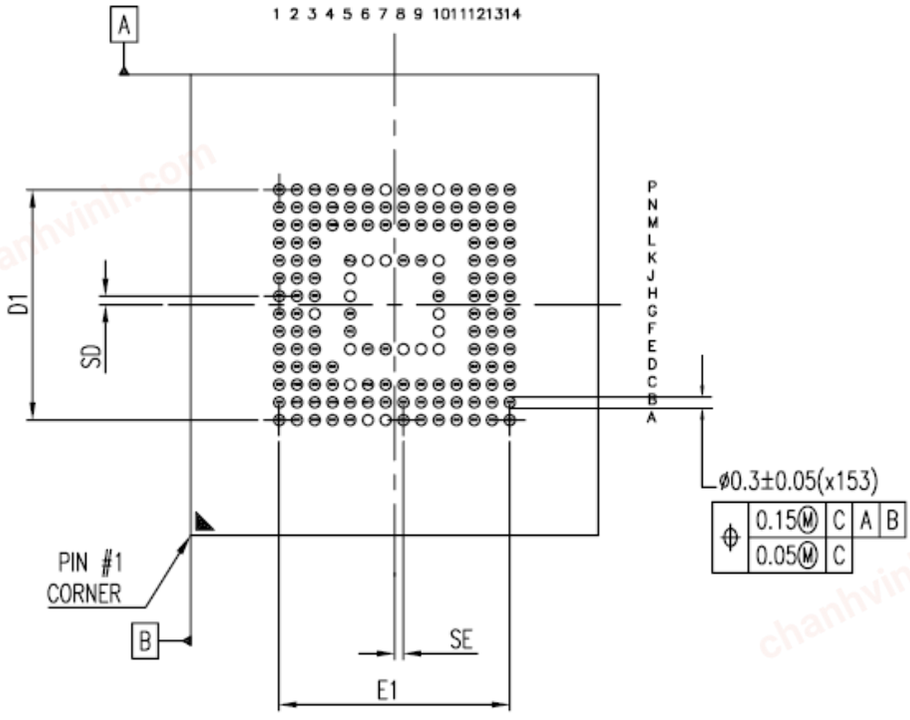
Figure 2: Mechanical dimensions e·MMC

Package Mechanical (11.5 x 13.0 x 1.2mm)



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Figure 3: Mechanical dimensions e·MMC



BOTTOM VIEW

N	SE (MM)	SD (MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

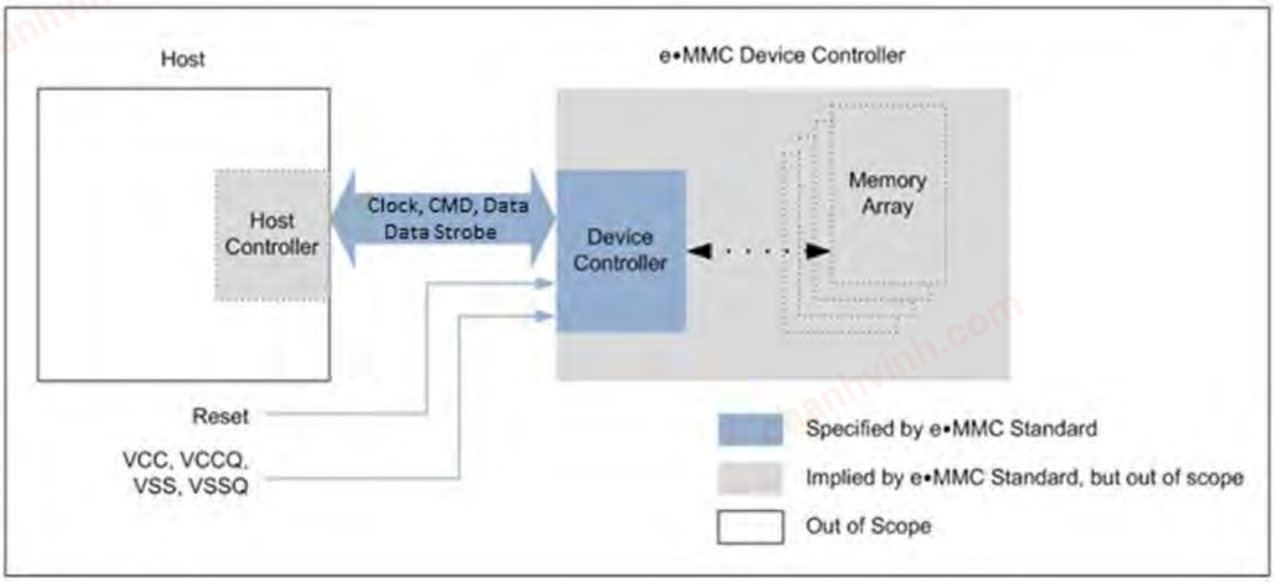
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6. e•MMC device and system

6.1 e•MMC system overview

The e•MMC specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

Figure 4: e•MMC System Overview



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6.2 Pinout

Figure 5: Ball assignment (top view, ball down)

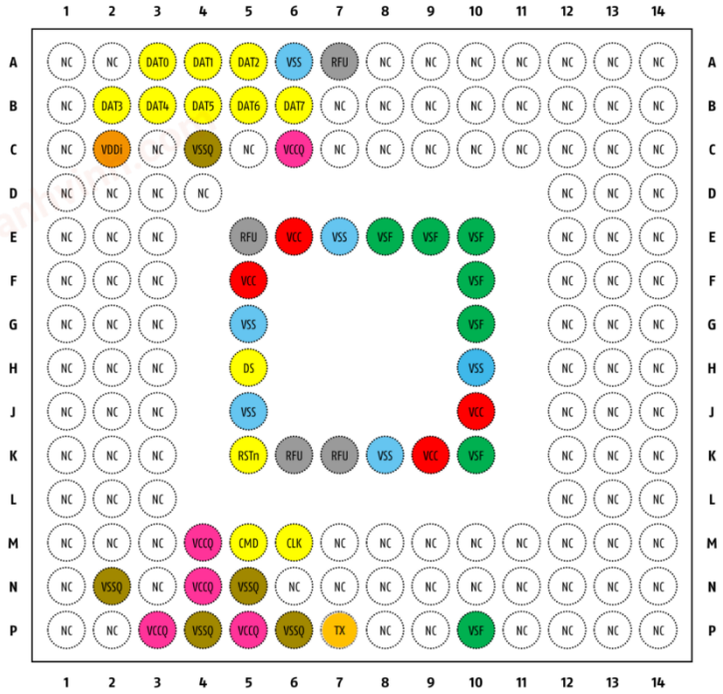


Table 14: Pinout

Name	Type[1]	Ball No.	Description
CLK	I	M6	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	I/O/PP/OD	M5	Command: A bidirectional channel used for device initialization and command transfer. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
DAT0	I/O/PP	A3	Data I/O0: Bidirectional channel used for data transfer.
DAT1	I/O/PP	A4	Data I/O1: Bidirectional channel used for data transfer.
DAT2	I/O/PP	A5	Data I/O2: Bidirectional channel used for data transfer.
DAT3	I/O/PP	B2	Data I/O3: Bidirectional channel used for data transfer.
DAT4	I/O/PP	B3	Data I/O4: Bidirectional channel used for data transfer.
DAT5	I/O/PP	B4	Data I/O5: Bidirectional channel used for data transfer.
DAT6	I/O/PP	B5	Data I/O6: Bidirectional channel used for data transfer.
DAT7	I/O/PP	B6	Data I/O7: Bidirectional channel used for data transfer.
RST_n	I	K5	Reset signal pin
VCC	S	E6, F5, J10, K9	VCC: Flash memory I/F and Flash memory power supply.
VCCQ	S	C6, M4, N4, P3, P5	VCCQ : Memory controller core and MMC interface I/O power supply.
VSS	S	A6, E7, G5, H10, J5, K8	VSS: Flash memory I/F and Flash memory ground connection.
VSSQ	S	C4, N2, N5, P4, P6	VSSQ: Memory controller core and MMC I/F ground connection.
VDDi		C2	VDDi : Connect capacitor Creg from VDDi to GND.
DS	O/PP	H5	Data Strobe: Newly assigned pin for HS400 mode.
NC			Not connected

1. I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected; S: power supply.

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6.3 e·MMC Communication Interface

The e·MMC device transfers data via a configurable number of data bus signals. The communication signals are:

- Clock (CLK)
  Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

- Data Strobe (DS)
  This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data – one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

- Command (CMD)
  This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e·MMC host controller to the e·MMC Device and responses are sent from the Device to the host.

- Input/Outputs (DAT0-DAT7)
  These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e·MMC host controller. The e·MMC Device includes internal pull-ups for data lines DAT1-DAT7.
  Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

6.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based e·MMC bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard JESD84-B51.

6.5 Bus Speed Modes

e·MMC defines several bus speed modes as shown in following Table 15.

Table 15: Bus Speed Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s
HS400	Dual	1.8V	8	0-200MHz	400MB/s

6.5.1 HS200 Bus Speed Mode

The HS200 mode offers the following features:

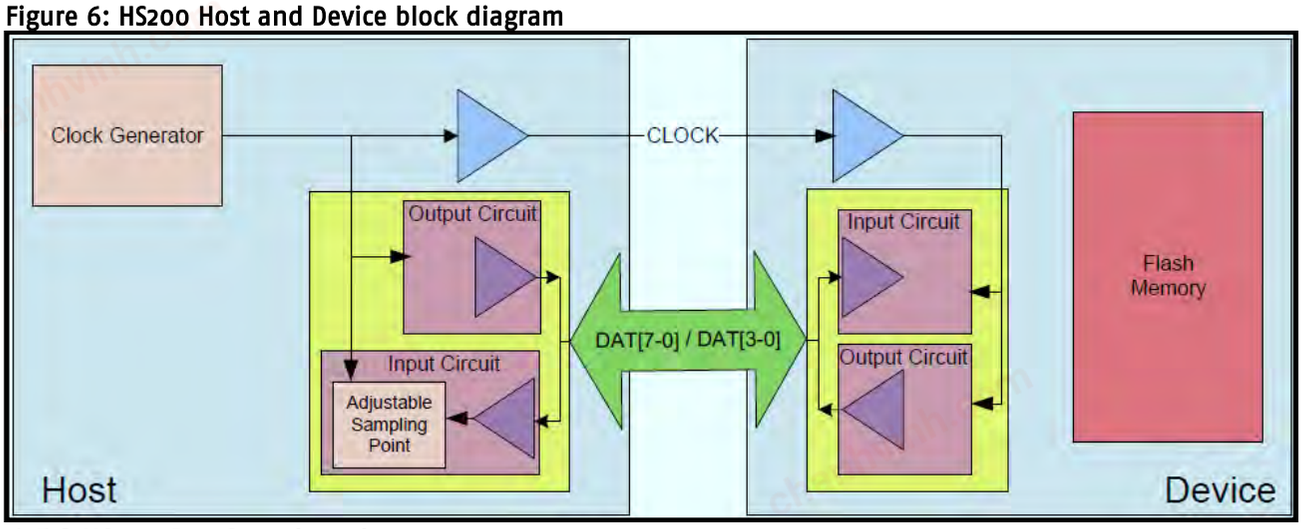
- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

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6.5.2 HS200 System Block Diagram

Figure 6 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

Figure 6: HS200 Host and Device block diagram



6.5.3 HS400 Bus Speed mode

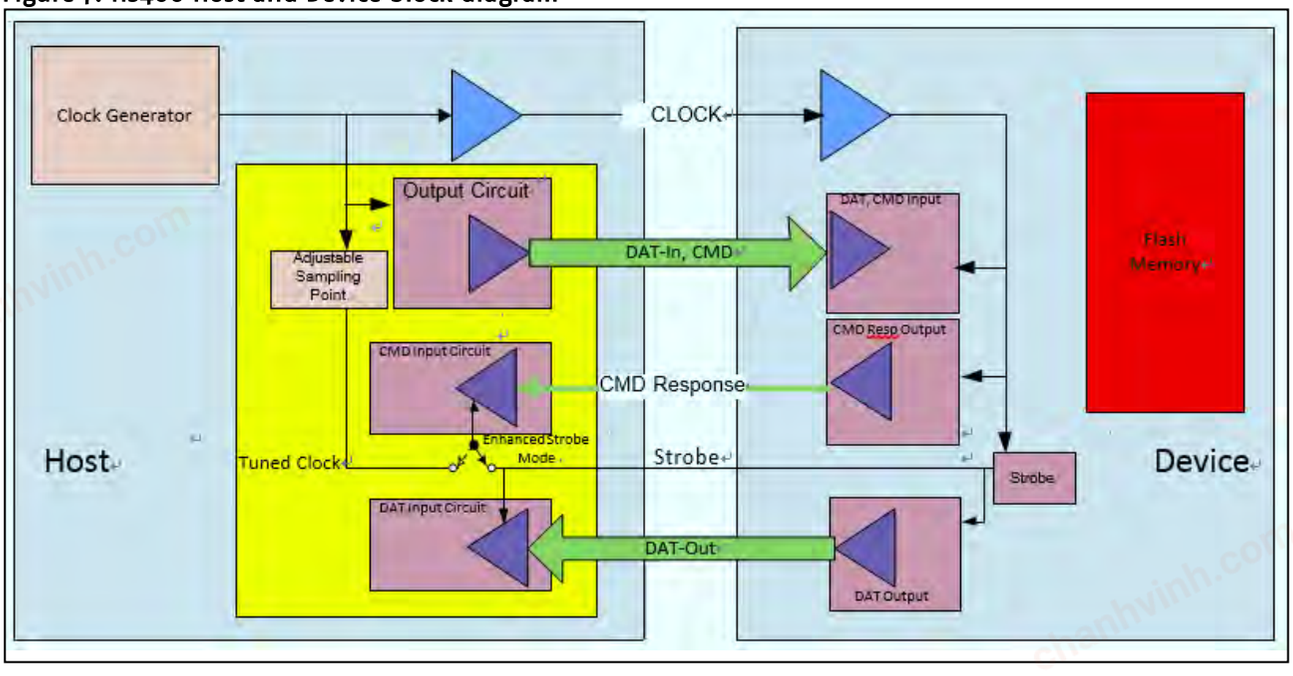
The HS400 mode has the following features:

- DDR Data sampling method
- CLK frequency up to 200MHz, Data rate is – up to 400MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 5 selective Drive Strength
- Data strobe signal is toggled only for Data out and CRC response

6.5.4 HS400 System Block Diagram

Figure 7 shows a typical HS400 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For read operations, Data Strobe is generated by device output circuit. Host receives the data which is aligned to the edge of Data Strobe.

Figure 7: HS400 Host and Device block diagram



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7. e·MMC Functional Description

7.1 e·MMC Overview

All communication between host and device are controlled by the host (master). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard JESD84-B51. Five operation modes are defined for the e·MMC system:

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

7.2 Boot Operation Mode

In boot operation mode, the master (e·MMC host) can read boot data from the slave (e·MMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard JESD84-B51.

7.3 Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard JESD84-B51.

7.4 Interrupt Mode

The interrupt mode on the e·MMC system enables the master (e·MMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting e·MMC interrupt mode is an option, both for the host and the Device. For more details, refer to section 6.5 of the JEDEC Standard JESD84-B51.

7.5 Data Transfer Mode

When the Device is in *Stand-by* State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard JESD84-B51.

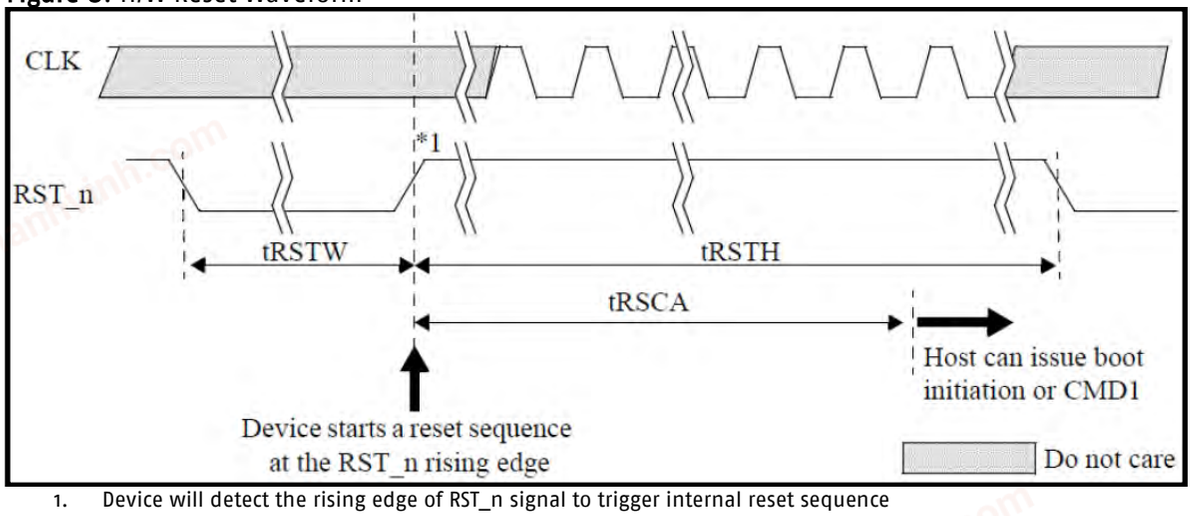
7.6 Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to *Pre-idle* state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard JESD84-B51.

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7.7 H/W Reset Operation

Figure 8: H/W Reset Waveform



1. Device will detect the rising edge of RST_n signal to trigger internal reset sequence

Table 16: H/W Reset Timing Parameters

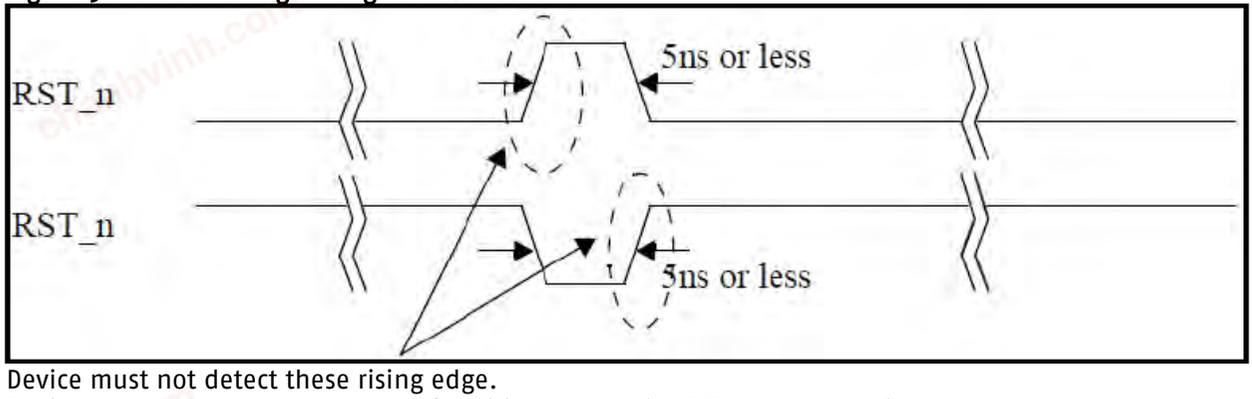
Symbol	Comment	Min.	Max.	Unit
tRSTW	RST_n pulse width	1		[us]
tRSCA	RST_n to Command time	200[1]		[us]
tRSTH	RST_n high period (interval time)	1		[us]

1. 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA

7.8 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity

Figure 9: Noise Filtering Timing for H/W Reset



Device must not detect these rising edge.
Device must not detect 5ns or less of positive or negative RST_n pulse. Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

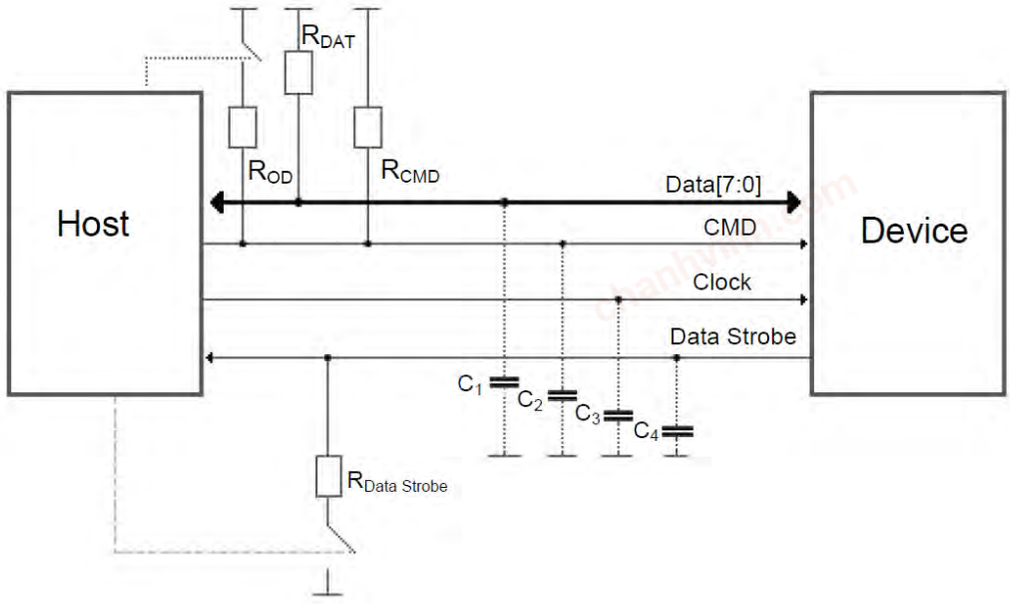
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8. The e·MMC bus

The e·MMC bus has eleven communication lines and three supply lines:

- CMD: Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- DATo-7: Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode.
- CLK: Clock is a host to Device signal. CLK operates in push-pull mode.
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

Figure 10: Bus Circuitry Diagram



The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.
A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used). Consequently the maximum operating frequency in the open drain mode has to be reduced if the used R_{CMD} value is higher than the minimal one given in.

$R_{Data\ strobe}$ is pull-down resistor used in HS400 device.

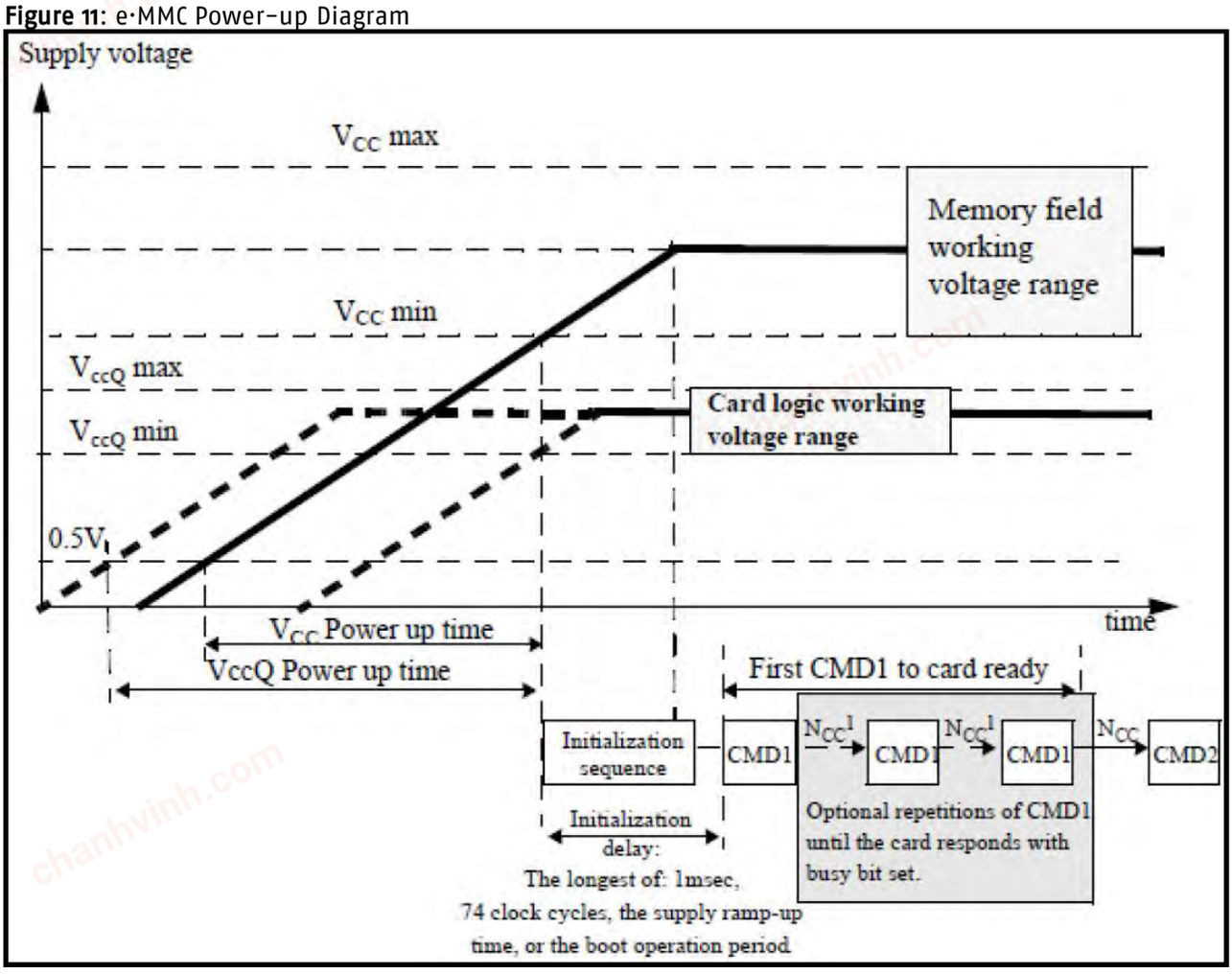
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8.1 Power-up

8.1.1 e·MMC power-up

An e·MMC bus power-up is handled locally in each device and in the bus master. Figure 11 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard JESD84-B51.

Figure 11: e·MMC Power-up Diagram

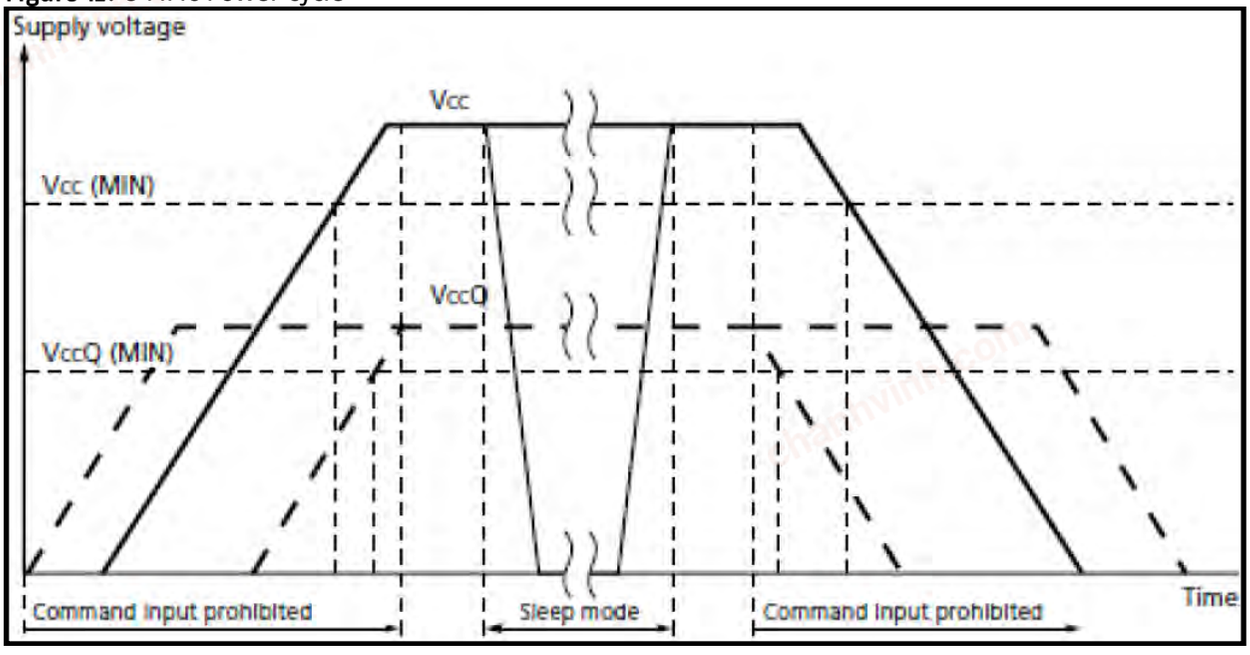


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8.1.2 e·MMC Power Cycling

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling refer to Section 10.1.3 of the JEDEC Standard JESD84-B51.

Figure 12: e·MMC Power Cycle



8.2 Bus Operating Conditions

Table 17: General Operating Conditions

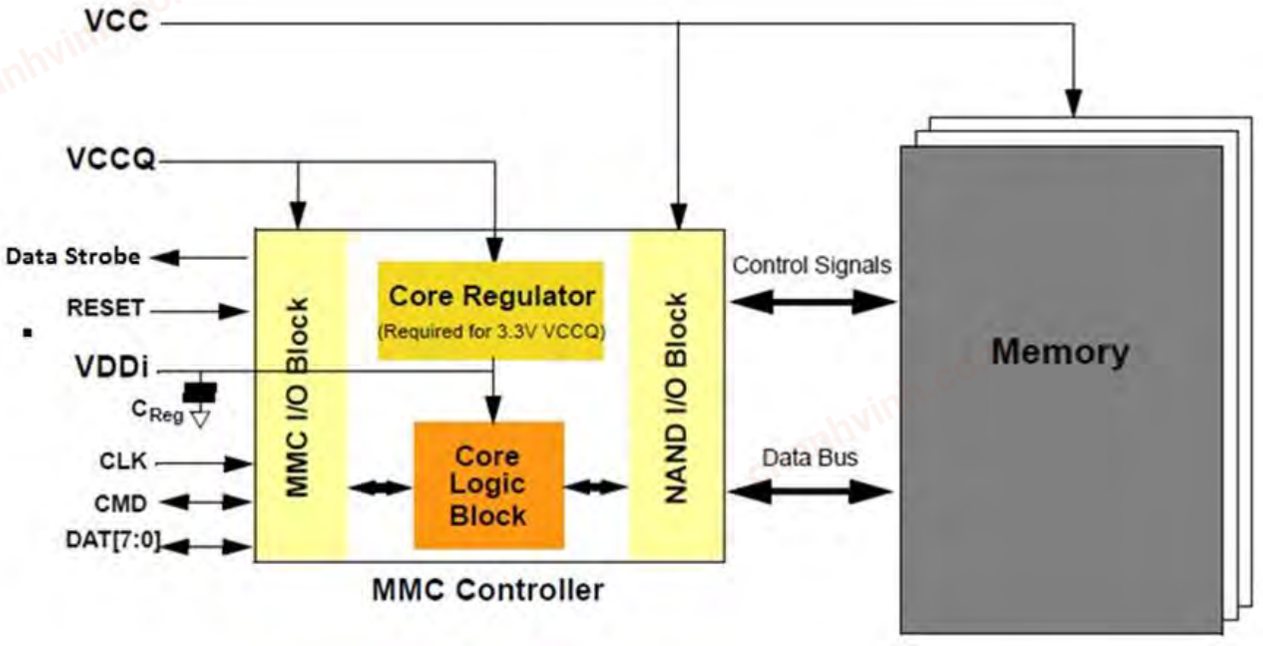
Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.5	V_{CCQ} + 0.5	V	
All Inputs					
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)		-100	100	µA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA	
All Outputs					
Output Leakage Current (before initialization sequence)		-100	100	µA	
Output Leakage Current (after initialization sequence)		-2	2	µA	

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8.2.1 Power supply e·MMC

In the e·MMC, V_{CC} is used for the NAND flash device and its interface voltage; V_{CCQ} is for the controller and the MMC interface voltage as shown in Figure 13. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ}. A C_{Reg} capacitor must be connected to the V_{DDi} terminal to stabilize regulator output on the system.

Figure 13: e·MMC Internal Power Diagram



8.2.2 e·MMC Power Supply Voltages

The e·MMC supports one or more combinations of V_{CC} and V_{CCQ} as shown in Table 18. The V_{CCQ} must be defined at equal to or less than V_{CC}.

Table 18: e·MMC Operating Voltage

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (NAND)	V_{CC}	2.7	3.6	V	
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V	
		1.7	1.95	V	
Supply power-up for 3.3V	t_{PRUH}		35	ms	
Supply power-up for 1.8V	t_{PRUL}		25	ms	

The e·MMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table 19).

Table 19: e·MMC Voltage Combinations

		V_{CCQ}	
		1.7V–1.95V	**2.7V–3.6V***
V_{CC}	**2.7V–3.6V**	Valid	Valid

* VCCQ (I/O) 3.3 volt range is not supported in HS200 /HS400 devices

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8.2.3 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of e·MMC connected to this line:

$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$

The sum of the host and bus capacitances must be under 20pF.

Table 20: Signal Line Load

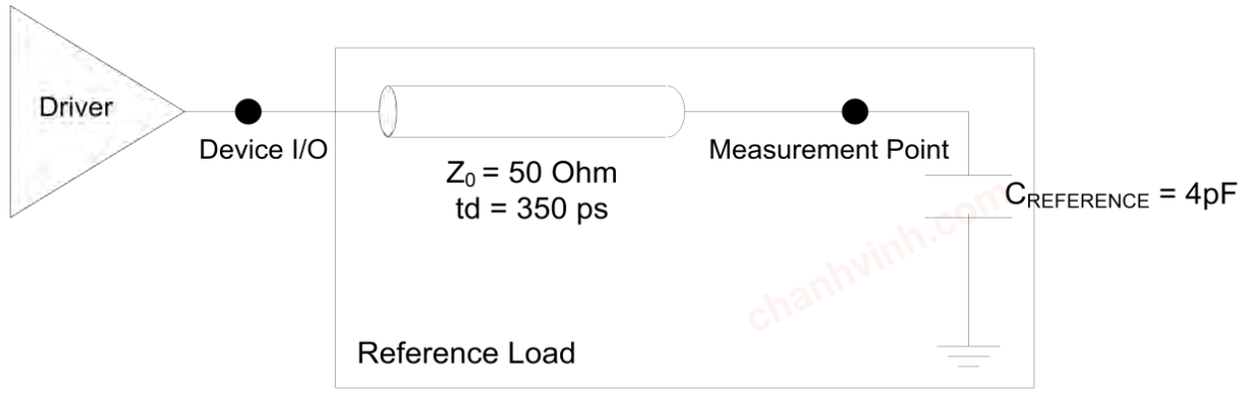
Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	Kohm	to prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10	50	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Bus signal line capacitance	CL		30	pF	Single Device
Single Device capacitance	C_{BGA}		6	pF	
Maximum signal line inductance			16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	ohm	Impedance match
Serial's resistance on CLK line	SR_{CLK}	0	47	ohm	
Serial's resistance on CMD / DAT0~7 line	SR_{CMD} $SR_{DAT0\sim7}$	0	47	ohm	
V_{CCQ} decoupling capacitor	$C_{VCCQ}1$	4.7	10	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
	$C_{VCCQ}2$	0.1	0.1		
V_{CC} capacitor value	$C_{VCC}1$	4.7	10	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
	$C_{VCC}2$	0.1	0.1		
V_{DDi} capacitor value	C_{REG}	1+0.1	2.2+0.1	µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

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8.2.4 HS400 reference load

The circuit in Figure 14 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.
The reference load is made up by the transmission line and the $C_{REFERENCE}$ capacitance.
The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.
System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.
Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

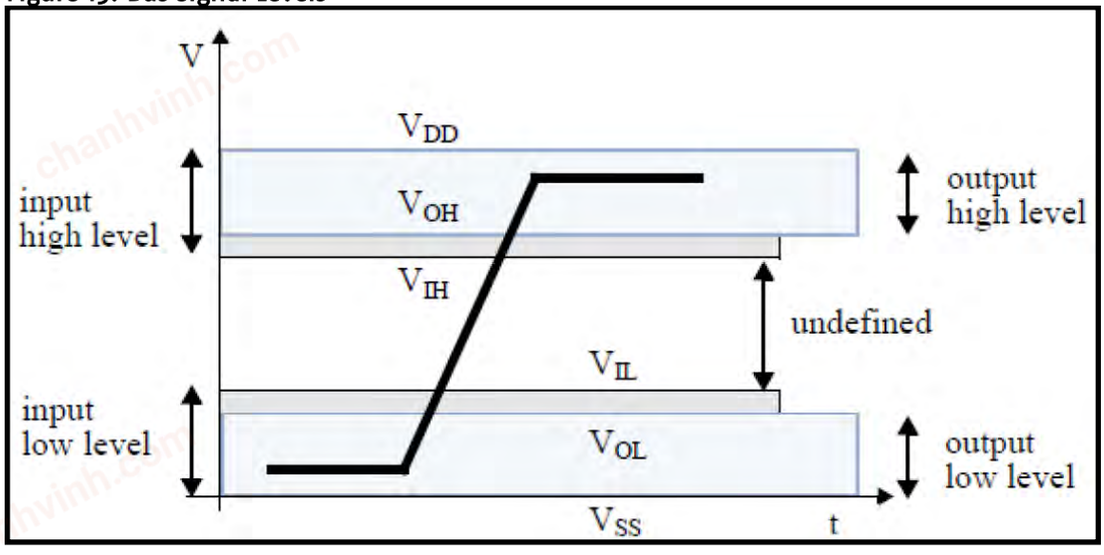
Figure 14: HS400 reference load



8.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 15: Bus Signal Levels



8.3.1 Open-drain Mode Bus Signal Level

Table 21: Open-drain Bus Signal Level

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	VOH	VDD – 0.2		V	IOH = -100 µA
Output LOW voltage	VOL		0.3	V	IOL = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

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8.3.2 Push-pull mode bus signal level– e·MMC

The device input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range

For 2.7V-3.6V V_{CCQ} range (compatible with JESD8C.01):

Table 22: Push-pull Signal Level—High-voltage e·MMC

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75 * V_{CCQ}		V	IOH = -100 µA @ V_{CCQ} min
Output LOW voltage	VOL		0.125 * V_{CCQ}	V	IOL = 100 µA @ V_{CCQ} min
Input HIGH voltage	VIH	0.625 * VCCQ	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	VSS – 0.3	0.25 * V_{CCQ}	V	

For 1.70V – 1.95V V_{CCQ} range (Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Normal Range" as defined in the following table):

Table 23: Push-pull Signal Level—1.70 -1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	VOH	V_{CCQ} – 0.45V		V	IOH = -2mA
Output LOW voltage	VOL		0.45V	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	V_{SS} – 0.3	0.35 * V_{DD} [2]	V	

Note 1: 0.7 * VDD for MMC™4.3 and older revisions.
Note 2: 0.3 * VDD for MMC™4.3 and older revisions.

8.3.3 Bus Operating Conditions for HS200 & HS400

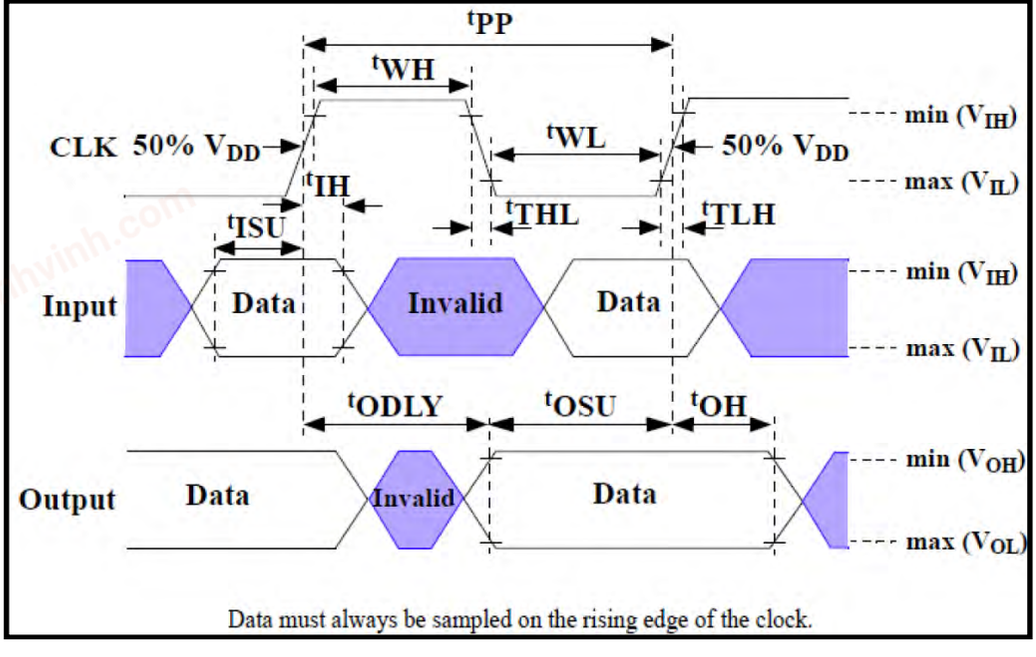
The bus operating conditions for HS200 & HS400 devices is the same as specified in sections 10.5.1 through 10.5.2 of JESD84-B51. The only exception is that V_{CCQ}=3.3v is not supported.

8.3.4 Device Output Driver Requirements for HS200 & HS400

Refer to section 10.5.4 of the JEDEC Standard JESD84-B51.

8.4 Bus Timing

Figure 16: Timing diagram: data input/output



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8.4.1 Device Interface Timings

Table 24: High-speed Device Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL ≤ 30 pF
Clock low time	tWL	6.5		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL ≤ 30 pF
Clock fall time	tTHL		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5		ns	CL ≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL ≤ 30 pF
Signal fall time	tFALL		3	ns	CL ≤ 30 pF

Note 1: CLK timing is measured at 50% of VDD.
Note 2: e·MMC shall support the full frequency range from 0-26MHz or 0-52MHz
Note 3: Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
Note 4: CLK rise and fall times are measured by min (VIH) and max (VIL).
Note 5: Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

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Table 25: Backward-compatible Device Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Remark[1]
Clock CLK[2]					
Clock frequency Data Transfer Mode (PP)[3]	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10			CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	tTHL		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	tOSU	11.7		ns	CL ≤ 30 pF
Output hold time[5]	tOH	8.3		ns	CL ≤ 30 pF

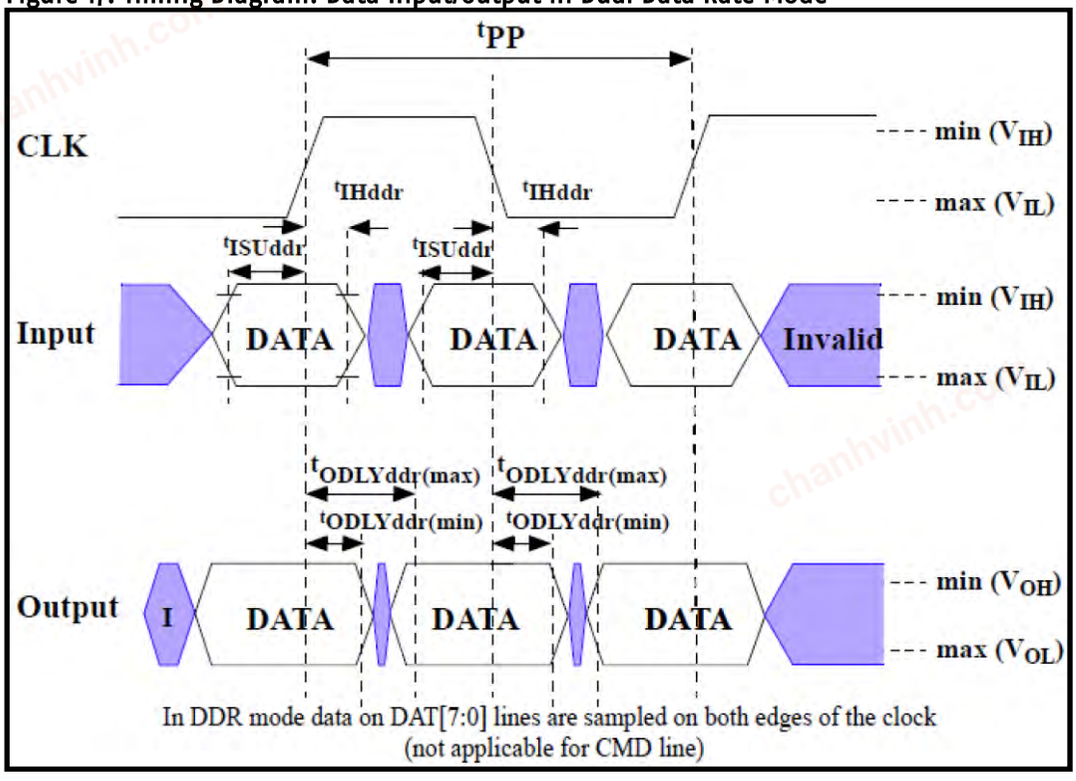
Note 1: The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
Note 2: CLK timing is measured at 50% of VDD.
Note 3: For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high speed interface timing.
Note 4: CLK rise and fall times are measured by min (VIH) and max (VIL).
Note 5: tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

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8.5 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.5 of JESD84-B51, therefore there is no timing change for the CMD signal.

Figure 17: Timing Diagram: Data Input/Output in Dual Data Rate Mode



8.5.1 Dual Data Rate Interface Timings

Table 26: High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

Note 1: CLK timing is measured at 50% of VDD.
Note 2: Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL)

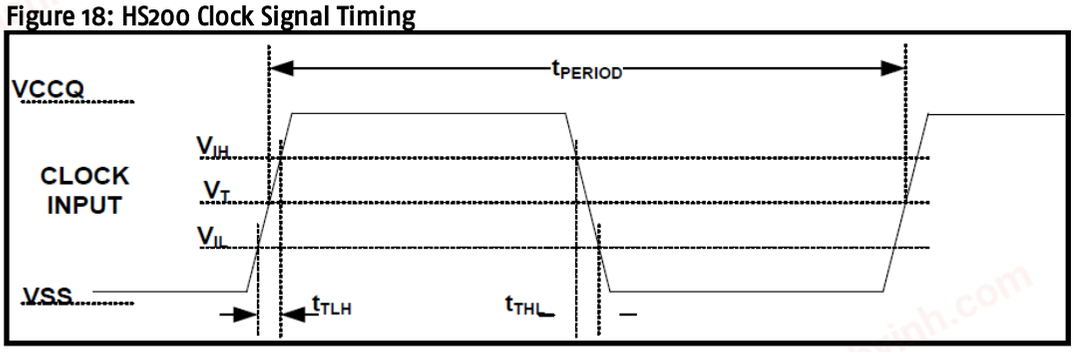
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8.6 Bus Timing Specification in HS200 Mode

8.6.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 18 and Table 27.
CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.
The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

Figure 18: HS200 Clock Signal Timing



Note 1: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).
Note 2: V_T=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

Table 27: HS200 Clock Signal Timing

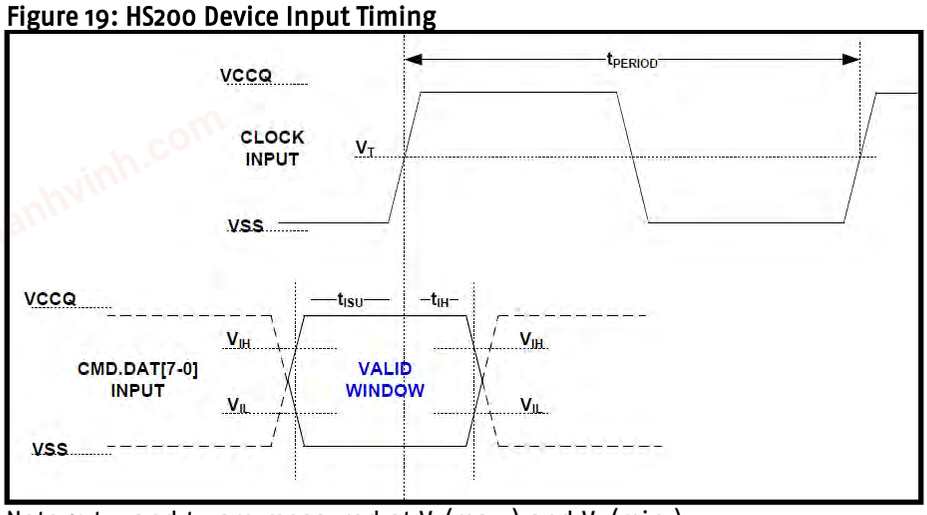
Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{BGA}=12pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

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8.6.2 HS200 Device Input Timing

Figure 19 and Table 28 define Device input timing.

Figure 19: HS200 Device Input Timing



Note 1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
Note 2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Table 28: HS200 Device Input Timing

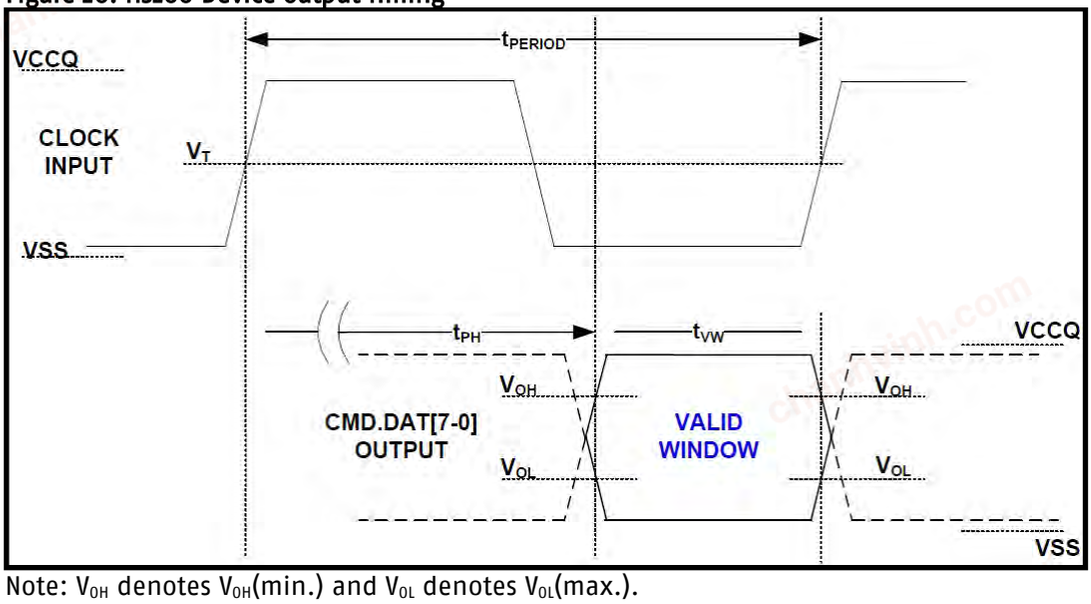
Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.4	-	ns	$C_{BGA} \leq 6pF$
t_{IH}	0.8		ns	$C_{BGA} \leq 6pF$

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8.6.3 HS200 Device Output Timing

t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD}. After initialization, the t_{PH} may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.
Figure 20 and Table 29 define Device output timing.
While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔT_{PH}. Output valid data window (t_{VW}) is available regardless of the drift (ΔT_{PH}) but position of data window varies by the drift, as described in Figure 21.

Figure 20: HS200 Device Output Timing



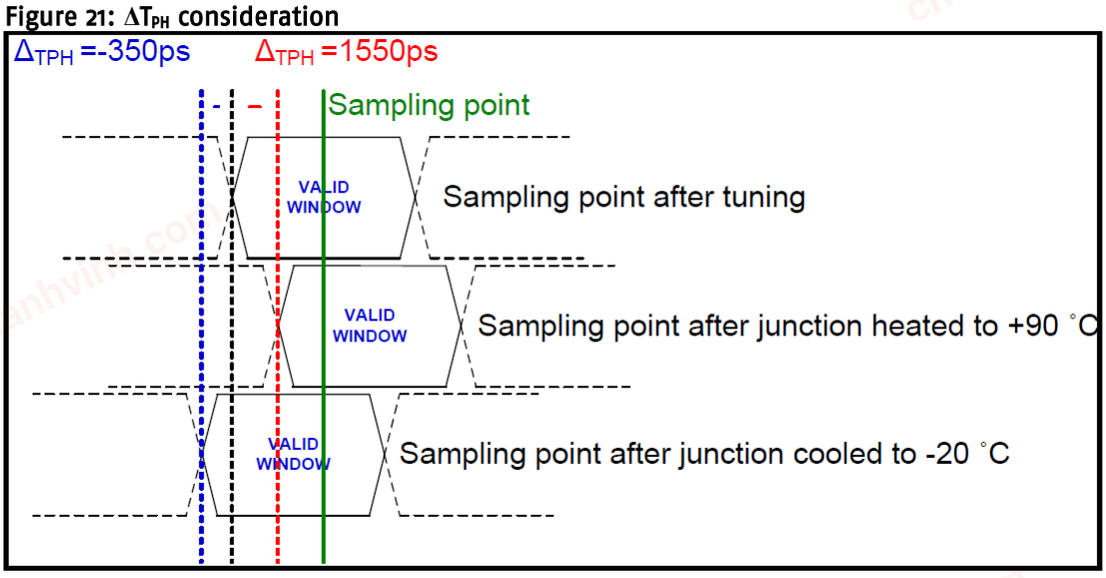
Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Table 29: Output Timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT= -20°C)	+1550 (ΔT=90°C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 85°C during operation.
T_{VW}	0.575	-	UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 15 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.
Note：Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

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Figure 21: ΔT_{PH} consideration



Implementation Guide: Host should design to avoid sampling errors that may be caused by the Δ_{TPH} drift.
It is recommended to perform tuning procedure while Device wakes up, after sleep.
One simple way to overcome the Δ_{TPH} drift is by reduction of operating frequency.

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8.7 Bus Timing Specification in HS400 mode

8.7.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.
Figure 22 and Table 30show Device input timing.

Figure 22: HS400 Device Data input timing

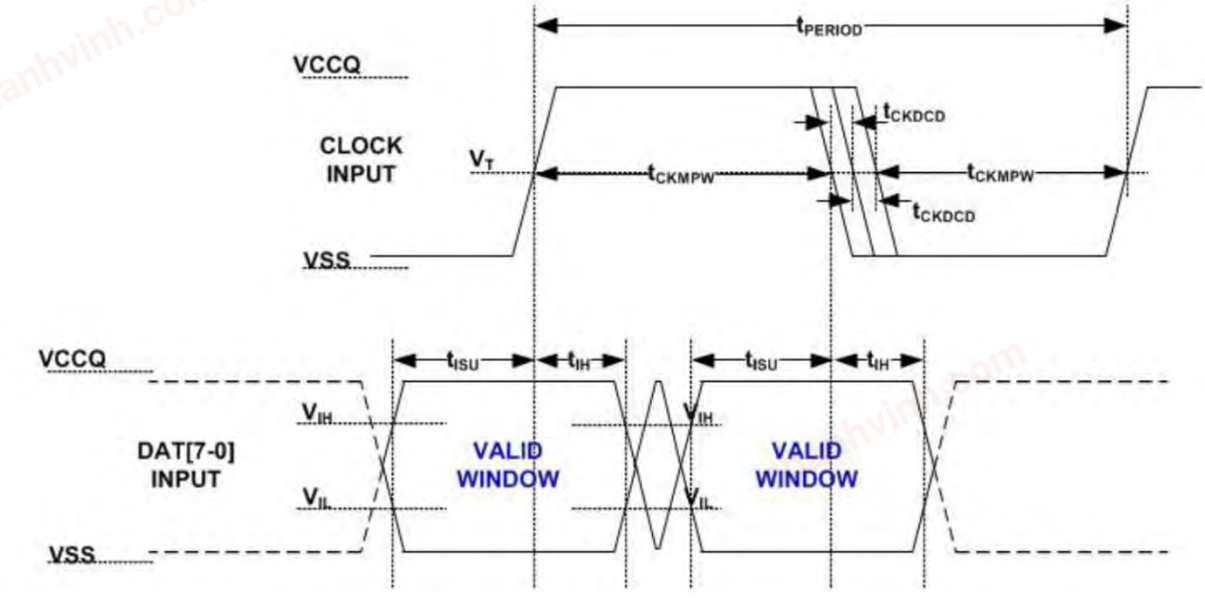


Table 30: HS400 Device input timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges with respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. Includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT.
Input DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Input hold time	tIHddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.

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8.7.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

Figure 23: HS400 Device output timing

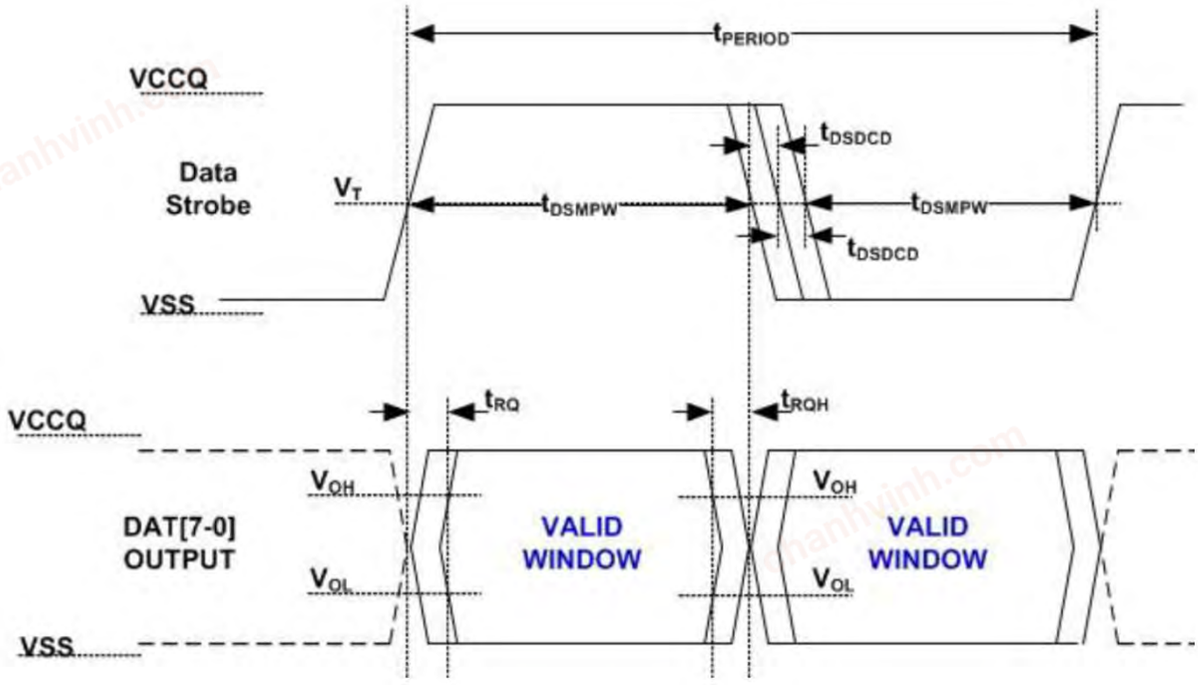


Table 31 HS400 Device Output timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to VT
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	tRQ		0.4	ns	With respect to VOH/VOL and HS400 reference load
Output hold skew	tRQH		0.4	ns	With respect to VOH/VOL and HS400 reference load.
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load

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Table 32: HS400 Capacitance and Resistors

Parameter	Symbol	Min.	Type	Max.	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7		100	kOhm	
Pull-up resistance for DAT0-7	RDAT	10		100	kOhm	
Pull-down resistance for Data Strobe	RDS	10		100	kOhm	
Internal pull up resistance DAT1-DAT7	Rint	10		150	kOhm	
Single Device capacitance	CDevice			6	pF	

9. e·MMC Registers

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

Table 33: e·MMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional, not implemented
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

9.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table 34: OCR register

OCR bit	V_{CCQ} voltage window	typ. value
[6:0]	Reserved	000 0000b
[7]	1.70 – 1.95V	1b
[14:8]	2.0 – 2.6V	000 0000b
[23:15]	2.7 – 3.6V	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b (sector mode, for devices >2GB)
[31]	Card power up status bit (0=busy; 1=ready)[1]	

Note 1: This bit is set to LOW if the Device has not finished the power up routine.

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9.1.1 Memory Addressing

Previous implementations of the e·MMC specification (versions up to v4.1) implemented byte addressing using a 32 bit field. This addressing mechanism permitted for e·MMC densities up to and including 2 GB.
To support larger densities the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.
To determine the addressing mode use the host should read bit [30:29] in the OCR register.

9.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (e·MMC protocol). For details, refer to section 7.2 of the JEDEC Standard JESD84-B51.

Table 35: CID register

Register Name	Bit Width	Description	typ. Value
MID	8	Manufacture ID	0x52
–	6	Reserved	000000
CBX	2	Device/BGA	01
OID	8	OEM/Application ID	0X52
PNM	48	Product Name 5GB	"AS005G"
		Product Name 10GB	"AS010G"
PRV	8	Product Revision	0x11
PSN	32	Product Serial Number	xxxxxxxx
MDT	8	Manufacture Date	xx
CRC	7	Check sum of CID contents	CRC7 chksum
–	1	Not used; always=1	1

9.3 CSD Register

The Device-Specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. For details, refer to section 7.3 of the JEDEC Standard JESD84-B51.

Table 36: CSD register

Register Name	Bits	Bit Width	Description	typ. Value
CSD_STRUCTURE	127:126	2	CSD structure	0x3
SPEC_VERS	125:122	4	System Specification version	0x4
–	121:120	2	Reserved	-
TAAC	119:112	8	Data read access-time 1	0x27
NSAC	111:104	8	Data read access-time 2 in CLK cycle (NSAC*100)	0x01
TRAN_SPEED	103:96	8	Max. bus clock frequency	0x32
CCC	95:84	12	Device command classes	0x0F5
READ_BL_LEN	83:80	4	Max. read data block length	0x9
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	0x0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0x0
READ_BLK_MISALIGN	77	1	Read block misalignment	0x0
DSR_IMP	76	1	DSR implemented	0x0
–	75:74	2	Reserved	-
C_SIZE	73:62	12	Device size	0x**FFF**

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Register Name	Bits	Bit Width	Description	typ. Value
VDD_R_CURR_MIN	61:59	3	Max read current @VDD min	0x7
VDD_R_CURR_MAX	58:56	3	Max read current @VDD max	0x7
VDD_W_CURR_MIN	55:53	3	Max write current @VDD min	0x7
VDD_W_CURR_MAX	52:50	3	Max write current @VDD max	0x7
C_SIZE_MULT	49:47	3	Device size multiplier	0x7
ERASE_GRP_SIZE	46:42	5	Erase group size	0x1F
ERASE_GRP_MULT	41:37	5	Erase group size multiplier	0x1F
WP_GRP_SIZE	36:32	5	Write protect group size	0x0F
WP_GRP_ENABLE	31	1	Write protect group enable	0x1
DEFAULT_ECC	30:29	2	Manufacturer default ECC	0x0
R2W_FACTOR	28:26	3	Write speed factor	0x2
WRITE_BL_LEN	25:22	4	Max. write data block length	0x9
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0x0
–	20:17	4	Reserved	–
CONTENT_PROT_APP	16	1	Content protection application	0x0
FILE_FORMAT_GRP	15	1	File format group	0x0
COPY	14	1	Copy flag (OTP)	0x1
PERM_WRITE_PROTECT	13	1	Permanent write protection	0x0
TMP_WRITE_PROTECT	12	1	Temporary write protection	0x0
FILE_FORMAT	11:10	2	File format	0x0
ECC	9:8	2	ECC code	0x0
CRC	7:1	7	Checksum of CSD contents	–
–	0	1	Always=1	0x1

9.4 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard JESD84-B51.

Table 37: Extended CSD Register

Register Name	Bytes	Byte Width	Description	typ. Value
Properties Segment				
–	511:506	6	Reserved	–
EXT_SECURITY_ERR	505	1	Extended Security Commands Error	0x00
S_CMD_SET	504	1	Supported Command Sets	0x01
HPI_FEATURES	503	1	HPI features	0x01
BKOPS_SUPPORT	502	1	Background operations support	0x01
MAX_PACKED_READS	501	1	Max packed read commands	0x20

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Register Name	Bytes	Byte Width	Description	typ. Value
MAX_PACKED_WRITES	500	1	Max packed write commands	0x20
DATA_TAG_SUPPORT	499	1	Data Tag Support	0x01
TAG_UNIT_SIZE	498	1	Tag Unit Size	0x00
TAG_RES_SIZE	497	1	Tag Resources Size	0x00
CONTEXT_CAPABILITIES	496	1	Context management capabilities	0x78
LARGE_UNIT_SIZE_M1	495	1	Large Unit size	0x01
EXT_SUPPORT	494	1	Extended partitions attribute support	0x03
SUPPORTED_MODES	493	1	Supported modes	0x01
FFU_FEATURES	492	1	FFU features	0x00
OPERATION_CODE_TIME_OUT	491	1	Operation codes timeout	0x17
FFU_ARG	490:487	4	FFU Argument	0xFFFAFFF0
BARRIER_SUPPORT	486	1	Barrier support	0x01
Reserved	485:309	177	Reserved	–
CMDQ_SUPPORT	308	1	CMD Queuing Support	0x01
CMDQ_DEPTH	307	1	CMD Queuing Depth	0x1F
Reserved	306	1	Reserved	–
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	305:302	4	Number of FW sectors correctly programmed	0x00000000
VENDOR_PROPRIETARY_HEALTH_REPORT	301	1	Alliance specific data revision index	0x02
	300:299	2	3D TLC Target erase count	0x0BB8
	298:297	2	3D TLC current average erase count	variable
	296:295	2	3D TLC current maximum erase count	variable
	294:291	4	pSLC Target erase count	0x00007530
	290:287	4	pSLC current average erase count	variable
	286:283	4	pSLC current maximum erase count	variable
	282:281	2	Spare block count total	variable
	280:279	2	Runtime bad block total	variable
	278:275	4	Power Cycle Counter	variable
	274:273	2	Uncorrectable ECC count (limited to 65536)	variable

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Register Name	Bytes	Byte Width	Description	typ. Value
	272:271	2	Vendor proprietary health report (not used)	–
	270	1	Device temperature °C (signed)	variable
DEVICE_LIFE_TIME_EST_TYP_B	269	1	Device life time estimation type B (3D TLC, not applicable)	0x01 (constant)
DEVICE_LIFE_TIME_EST_TYP_A	268	1	Device life time estimation type A (3D pSLC)	0x01 (fresh device)
PRE_EOL_INFO	267	1	Pre EOL information	0x01 (fresh device)
OPTIMAL_READ_SIZE	266	1	Optimal read size	0x40
OPTIMAL_WRITE_SIZE	265	1	Optimal write size	0x40
OPTIMAL_TRIM_UNIT_SIZE	264	1	Optimal trim unit size	0x07
DEVICE_VERSION	263:262	2	Device version	0x0005
FIRMWARE_VERSION	261:254	8	Firmware version	0x0000000000000010
PWR_CL_DDR_200_360	253	1	Power class for 200MHz, DDR at V_{CC}=3.6V	0x00
CACHE_SIZE	252:249	4	Cache size	0x00000400
GENERIC_CMD6_TIME	248	1	Generic CMD6 timeout	0x05
POWER_OFF_LONG_TIME	247	1	Power off notification(long) timeout	0x64
BKOPS_STATUS	246	1	Background operations status	0x00
CORRECTLY_PRG_SECTORS_NUM	245:242	4	Number of correctly programmed sectors	0x00000000
INI_TIMEOUT_AP	241	1	1st initialization time after partitioning	0x0A
CACHE_FLUSH_POLICY	240	1	Cache Flushing Policy	0x01
PWR_CL_DDR_52_360	239	1	Power class for 52MHz, DDR at 3.6V	0x00
PWR_CL_DDR_52_195	238	1	Power class for 52MHz, DDR at 1.95V	0x00
PWR_CL_200_360	237	1	Power class for 200MHz at 3.6V	0x00
PWR_CL_200_130	236	1	Power class for 200MHz, at 1.95V	0x00
MIN_PERF_DDR_W_8_52	235	1	Minimum Write Performance for 8bit at 52MHz in DDR mode	0x00
MIN_PERF_DDR_R_8_52	234	1	Minimum Read Performance for	0x00

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Register Name	Bytes	Byte Width	Description	typ. Value
			8bit at 52MHz in DDR mode	
–	233	1	Reserved	–
TRIM_MULT	232	1	TRIM Multiplier	0x02
SEC_FEATURE_SUPPORT	231	1	Secure Feature support	0x55
SEC_ERASE_MULT	230	1	Secure Erase Multiplier	0x19 (5GB) 0x19 (10GB)
SEC_TRIM_MULT	229	1	Secure TRIM Multiplier	0x0A
BOOT_INFO	228	1	Boot information	0x07
–	227	1	Reserved	–
BOOT_SIZE_MULT	226	1	Boot partition size	0xFC
ACC_SIZE	225	1	Access size	0x06
HC_ERASE_GRP_SIZE	224	1	High-capacity erase unit size	0x01
ERASE_TIMEOUT_MULT	223	1	High-capacity erase timeout	0x02
REL_WR_SEC_C	222	1	Reliable write sector count	0x10
HC_WP_GRP_SIZE	221	1	High-capacity write protect group size	0x10
S_C_VCC	220	1	Sleep current (VCC)	0x07
S_C_VCCQ	219	1	Sleep current (VCCQ)	0x07
PRODUCTION_STATE_AWARENESS_TIMEOUT	218	1	Production state awareness Timeout	0x17
S_A_TIMEOUT	217	1	Sleep/awake timeout	0x12
SLEEP_NOTIFICATION_TIME	216	1	Sleep Notification timeout	0x0C
SEC_COUNT	215:212	4	Sector Count	0x00998000 (5GB) 0x01334000 (10GB)
SECURE_WP_INFO	211	1	Secure Write Protect Information	0x01
MIN_PERF_W_8_52	210	1	Minimum Write Performance for 8bit at 52MHz	0x00
MIN_PERF_R_8_52	209	1	Minimum Read Performance for 8bit at 52MHz	0x00
MIN_PERF_W_8_26_4_52	208	1	Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	0x00
MIN_PERF_R_8_26_4_52	207	1	Minimum Read Performance for	0x00

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Register Name	Bytes	Byte Width	Description	typ. Value
			8bit at 26MHz, for 4bit at 52MHz	
MIN_PERF_W_4_26	206	1	Minimum Write Performance for 4bit at 26MHz	0x00
MIN_PERF_R_4_26	205	1	Minimum Read Performance for 4bit at 26MHz	0x00
–	204	1	Reserved	–
PWR_CL_26_360	203	1	Power class for 26MHz at 3.6V 1 R	0x00
PWR_CL_52_360	202	1	Power class for 52MHz at 3.6V 1 R	0x00
PWR_CL_26_195	201	1	Power class for 26MHz at 1.95V 1 R	0x00
PWR_CL_52_195	200	1	Power class for 52MHz at 1.95V 1 R	0x00
PARTITION_SWITCH_TIME	199	1	Partition switching timing	0x04
OUT_OF_INTERRUPT_TIME	198	1	Out-of-interrupt busy timing	0x0A
DRIVER_STRENGTH	197	1	I/O Driver Strength	0x1F
CARD_TYPE	196	1	Device type	0x57
–	195	1	Reserved	–
CSD_STRUCTURE	194	1	CSD structure	0x02
–	193	1	Reserved	–
EXT_CSD_REV	192	1	Extended CSD revision	0x08
Modes Segment				
CMD_SET	191	1	Command set	0x00
–	190	1	Reserved	–
CMD_SET_REV	189	1	Command set revision	0x00
–	188	1	Reserved	–
POWER_CLASS	187	1	Power class	0x00
–	186	1	Reserved	–
HS_TIMING	185	1	High-speed interface timing	0x01
STROBE_SUPPORT	184	1	Strobe Support	0x01
BUS_WIDTH	183	1	Bus width mode	0x01
–	182	1	Reserved	–
ERASED_MEM_CONT	181	1	Erased memory content	0x00
–	180	1	Reserved	–
PARTITION_CONFIG	179	1	Partition configuration	0x00
BOOT_CONFIG_PROT	178	1	Boot config protection	0x00
BOOT_BUS_CONDITIONS	177	1	Boot bus Conditions	0x00
–	176	1	Reserved	–

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Register Name	Bytes	Byte Width	Description	typ. Value
ERASE_GROUP_DEF	175	1	High-density erase group definition	0x01
BOOT_WP_STATUS	174	1	Boot write protection status registers	0x00
BOOT_WP	173	1	Boot area write protection register	0x00
–	172	1	Reserved	–
USER_WP	171	1	User area write protection register	0x00
–	170	1	Reserved	–
FW_CONFIG	169	1	FW configuration	0x00
RPMB_SIZE_MULT	168	1	RPMB Size	0x20
WR_REL_SET	167	1	Write reliability setting register	0x1F
WR_REL_PARAM	166	1	Write reliability parameter register	0x15
SANITIZE_START	165	1	Start Sanitize operation	0x00
BKOPS_START	164	1	Manually start background operations	0x00
BKOPS_EN	163	1	Enable background operations handshake	0x00
RST_n_FUNCTION	162	1	H/W reset function	0x00
HPI_MGMT	161	1	HPI management	0x00
PARTITIONING_SUPPORT	160	1	Partitioning Support	0x07
MAX_ENH_SIZE_MULT	159:157	3	Max Enhanced Area Size	0x000266 (5GB) 0x0004CD (10GB)
PARTITIONS_ATTRIBUTE	156	1	Partitions attribute	0x00
PARTITION_SETTING_COMPLETED	155	1	Partitioning Setting	0x00
GP_SIZE_MULT4	154:152	3	General Purpose Partition Size	0x000000
GP_SIZE_MULT3	151:149	3	General Purpose Partition Size	0x000000
GP_SIZE_MULT2	148:146	3	General Purpose Partition Size	0x000000
GP_SIZE_MULT1	145:143	3	General Purpose Partition Size	0x000000
ENH_SIZE_MULT	142:140	3	Enhanced User Data Area Size	0x000000
ENH_START_ADDR	139:136	4	Enhanced User Data Start Address	0x00000000
–	135	1	Reserved	–
SEC_BAD_BLK_MGMNT	134	1	Bad Block Management mode	0x00
PRODUCTION_STATE_AWARENESS	133	1	Production state awareness	0x00

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Register Name	Bytes	Byte Width	Description	typ. Value
TCASE_SUPPORT	132	1	Package Case Temperature is controlled	0x00
PERIODIC_WAKEUP	131	1	Periodic Wake-up	0x00
PROGRAM_CID_CSD_DDR_SUPPORT	130	1	Program CID/CSD in DDR mode support	0x00
–	129:128	2	Reserved	–
VENDOR_SPECIFIC_FIELD	127:64	64	Vendor Specific Fields (not used)	–
NATIVE_SECTOR_SIZE	63	1	Native sector size	0x01
USE_NATIVE_SECTOR	62	1	Sector size emulation	0x00
DATA_SECTOR_SIZE	61	1	Sector size	0x00
INI_TIMEOUT_EMU	60	1	1st initialization after disabling sector size emulation	0x0A
CLASS_6_CTRL	59	1	Class 6 commands control	0x00
DYNCAP_NEEDED	58	1	Number of addressed group to be Released	0x00
EXCEPTION_EVENTS_CTRL	57:56	2	Exception events control	0x0000
EXCEPTION_EVENTS_STATUS	55:54	2	Exception events status	0x0000
EXT_PARTITIONS_ATTRIBUTE	53:52	2	Extended Partitions Attribute	0x0000
CONTEXT_CONF	51:37	15	Context configuration	all 0x00
PACKED_COMMAND_STATUS	36	1	Packed command status	0x00
PACKED_FAILURE_INDEX	35	1	Packed command failure index	0x00
POWER_OFF_NOTIFICATION	34	1	Power Off Notification	0x00
CACHE_CTRL	33	1	Control to turn the Cache ON/OFF	0x00
FLUSH_CACHE	32	1	Flushing of the cache	0x00
BARRIER_CTRL	31	1	Control to turn the Barrier ON/OFF	0x00
MODE_CONFIG	30	1	Mode config	0x00
MODE_OPERATION_CODES	29	1	Mode operation codes	0x00
Reserved	28:27	2	Reserved	–
FFU_STATUS	26	1	FFU status	0x00
PRE_LOADING_DATA_SIZE	25:22	4	Per loading data size	0x00000000

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MAX_PRE_LOADING_DATA_SIZE	21:18	4	Max pre loading data size	0x00998000 (5GB) 0x01334000 (10GB)
PRODUCT_STATE_AWARENESS_ENABLEMENT	17	1	Product state awareness enablement	0x01
SECURE_REMOVAL_TYPE	16	1	Secure removal type	0x3B
CMDQ_MODE_EN	15	1	Command Queue Mode Enable	0x00
Reserved	14:0	15	Reserved	–
Note 1: Reserved bits should read as "0." Note 2: Obsolete values should be don't care.				

9.5 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7.

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10. Part number system

Table 38. Part number system

AS	FC	5G	3	1	P	3	-51	B	I	N	XX
Alliance Memory	eMMC Series (Flash + Controller)	Density 5G=5GB 10G=10GB	Flash Voltage 3=3.3V 1=1.8V	NAND Die 1=Single 2=Dual Die	NAND Type S = SLC M = MLC T = TLC P =pSLC	Generation Code Blank = rev0 A = revA B = revB (Change in controller or Flash will change Rev) 3 = TLC Gen3	eMMC Version 51 = 5.1	Package Type B = 153b FBGA (11.5x13mm)	Operating Temperature I = Industrial (-40°C~85°C)	ROHS Compliant	Packing Type None:Tray TR:Reel

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