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Revision History

2Gb AS4C128M16D2A - 84 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Dec 2015

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Features

- JEDEC Standard Compliant
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Power supplies: V_{DD} & V_{DDQ} = +1.8V ± 0.1V
- Operating temperature:
  - Commercial (0 ~ 85 °C)
  - Industrial (-40 ~ 95 °C)
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 400MHz
- Differential Clock, CK & CK#
- Bidirectional single/differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 4-bit prefetch architecture
- Internal pipeline architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Posted CAS# additive latency (AL): 0, 1, 2, 3, 4, 5
- WRITE latency = READ latency - 1 t_{CK}
- Burst lengths: 4 or 8
- Burst type: Sequential / Interleave
- DLL enable/disable
- Off-Chip Driver (OCD)
  - Impedance Adjustment
  - Adjustable data-output drive strength
- On-die termination (ODT)
- RoHS compliant
- Auto Refresh and Self Refresh
- 8192 refresh cycles / 64ms
  - Average refresh period
  7.8μs @ -40°C ≦TC≦ +85°C
  3.9μs @ +85°C ＜TC≦ +95°C
- Package: 84-ball 8 x 12.5 x 1.2mm (max) FBGA
  - Pb Free and Halogen Free

Overview

The 2Gb DDR2 is a high-speed CMOS Double-Data-Rate-Two (DDR2), synchronous dynamic random - access memory (SDRAM) containing 2048 Mbits in a 16-bit wide data I/Os. It is internally configured as a 8-bank DRAM, 8 banks x 16Mb addresses x 16 I/Os. The device is designed to comply with DDR2 DRAM key features such as posted CAS# with additive latency, Write latency = Read latency -1, Off-Chip Driver (OCD) impedance adjustment, and On Die Termination(ODT).

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS#) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in RAS #, CAS# multiplexing style. Accesses begin with the registration of a Bank Activate command, and then it is followed by a Read or Write command. Read and write accesses to the DDR2 SDRAM are 4 or 8-bit burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Operating the eight memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. A sequential and gapless data rate is possible depending on burst length, CAS latency, and speed grade of the device.

Table 1. Speed Grade Information

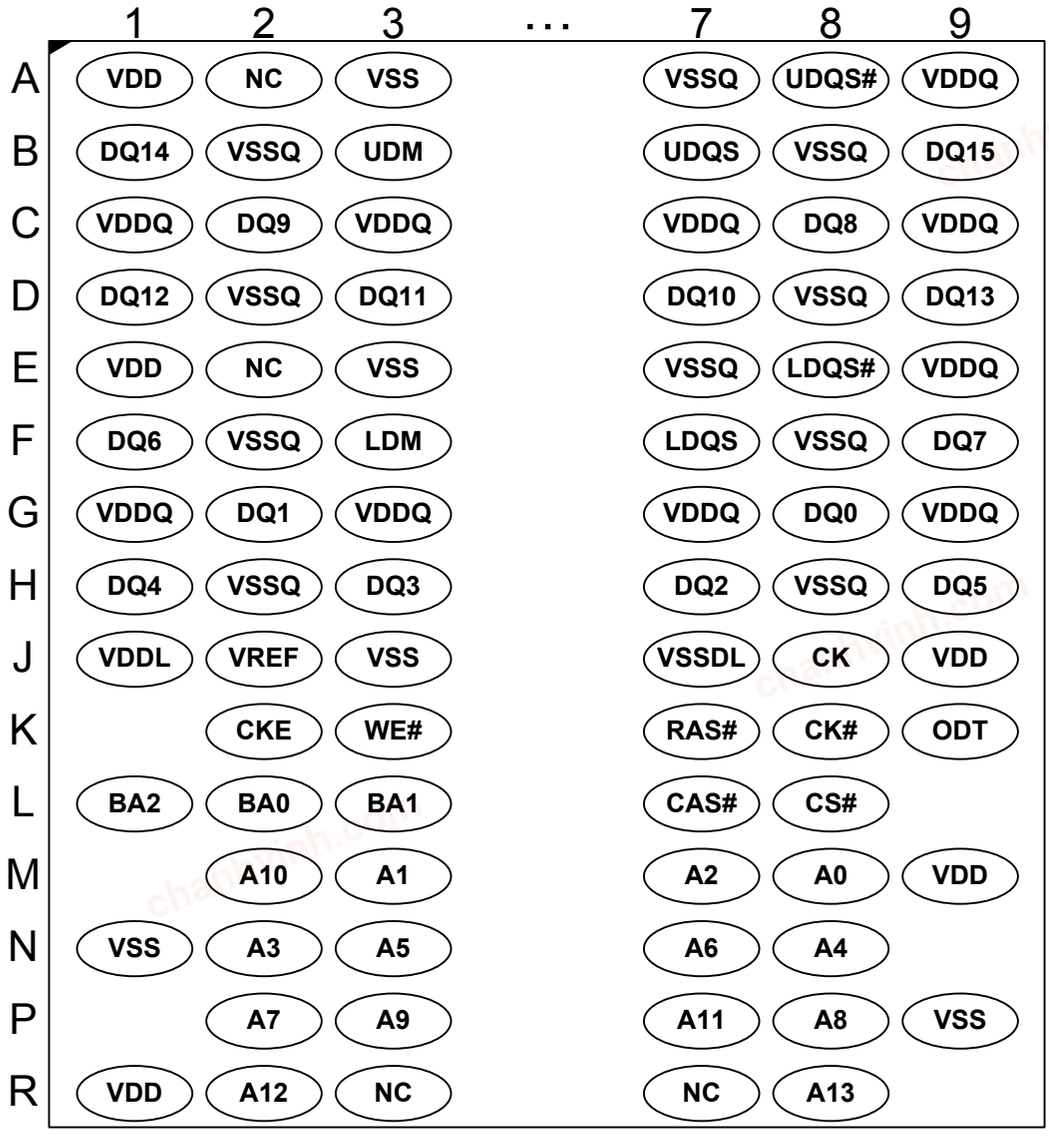
Speed Grade	Clock Frequency	CAS Latency	tRCD(ns)	tRP(ns)
DDR2-800	400MHz	5	12.5	12.5

Table 2. Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C128M16D2A-25BCN	128Mx 16	Commercial 0°C to 85°C	400	84-ball FBGA
AS4C128M16D2A-25BIN	128Mx 16	Industrial -40°C to 95°C	400	84-ball FBGA

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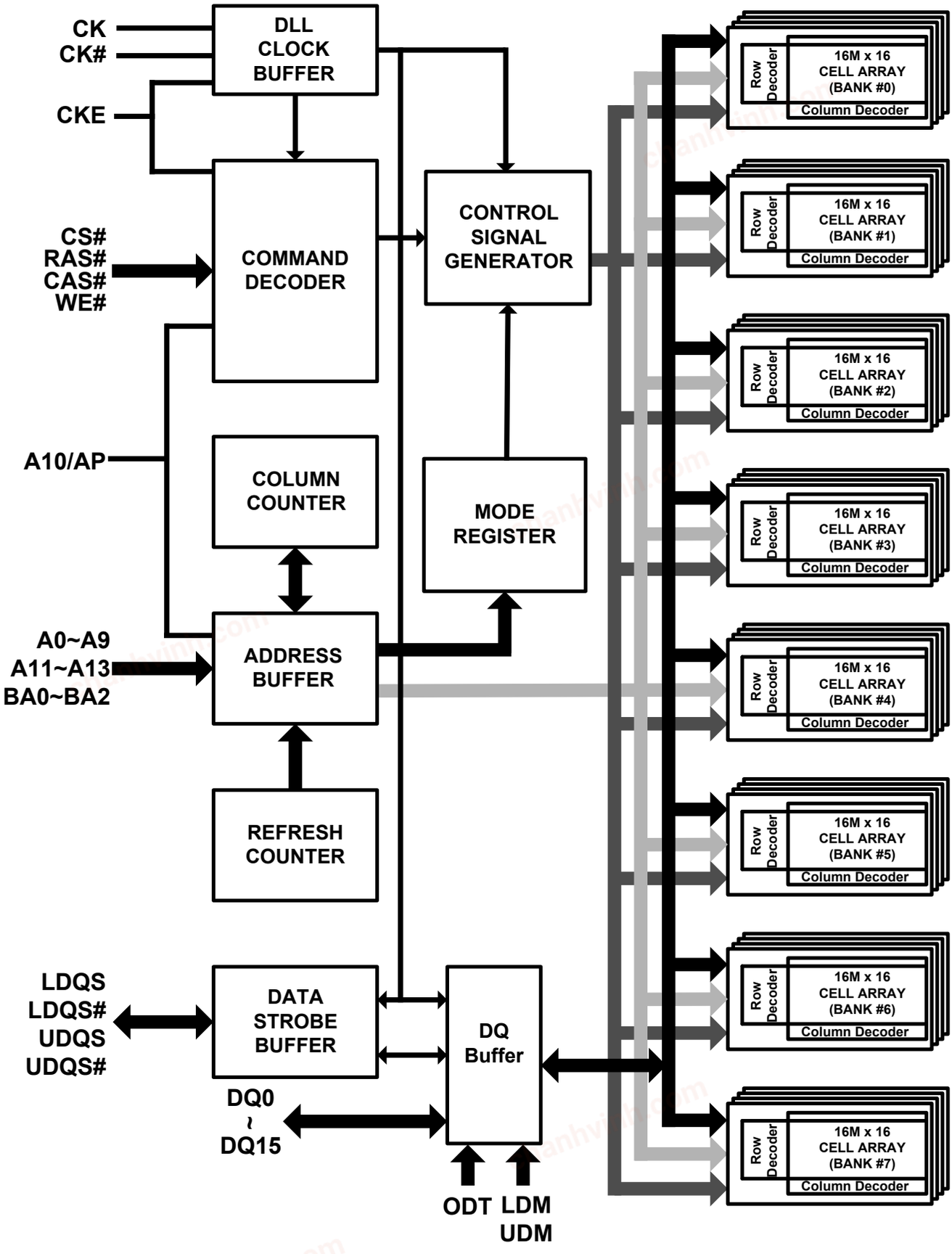
Figure 1. Ball Assignment (FBGA Top View)



	1	2	3	...	7	8	9
A	VDD	NC	VSS		VSSQ	UDQS#	VDDQ
B	DQ14	VSSQ	UDM		UDQS	VSSQ	DQ15
C	VDDQ	DQ9	VDDQ		VDDQ	DQ8	VDDQ
D	DQ12	VSSQ	DQ11		DQ10	VSSQ	DQ13
E	VDD	NC	VSS		VSSQ	LDQS#	VDDQ
F	DQ6	VSSQ	LDM		LDQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ		VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3		DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS		VSSDL	CK	VDD
K		CKE	WE#		RAS#	CK#	ODT
L	BA2	BA0	BA1		CAS#	CS#	
M		A10	A1		A2	A0	VDD
N	VSS	A3	A5		A6	A4	
P		A7	A9		A11	A8	VSS
R	VDD	A12	NC		NC	A13	

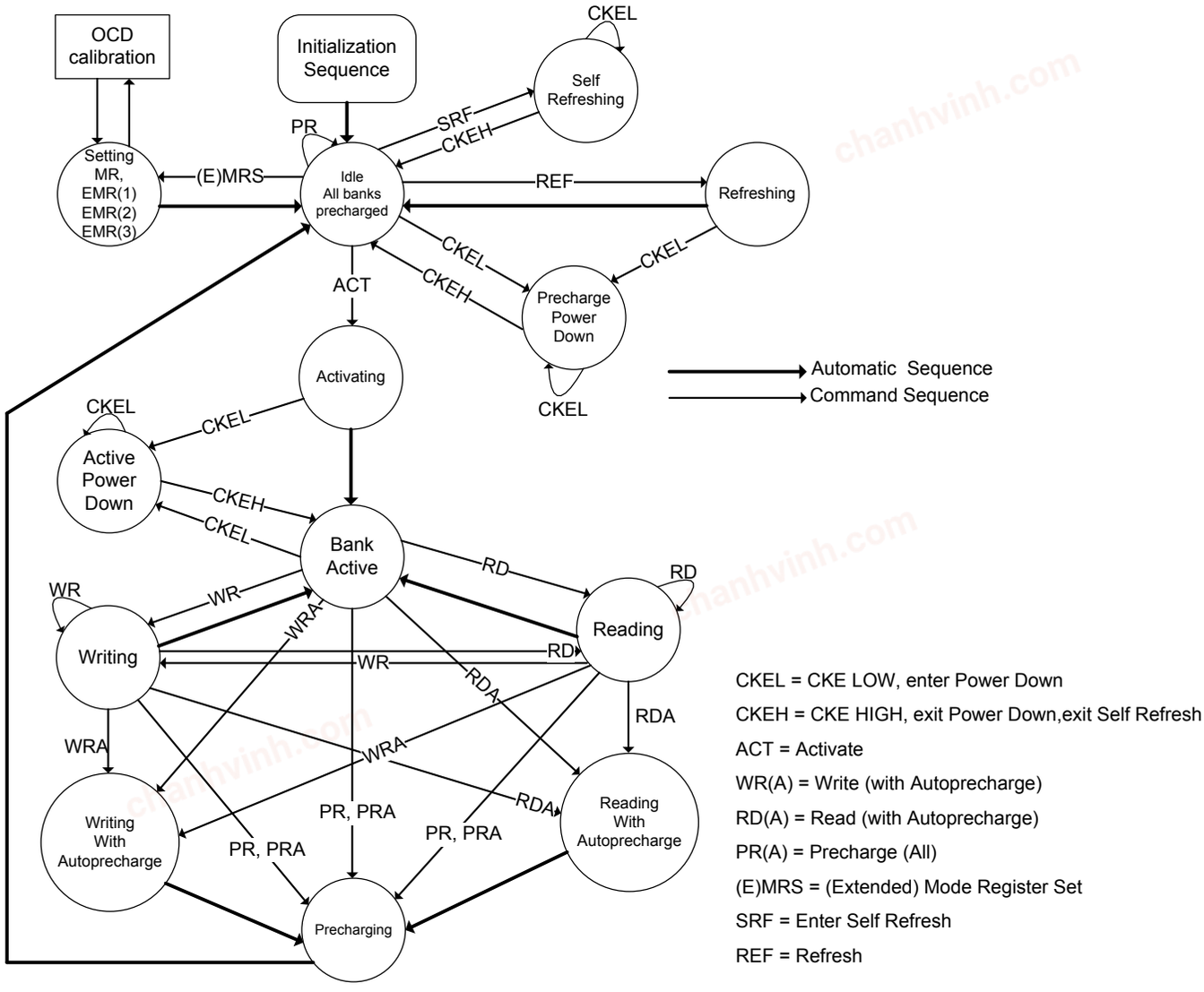
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Figure 2. Block Diagram



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Figure 3. State Diagram



Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit, timing restrictions during state transitions, among other things, are not captured in full detail.

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Ball Descriptions

Table 3. Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK, CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	**Bank Address:** BA0-BA2 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A13	Input	**Address Inputs:** A0-A13 are sampled during the BankActivate command (row address A0-A13) and Read/Write command (column address A0-A9 with A10 defining Auto Precharge).
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH" the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW" the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW" the column access is started by asserting CAS# "LOW". Then, the Read or Write command is selected by asserting WE# “HIGH" or “LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, LDQS# UDQS UDQS#	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15. The data strobes LDOS and UDQS may be used in single ended mode or paired with LDQS# and UDQS# to provide differential pair signaling to the system during both reads and writes.A control bit at EMR (1)[A10] enables or disables all complementary data strobe signals.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0 - DQ15	Input / Output	**Data I/O:** The DQ0-DQ15 input and output data are synchronized with the positive edges of CK and CK#. The I/Os are byte-maskable during Writes.
ODT	Input	**On Die Termination:** ODT enables internal termination resistance. It is applied to each DQ, LDQS/LDQS#, UDQS/UDQS#, LDM, and UDM signal. The ODT pin is ignored if the EMR (1) is programmed to disable ODT.

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V_{DD}	Supply	**Power Supply:** +1.8V ±0.1V
V_{SS}	Supply	**Ground**
V_{DDL}	Supply	**DLL Power Supply:** +1.8V ±0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DDQ}	Supply	**DQ Power:** +1.8V ±0.1V.
V_{SSQ}	Supply	**DQ Ground**
V_{REF}	Supply	**Reference Voltage for Inputs:** +0.5*V_{DDQ}
NC	-	**No Connect:** These pins should be left unconnected.

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Operation Mode

The following tables provide a quick reference of available DDR2 SDRAM commands, including CKE power-down modes and bank-to-bank commands.

Table 4. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}	CKE_n	DM	BA0-2	A10	A0-9, 11-13	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	H	X	V	Row address		L	L	H	H
Single Bank Precharge	Any	H	H	X	V	L	X	L	L	H	L
All Banks Precharge	Any	H	H	X	X	H	X	L	L	H	L
Write	Active(3)	H	H	X	V	L	Column address (A0 – A9)	L	H	L	L
Write with AutoPrecharge	Active(3)	H	H	X	V	H		L	H	L	L
Read	Active(3)	H	H	X	V	L	Column address (A0 – A9)	L	H	L	H
Read and Autoprecharge	Active(3)	H	H	X	V	H		L	H	L	H
(Extended) Mode Register Set	Idle	H	H	X	V	OP code		L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down Mode Entry	Idle	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down Mode Exit	Any	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X
Data Input Mask Enable(4)	Active	H	X	H	X	X	X	X	X	X	X

NOTE 1: V=Valid data, X=Don't Care, L=Low level, H=High level
NOTE 2: CKEn signal is input level when commands are provided.
CKEn-1 signal is input level one clock cycle before the commands are provided.
NOTE 3: These are states of bank designated by BA signal.
NOTE 4: LDM and UDM can be enabled respectively.

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Functional Description

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.
Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

● Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.
The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*V_{DDQ} and ODT [*1] at a low state (all other inputs may be undefined.) The V_{DD} voltage ramp time must be no greater than 200ms from when V_{DD} ramps from 300mV to V_{DD}min; and during the V_{DD} voltage ramp, $|V_{DD}-V_{DDQ}| \leqq 0.3V$
   - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output, AND
   - V_{TT} is limited to 0.95 V max, AND
   - V_{REF} tracks $V_{DDQ}/2$.

   or
   - Apply V_{DD} before or at the same time as V_{DDL}.
   - Apply V_{DDL} before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} before or at the same time as V_{TT} & V_{REF}.

   At least one of these two sets of conditions must be met.
2. Start clock and maintain stable condition.
3. For the minimum of 200μs after stable power and clock (CK, CK#), then apply NOP or deselect and take CKE HIGH.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS (2) command, provide “LOW” to BA0, “HIGH” to BA1.)
6. Issue EMRS (3) command. (To issue EMRS (3) command, provide “HIGH” to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "LOW" to A0, "HIGH" to BA0 and "LOW" to BA1.)
8. Issue a Mode Register Set command for “DLL reset”.
   (To issue DLL reset command, provide "HIGH" to A8 and "LOW" to BA0-1)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment).If OCD calibration is not used, EMRS OCD Default command (A9=A8=A7=HIGH) followed by EMRS OCD calibration Mode Exit command (A9=A8=A7=LOW) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

NOTE 1: To guarantee ODT off, V_{REF} must be valid and a LOW level must be applied to the ODT pin.

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Mode Register Set(MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, WR, and various vendor specific options to make DDR2 SDRAM useful for various applications.The default value of the mode register is not defined, therefore the mode register must be programmed during initialization for proper operation. The mode register is written by asserting LOW on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0 - A13. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register.The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all bank are in the precharge state.The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2, A1, A0): This field specifies the data length of column access and selects the Burst Length.
- Addressing Mode Select Field (A3): The Addressing Mode can be Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 4 and 8.
-CAS Latency Field (A6, A5, A4): This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field. t_{CAC}(min) □ CAS Latency X t_{CK}
- Test Mode field (A7); DLL Reset Mode field (A8): These two bits must be programmed to "00" in normal operation.
- (BA0, BA1): Bank addresses to define MRS selection.

Table 5. Mode Register Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
																	Address Field
0*2	0	0	0*2	PD	WR			DLL	TM	CAS Latency			BT	Burst Length			Mode Register

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit (use t_{XARD})
1	Slow exit (use t_{XARDS})

Write recovery for autoprecharge*1

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

BA1	BA0	MRS Mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

Note 1: For DDR2-800, WR min is determined by t_{CK} (avg) max and WR max is determined by t_{CK}(avg) min. WR [cycles] = RU {t_{WR}[ns]/t_{CK}(avg)[ns]}, where RU stands for round up. The mode register must be programmed to this value.This is also used with t_{RP} to determine t_{DAL}.

Note 2: BA2 and A13 are reserved for future use and must be set to 0 when programming the MR.

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● Extended Mode Register Set (EMRS)

EMR(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting LOW on CS#, RAS#, CAS#, WE#, BA1 and HIGH on BA0, while controlling the states of address pins A0 ~ A13. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength data-output driver. A3~A5 determine the additive latency, A2 and A6 are used for ODT value selection, A7~A9 are used for OCD control, A10 is used for DQS# disable.

- DLL Enable/Disable: The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.

Table 6. Extended Mode Register EMR (1) Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*3	0	1	0*3	Qoff	0*3	DQS#	OCD program			Rtt	Additive Latency			Rtt	D.I.C	DLL	Extended Mode Register

BA1	BA0	MRS mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

A6	A2	Rtt(NOMINAL)
0	0	ODT Disable
0	1	75Ω
1	0	150Ω
1	1	50Ω

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode*1
1	1	1	OCD Calibration default*2

A1	Output Driver Impedance Control
0	Full strength
1	Reduced strength

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff *3
0	Output buffer enabled
1	Output buffer disabled

A10	DQS#
0	Enable
1	Disable

NOTE 1: When Adjust mode is issued, AL from previously set value must be applied.

NOTE 2: After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000.

NOTE 3: Output disabled – DQs, DQSs, DQSs#.This feature is intended to be used during I_{DD} characterization of read current.

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EMR(2)

The extended mode register (2) controls refresh related features. The default value of the extended mode register (2) is not defined, therefore the extended mode register (2) must be written after power-up for proper operation. The extended mode register(2) is written by asserting LOW on CS#, RAS#, CAS#, WE#, HIGH on BA1 and LOW on BA0, while controlling the states of address pins A0 ~ A13. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register (2). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

Table 7. Extended Mode Register EMR(2) Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*1	1	0	0*1						SRF	0*1			DCC	PASR*3			Extended Mode Register(2)

A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable *2

BA1	BA0	MRS mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

A3	DCC Enable (Optional) *4
0	Disable
1	Enable

A2	A1	A0	Partial Array Self Refresh for 8 Banks (Optional)
0	0	0	Full array
0	0	1	Half Array (BA[2:0]=000,001,010&011)
0	1	0	Quarter Array (BA[2:0]= 000&001)
0	1	1	1/8 array (BA[2:0]=000)
1	0	0	3/4 array (BA[2:0]=010,011,100,101,110&111)
1	0	1	Half array (BA[2:0]= 100,101,110&111)
1	1	0	Quarter array (BA[2:0]= 110&111)
1	1	1	1/8 array (BA[2:0]=111)

NOTE 1: BA2 and A4-A6, A8-A13 is reserved for future use and must be set to 0 when programming the EMR(2).

NOTE 2: Due to the migration nature, user needs to ensure the DRAM part supports higher than 85∞C Tcase temperature self-refresh entry. If the high temperature self-refresh mode is supported then controller can set the EMRS2[A7] bit to enable the self-refresh rate in case of higher than 85∞C temperature self-refresh operation.

NOTE 3: If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified location will be lost if self refresh is entered. Data integrity will be maintained if t_{REF} conditions are met and no Self Refresh command is issued.

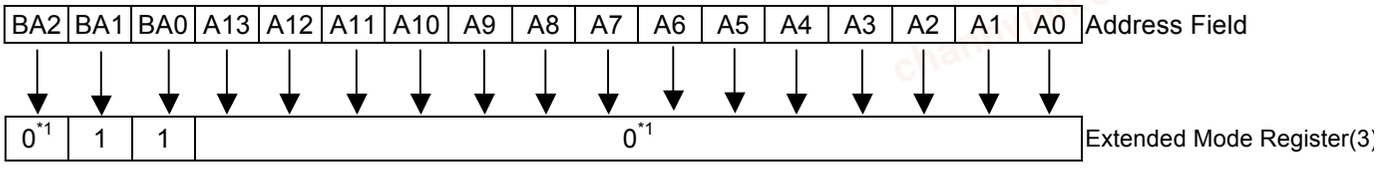
NOTE 4: DCC (Duty Cycle Corrector) implemented, user may be given the controllability of DCC thru EMR (2) [A3] bit.

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EMR(3)

No function is defined in extended mode register(3).The default value of the extended mode register(3) is not defined, therefore the extended mode register(3) must be programmed during initialization for proper operation.

Table 8. Extended Mode Register EMR (3) Bitmap



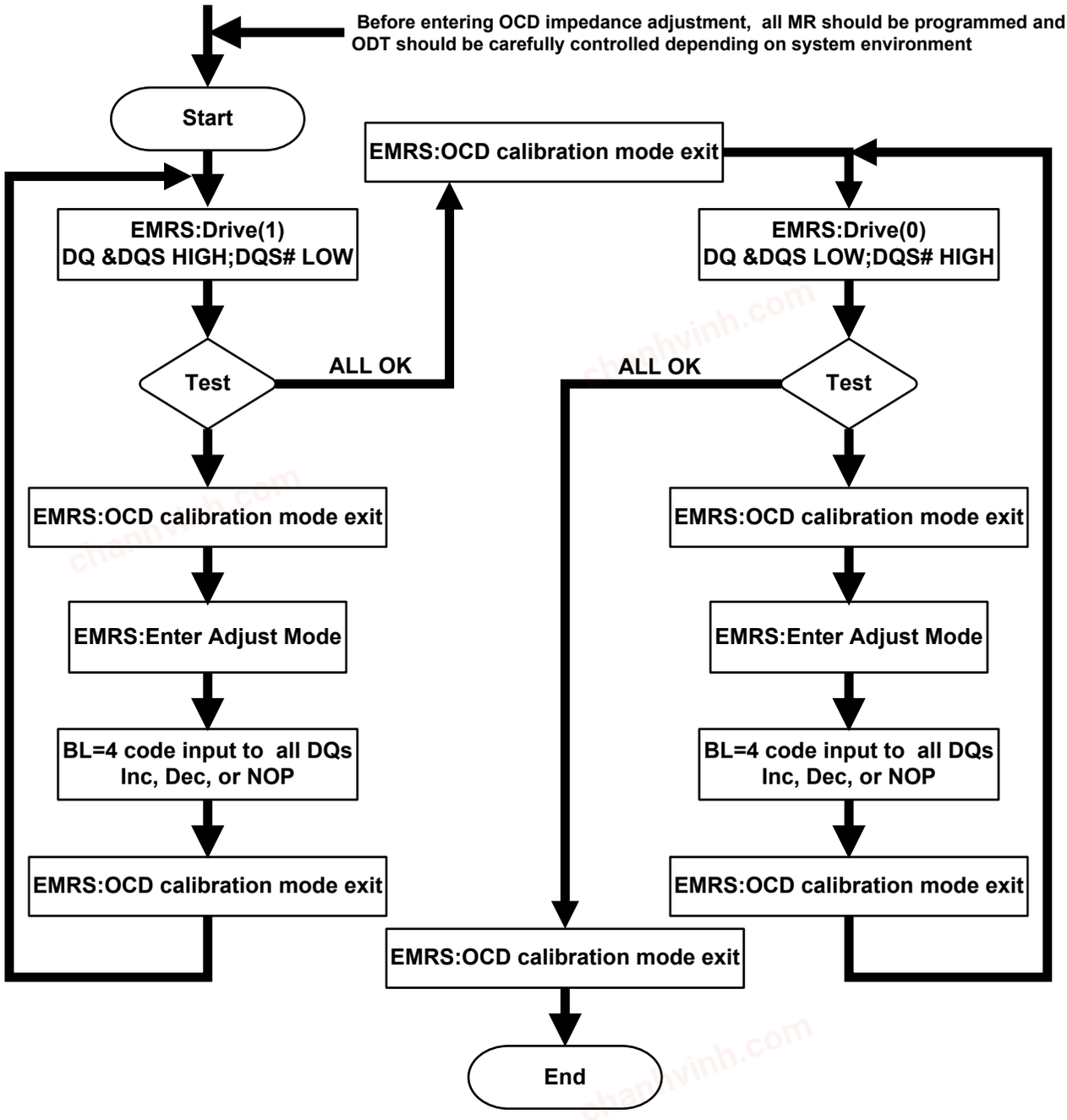
NOTE 1: All bits in EMR (3) except BA0 and BA1 are reserved for future use and must be set to 0 when programming the EMR (3).

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Off-chip drive (OCD) impedance adjustment

DDR2 SDRAM supports driver calibration feature and the following flow chart is an example of sequence.Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued.All MR should be programmed before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.

Figure 4. OCD impedance adjustment sequence



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- Extended mode register for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive (1) mode, all DQ, DQS signals are driven HIGH and all DQS# signals are driven LOW. In Drive (0) mode, all DQ, DQS signals are driven LOW and all DQS# signals are drive HIGH. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in the following table. OCD applies only to normal full strength output drive setting defined by EMRS and if half strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A7~A9 as '000' in order to maintain the default or calibrated value.

Table 9. OCD drive mode program

A9	A8	A7	operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, HIGH and DQS# LOW
0	1	0	Drive(0) DQ, DQS, LOW and DQS# HIGH
1	0	0	Adjust mode
1	1	1	OCD calibration default

- OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. D_{T0} in the following table means all DQ bits at bit time 0, D_{T1} at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting.

The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting maybe any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 10. OCD adjust mode program

4bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP	NOP
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

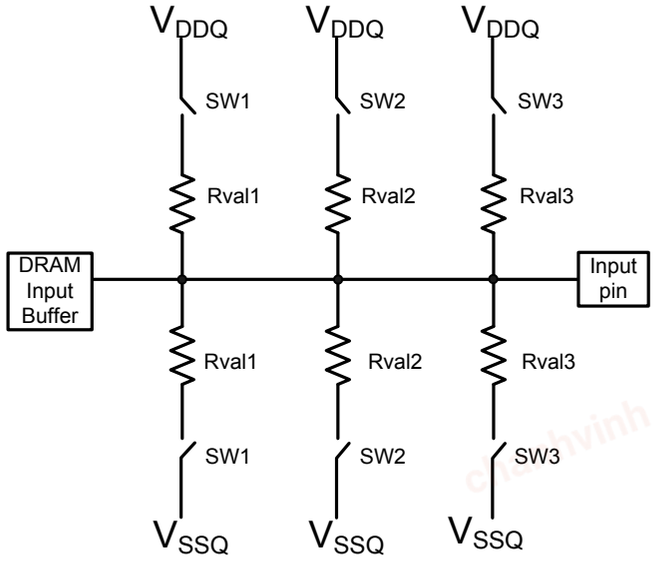
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● ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, UDQS/UDQS#, LDQS/LDQS#, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. It is turned off and not supported in SELF REFRESH mode.

Figure 5. Functional representation of ODT



Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2, and sw3 is determined by "Rtt (nominal)" in EMR.
Termination included on all DQs, DM, DQS, and DQS# pins

Table 11. ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Rtt effective impedance value for EMRS(A6,A2)=0,1;75Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,0;150Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,1;50Ω	Rtt3(eff)	40	50	60	Ω	1
Rtt mismatch tolerance between any pull-up/pull-down pair	Rtt(mis)	-6	-	6	%	2

NOTE 1: Measurement Definition for Rtt(eff): Apply V_{IH} (ac) and V_{IL} (ac) to test pin separately, then measure current I(V_{IH}(ac)) and I(V_{IL}(ac)) respectively.

$$Rtt(eff)=\frac{V_{IH}(ac)-V_{IL}(ac)}{I(V_{IH}(ac))-I(V_{IL}(ac))}$$

NOTE 2: Measurement Definition for Rtt (mis): Measure voltage (VM) at test pin (midpoint) with no load.

$$Rtt(mis)=\left(\frac{2xVM}{V_{DDQ}}-1\right)\times 100\%$$

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Bank activate command

The Bank Activate command is issued by holding CAS# and WE# HIGH with CS# and RAS# LOW at the rising edge of the clock. The bank addresses BA0-BA2 are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the t_{RCD}min specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure t_{RCD}min is satisfied. Additive latencies of 0, 1, 2, 3, and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (t_{RC}). The minimum time interval between Bank Active commands is t_{RRD}

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

- 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW}[ns] by t_{CK}[ns] or t_{CK}[ns], depending on the speed bin, and rounding up to next integer value. As an example of the rolling window, if RU{ (t_{FAW} / t_{CK}) } or RU{ (t_{FAW} / t_{CK})} is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9.
- 8 bank device Precharge All Allowance : t_{RP} for a Precharge All command for an 8 Bank device will equal to t_{RP} + 1 x t_{CK} or t_{RP} + 1 x t_{CK}, depending on the speed bin, where t_{RP} = RU{ t_{RP} / t_{CK}} and t_{RP} is the value for a single bank precharge.

Read and Write access modes

After a bank has been activated, a Read or Write cycle can be executed. This is accomplished by setting RAS# HIGH, CS# and CAS# LOW at the clock's rising edge. WE# must also be defined at this time to determine whether the access cycle is a Read operation (WE# HIGH) or a Write operation (WE# LOW). The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial Read or Write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. Any system or application incorporating random access memory products should be properly designed, tested, and qualified to ensure proper use or access of such memory products. Disproportionate, excessive, and/or repeated access to a particular address or addresses may result in reduction of product life.

Posted CAS#

Posted CAS# operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a CAS# Read or Write command to be issued immediately after the RAS bank activate command (or any time during the RAS# -CAS#-delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the t_{RCD}min, then AL (greater than 0) must be written into the EMR(1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section)

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst Read or Write operations are supported. Interruption of a burst Read or Write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a Read or Write burst when burst length = 8 is used, see the "Burst Interruption" section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

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Table 12. Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Burst read command

The Burst Read command is initiated by having CS# and CAS# LOW while holding RAS# and WE# HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the Read Latency (RL). The data strobe output (DQS) is driven LOW 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus CAS Latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1) (EMRS (1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS#. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS#, must be tied externally to V_{SS} through a 20 Ω to 10 KΩresistor to insure proper operation.

Burst write operation

The Burst Write command is initiated by having CS#, CAS# and WE# LOW while holding RAS# HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a Read latency (RL) minus one and is equal to (AL + CL -1);and is the number of clocks of delay that are required from the time the Write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles.

The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst Write to bank precharge is the write recovery time (WR). DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent.

In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at the specified AC/DC levels. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS#. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS#, must be tied externally to V_{SS} through a 20Ω to 10KΩ resistor to insure proper operation.

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Write data mask

One Write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, Consistent with the implementation on DDR SDRAMs. It has identical timings on Write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles.

Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when CS#, RAS# and WE# are LOW and CAS# is HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA2, BA1, and BA0 are used to define which bank to precharge when the command is issued.

Table 13. Bank Selection for Precharge by address bits

A10	BA2	BA1	BA0	Precharged Bank(s)
LOW	LOW	LOW	LOW	Bank 0 only
LOW	LOW	LOW	HIGH	Bank 1 only
LOW	LOW	HIGH	LOW	Bank 2 only
LOW	LOW	HIGH	HIGH	Bank 3 only
LOW	HIGH	LOW	LOW	Bank 4 only
LOW	HIGH	LOW	HIGH	Bank 5 only
LOW	HIGH	HIGH	LOW	Bank 6 only
LOW	HIGH	HIGH	HIGH	Bank 7 only
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	ALL Banks

Burst read operation followed by precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 + max (RTP, 2) - 2 clocks. For the earliest possible precharge, the precharge command may be issued on the rising edge which "Additive latency (AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS# precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called t_{RTP} (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

Burst Write operation followed by precharge

Minimum Write to Precharge command spacing to the same bank = WL + BL/2 + t_{WR}. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. t_{WR} is an analog timing parameter and is not the programmed value for t_{WR} in the MRS.

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Auto precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the CAS# timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is LOW when the READ or WRITE Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is HIGH when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst. Auto-precharge also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst Read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS# lockout circuit internally delays the Precharge operation until the array restore operation has been completed (t_{RAS} satisfied) so that the auto precharge command may be issued with any Read or Write command.

Burst read with auto precharge

If A10 is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if t_{RAS}(min) and t_{RTP} are satisfied. If t_{RAS}(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RAS}(min) is satisfied. If t_{RTP}(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until t_{RTP}(min) is satisfied.
In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + t_{RTP} + t_{RP}. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + t_{RTP} + t_{RP}. Note that both parameters t_{RTP} and t_{RP} have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.
A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

(1) The RAS# precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.
(2) The RAS# cycle time (t_{RC}) from the previous bank activation has been satisfied.

Burst write with auto precharge

If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus Write recovery time (t_{WR}). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The data-in to bank activate delay time (WR + t_{RP}) has been satisfied.
(2) The RAS# cycle time (t_{RC}) from the previous bank activation has been satisfied.

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Table 14. Precharge & Auto Precharge Clariification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Note
Read	Precharge (to same Bank as Read)	AL+BL/2+max(RTP,2)-2	t_{CK}	1,2
	Precharge All	AL+BL/2+max(RTP,2)-2		
Read w/AP	Precharge (to same Bank as Read w/AP)	AL+BL/2+max(RTP,2)-2	t_{CK}	1,2
	Precharge All	AL+BL/2+max(RTP,2)-2		
Write	Precharge (to same Bank as Write)	WL+BL/2+t_{WR}	t_{CK}	2
	Precharge All	WL+BL/2+t_{WR}		
Write w/AP	Precharge (to same Bank as Write w/AP)	WL+BL/2+t_{WR}	t_{CK}	2
	Precharge All	WL+BL/2+t_{WR}		
Precharge	Precharge (to same Bank as Precharge)	1	t_{CK}	2
	Precharge All	1		
Precharge All	Precharge	1	t_{CK}	2
	Precharge All	1		

NOTE 1: RTP [cycles] =RU {t_{RTP} [ns]/t_{CK} (avg) [ns]}, where RU stands for round up.
NOTE 2: For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank.The prechrage period is satisfied after t_{RP} or t_{RP}all(=t_{RP} for 8 bank device + 1X t_{CK}) depending on the latest precharge command issued to that bank.

● Refresh command

When CS#, RAS# and CAS# are held LOW and WE# HIGH at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (t_{RFC}).To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * t_{REFI}.

● Self refresh operation

The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CS#, RAS#, CAS# and CKE# held LOW with WE# HIGH at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using EMRS command. Once the Command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are "don't care". For proper Self Refresh operation all power supply pins (V_{DD}, V_{DDQ}, V_{DDL} and V_{REF}) must be at valid levels. The DRAM initiates a minimum of one refresh command internally within t_{CKE} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is t_{CKE}. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSNR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSRD} for proper operation except for Self Refresh re-entry. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least t_{XSNR} period and issuing one refresh command(refresh period of t_{RFC}). NOP or Deselect commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSNR}. ODT should be turned off during t_{XSRD}. The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

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Power-Down

Power-down is synchronously entered when CKE is registered LOW along with NOP or Deselect command. No read or write operation may be in progress when CKE goes LOW. These operations are any of the following: read burst or write burst and recovery. CKE is allowed to go LOW while any of other operations such as row activation, precharge or autoprecharge, mode register or extended mode register command time, or autorefresh is in progress.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as Precharge Power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as Active Power-down. For Active Power-down two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to “LOW” this mode is referred as “standard active power-down mode” and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to “HIGH” this mode is referred as a power saving “LOW power active power-down mode”. This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are “Don’t Care”. Power-down duration is limited by 9 times t_{REFI} of the device.

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD} or t_{XARDS}, after CKE goes HIGH. Power-down exit latencies are defined in the AC spec table of this data sheet.

Asynchronous CKE LOW Event

DRAM requires CKE to be maintained “HIGH” for all valid operations as defined in this datasheet. If CKE asynchronously drops “LOW” during any valid peration DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay efore turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “HIGH” again. DRAM must be fully re-initialized. DRAM is ready for normal operation after the initialization sequence.

Input clock frequency change during precharge power down

DDR2 SDRAM input clock frequency can be changed under following condition: DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

No operation command

The No Operation Command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation Command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when CS# is LOW with RAS#, CAS#, and WE# held HIGH at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when CS# is brought HIGH at the rising edge of the clock, the RAS#, CAS#, and WE# signals become don’t cares.

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Table 15. Absolute Maximum DC Ratings

Symbol	Parameter	Values	Unit	Note
V_{DD}	Voltage on VDD pin relative to Vss	-1.0 ~ 2.3	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to Vss	-0.5 ~ 2.3	V	1,3
V_{DDL}	Voltage on VDDL pin relative to Vss	-0.5 ~ 2.3	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.5 ~ 2.3	V	1,4
T_{STG}	Storage temperature	-55 ~ 100	∞C	1,2

NOTE1: Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
NOTE2: Storage temperature is the case temperature on the center/top side of the DRAM.
NOTE3: When V_{DD} and V_{DDQ} and V_{DDL} are less than 500mV, Vref may be equal to or less than 300mV.
NOTE4: Voltage on any input or I/O may not exceed voltage on V_{DDQ}.

Table 16. Operating Temperature Condition

Symbol	Parameter	Values	Unit	Note
T_{OPER}	Commercial temperature	0 ~ 85	°C	1,2
	Industrial temperature	-40 ~ 95	°C	1,2

NOTE1: Operating Temperature is the case surface temperature on the center/top side of the DRAM.
NOTE2: The operation temperature range are the temperature where all DRAM specification will be supported. Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operation specification may be required. During operation, the DRAM case temperature must be maintained between 0 - 85 °C under all other specification parameter. However, in some applications, it is desirable to operate the DRAM up to 95 °C case temperature. Therefore, two spec options may exist.
a) Supporting 0 - 85 °C with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options.
b) This is an optional feature and not required. Supporting 0 - 85 °C and being able to extend to 95 °C with doubling auto-refresh commands in frequency to a 32 ms period (tREFI = 3.9 us). Supporting higher temperature Self-Refresh entry via the control of EMSR (2) bit A7.

Table 17. Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Power supply voltage	1.7	1.8	1.9	V	1
V_{DDL}	Power supply voltage for DLL	1.7	1.8	1.9	V	5
V_{DDQ}	Power supply voltage for I/O Buffer	1.7	1.8	1.9	V	1,5
V_{REF}	Input reference voltage	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	mV	2,3
V_{TT}	Termination voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	4

NOTE1: There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.
NOTE2: The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
NOTE3: Peak to peak ac noise on V_{REF} may not exceed +/-2 % V_{REF} (dc).
NOTE4: V_{TT} of transmitting device must track V_{REF} of receiving device.
NOTE5: V_{DDQ} tracks with V_{DD}, V_{DDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

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Table 18. Input logic level

Symbol	Parameter	-25		Unit
		Min.	Max.	
V_{IH} (DC)	DC Input logic High Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V
V_{IL} (DC)	DC Input Low Voltage	-0.3	V_{REF} - 0.125	V
V_{IH} (AC)	AC Input High Voltage	V_{REF} + 0.2	V_{DDQ}+V_{peak}	V
V_{IL} (AC)	AC Input Low Voltage	Vss_Q –V_{peak}	V_{REF} – 0.2	V
V_{ID} (AC)	AC Differential Voltage	0.5	V_{DDQ}	V
V_{IX} (AC)	AC Differential crosspoint Voltage	0.5 x V_{DDQ}-0.175	0.5 x V_{DDQ}+0.175	V

NOTE1: Refer to Overshoot/undershoot specification for V_{peak} value: maximum peak amplitude allowed for overshoot and undershoot.

Table 19. AC Input test conditions

Symbol	Parameter	Value	Unit	Note
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1
$V_{SWING(max)}$	Input signal maximum peak to peak swing	1.0	V	1
Slew Rate	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE1: Input waveform timing is referenced to the input signal crossing through the V_{IH} /$_{IL}$ (ac) level applied to the device under test.

NOTE2: The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(ac) min for rising edges and the range from V_{REF} to V_{IL} (ac) max for falling edges .

NOTE3: AC timings are referenced with input waveforms switching from V_{IL} (ac) to V_{IH} (ac) on the positive transitions and V_{IH} (ac) to V_{IL} (ac) on the negative transitions.

Table 20. Differential AC output parameters

Symbol	Parameter	Value		Unit	Note
		Min.	Max.		
$V_{ox(ac)}$	AC Differential Cross Point Voltage	0.5xV_{DDQ}-0.125	0.5xV_{DDQ}+0.125	V	1

NOTE1: The typical value of V_{OX} (ac) is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{OX} (ac) is expected to track variations in V_{DDQ}. V_{OX} (ac) indicates the voltage at which differential output signals must cross.

Table 21. AC overshoot/undershoot specification for address and control pins (A0-A12, BA0-BA2, CS#, RAS#, CAS#, WE#, CKE, ODT)

Parameter	-25	Unit
Maximum peak amplitude allowed for overshoot area	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	V
Maximum overshoot area above V_{DD}	0.66	V-ns
Maximum undershoot area below V_{SS}	0.66	V-ns

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Table 22. AC overshoot/undershoot specification for clock, data, strobe, and mask pins (DQ, DQS, DQS#, DM, CK, CK#)

Parameter	-25	Unit
Maximum peak amplitude allowed for overshoot area	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	V
Maximum overshoot area above V_{DD}	0.23	V-ns
Maximum undershoot area below V_{SS}	0.23	V-ns

Table 23. Output AC test conditions

Symbol	Parameter	Value	Unit	Note
V_{OTR}	Output timing measurement reference level	$0.5xV_{DDQ}$	V	1

NOTE1: The V_{DDQ} of the device under test is referenced.

Table 24. Output DC current drive

Symbol	Parameter	SSTL_18	Unit	Note
I_{OH}(dc)	Output minimum source DC current	-13.4	mA	1, 3, 4
I_{OL}(dc)	Output minimum sink DC current	13.4	mA	2, 3, 4

NOTE1: V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ}) /I_{OH} must be less than 21 Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
NOTE2: V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 Ω for values of V_{OUT} between 0 V and 280 mV.
NOTE3: The dc value of V_{REF} applied to the receiving device is set to V_{TT}
NOTE4: The values of I_{OH} (dc) and I_{OL} (dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and VIL max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see JEDEC standard: Section 3.3 of JESD8-15A) along a 21 Ω load line to define a convenient driver current for measurement.

Table 25. Capacitance (V_{DD} = 1.8V, f = 1MHz, T_{OPER} = 25°C)

Symbol	Parameter	DDR2-800		Unit
		Min.	Max.	
C_{IN}	Input Capacitance : Command and Address	2.0	3.25	pF
C_{CK}	Input Capacitance (CK, CK#)	2.0	3.5	pF
$C_{I/O}$	DM, DQ, DQS Input/Output Capacitance	2.5	3.5	pF
DC_{IN}	Delta Input Capacitance: Command and Address	-	0.5	pF
DC_{CK}	Delta Input Capacitance: CK, CK#	-	0.5	pF
DC_{IO}	Delta Input/Output Capacitance: DM, DQ, DQS	-	0.5	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

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Table 26. IDD specification parameters and test conditions (V_{DD} = 1.8V ± 0.1V, T_{OPER} = -40~95 °C)

Parameter & Test Condition		Symbol	-25 Max.	Unit
Operating one bank active-precharge current: t_{CK} =t_{CK} (min), t_{RC} = t_{RC} (min), t_{RAS} = t_{RAS}(min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD0}	130	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (min), AL = 0; t_{CK} = t_{CK} (min),t_{RC} = t_{RC} (min), t_{RAS} = t_{RAS}(min), t_{RCD} = t_{RCD} (min);CKE is HIGH, CS# is HIGH between valid commands;Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	150	mA
Precharge power-down current: All banks idle;t_{CK} =t_{CK} (min); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		I_{DD2P}	16	mA
Precharge quiet standby current: All banks idle; t_{CK} =t_{CK} (min); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		I_{DD2Q}	70	mA
Precharge standby current: All banks idle; t_{CK} = t_{CK} (min); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD2N}	70	mA
Active power-down current: All banks open; t_{CK} =t_{CK} (min); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	MRS(A12)=0	I_{DD3P}	46	mA
	MRS(A12)=1		32	mA
Active standby current: All banks open; t_{CK} = t_{CK}(min), t_{RAS} = t_{RAS} (max), t_{RP} = t_{RP} (min); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD3N}	90	mA
Operating burst write current: All banks open,continuous burst writes; BL = 4, CL = CL (min), AL = 0; t_{CK}= t_{CK} (min), t_{RAS} = t_{RAS} (max), t_{RP} = t_{RP} (min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	180	mA
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (min), AL = 0; t_{CK} = t_{CK} (min), t_{RAS} = t_{RAS} (max), t_{RP} = t_{RP} (min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD4R}	180	mA
Burst refresh current: t_{CK} = t_{CK} (min); refresh command at every t_{RFC} (min) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD5}	290	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V;Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		I_{DD6}	12	mA
Operating bank interleave read current: All bank interleaving reads, I_{OUT}= 0mA; BL = 4, CL = CL (min), AL =t_{RCD} (min) - 1 x t_{CK} (min); t_{CK} = t_{CK} (min), t_{RC} = t_{RC} (min), t_{RRD} = t_{RRD} (min), t_{RCD} = t_{RCD} (min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs.Data pattern is same as IDD4R		I_{DD7}	330	mA

NOTE 1: IDD specifications are tested after the device is properly initialized.
NOTE 2: Input slew rate is specified by AC Parametric Test Condition.
NOTE 3: IDD parameters are specified with ODT disabled.
NOTE 4: Data bus consists of DQ, DM, LDQS, LDQS#, UDQS and UDQS#. IDD values must be met with all combinations of EMRS bits 10 and 11.
NOTE 5: LOW = VIN □ VILAC(max), HIGH = VIN □ VIHAC(min), STABLE = inputs stable at a HIGH or LOW level, FLOATING = inputs at VREF = VDDQ/2, SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

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Table 27. Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 1.8V ± 0.1V, T_{OPER} = -40~95 °C)

Symbol	Parameter		-25		Unit	Specific Notes
			Min.	Max.		
$t_{CK(avg)}$	Average clock period	CL=3	5	8	ns	15, 33, 34
		CL=4	3.75	8	ns	15, 33, 34
		CL=5	2.5	8	ns	15, 33, 34
		CL=6	2.5	8	ns	15, 33, 34
		CL=7	-	-	ns	15, 33, 34
$t_{CH(avg)}$	Average clock HIGH pulse width		0.48	0.52	t_{CK}	34, 35
$t_{CL(avg)}$	Average Clock LOW pulse width		0.48	0.52	t_{CK}	34, 35
WL	Write command to DQS associated clock edge		RL-1		t_{CK}	
t_{DQSS}	DQS latching rising transitions to associated clock edges		-0.25	0.25	t_{CK}	28
t_{DSS}	DQS falling edge to CK setup time		0.2	-	t_{CK}	28
t_{DSH}	DQS falling edge hold time from CK		0.2	-	t_{CK}	
t_{DQSH}	DQS input HIGH pulse width		0.35	-	t_{CK}	
t_{DQSL}	DQS input LOW pulse width		0.35	-	t_{CK}	
t_{WPRE}	Write preamble		0.35	-	t_{CK}	
t_{WPST}	Write postamble		0.4	0.6	t_{CK}	10
$t_{IS(base)}$	Address and Control input setup time		0.175	-	ns	5, 7, 9, 22, 27
$t_{IH(base)}$	Address and Control input hold time		0.25	-	ns	5, 7, 9, 23, 27
t_{IPW}	Control & Address input pulse width for each input		0.6	-	t_{CK}	
$t_{DS(base)}$	DQ & DM input setup time		0.05	-	ns	6-8, 20, 26, 29
$t_{DH(base)}$	DQ & DM input hold time		0.125	-	ns	6-8, 21, 26, 29
t_{DIPW}	DQ and DM input pulse width for each input		0.35	-	t_{CK}	
t_{AC}	DQ output access time from CK, CK#		-0.4	0.4	ns	38
t_{DQSCK}	DQS output access time from CK, CK#		-0.35	0.35	ns	38
t_{HZ}	Data-out high-impedance time from CK, CK#		-	$t_{AC(max)}$	ns	18, 38
$t_{LZ(DQS)}$	DQS(DQS#) low-impedance time from CK, CK#		$t_{AC(min)}$	$t_{AC(max)}$	ns	18, 38
$t_{LZ(DQ)}$	DQ low-impedance time from CK, CK#		$2t_{AC(min)}$	$t_{AC(max)}$	ns	18, 38
t_{DQSQ}	DQS-DQ skew for DQS and associated DQ signals		-	0.2	ns	13
t_{HP}	CK half pulse width		$_{min}(t_{CH}, t_{CL})$	-	ns	11, 12, 35
t_{QHS}	DQ hold skew factor		-	0.3	ns	12, 36
t_{QH}	DQ/DQS output hold time from DQS		t_{HP}- t_{QHS}	-	ns	37
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}	19, 39
t_{RPST}	Read postamble		0.4	0.6	t_{CK}	19, 40
t_{RRD}	Active to active command period		7.5	-	ns	4, 30
t_{FAW}	Four Activate Window		35	-	ns	4, 30
t_{CCD}	CAS# to CAS# command delay		2	-	t_{CK}	
t_{WR}	Write recovery time		15	-	ns	30
t_{DAL}	Auto Power write recovery + precharge time		WR + t_{RP}	-	ns	14, 31
t_{WTR}	Internal Write to Read Command Delay		7.5	-	ns	3, 24, 30
t_{RTP}	Internal read to precharge command delay		7.5	-	ns	3, 30
t_{CKE}	CKE minimum pulse width		3	-	t_{CK}	25

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t_{XSNR}	Exit self refresh to non-read command delay		t_{RFC} + 10	-	ns	30
t_{XSRD}	Exit self refresh to a read command		200	-	t_{CK}	
t_{XP}	Exit precharge power down to any command		2	-	t_{CK}	
t_{XARD}	Exit active power down to read command		2	-	t_{CK}	1
t_{XARDS}	Exit active power down to read command(slow exit, lower power)		8 - AL	-	t_{CK}	1, 2
t_{AOND}	ODT turn-on delay		2	2	t_{CK}	16
t_{AON}	ODT turn-on		$t_{AC(min)}$	$t_{AC(max)}$ + 0.7	ns	6, 16, 38
t_{AONPD}	ODT turn-on (Power-Down mode)		$t_{AC(min)}$ + 2	$2t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{AOFD}	ODT turn-off delay		2.5	2.5	t_{CK}	17, 42
t_{AOF}	ODT turn-off		$t_{AC(min)}$	$t_{AC(max)}$ + 0.6	ns	17, 41, 42
t_{AOFPD}	ODT turn-off (Power-Down mode)		$t_{AC(min)}$ + 2	2.5 t_{CK} + $t_{AC(max)}$ +1	ns	
t_{ANPD}	ODT to power down entry latency		3	-	t_{CK}	
t_{AXPD}	ODT power down exit latency		8	-	t_{CK}	
t_{MRD}	Mode register set command cycle time		2	-	t_{CK}	
t_{MOD}	MRS command to ODT update delay		0	12	ns	30
t_{OIT}	OCD drive mode output delay		0	12	ns	30
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops LOW		t_{IS}+ t_{CK} + t_{IH}	-	ns	15
t_{RFC}	Refresh to active/Refresh command time		195	-	ns	43
t_{REFI}	Average periodic refresh interval	@ -40∞C≦TC≦ +85∞C	-	7.8	µs	43
		@ +85∞C＜TC≦ +95∞C	-	3.9	µs	43
t_{RCD}	RAS# to CAS# Delay time		12.5	-	ns	
t_{RP}	Row precharge Delay time		12.5	-	ns	
t_{RC}	Row cycle Delay time		57.5	-	ns	
t_{RAS}	Row active Delay time		45	70K	ns	

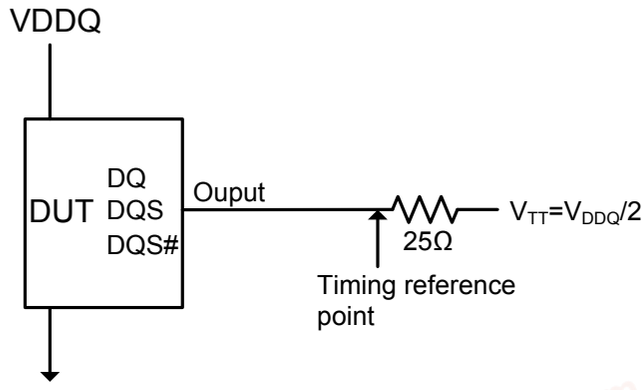
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General notes, which may apply for all AC parameters:

NOTE 1: DDR2 SDRAM AC timing reference load

The below figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester.

Figure 6. AC timing reference load



The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS#) signal.

NOTE 2: Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between V_{TT} - 250 mV and V_{TT} + 250 mV for single ended signals. For differential signals (e.g. DQS – DQS#) output slew rate is measured between DQS – DQS# = - 500 mV and DQS – DQS# = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

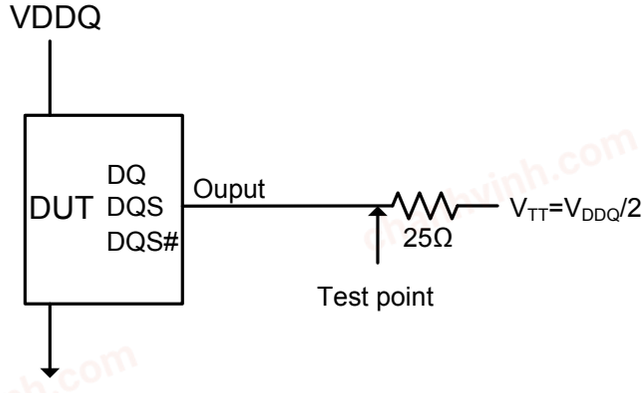
b) Input slew rate for single ended signals is measured from V_{REF} (dc) to V_{IH} (ac), min for rising edges and from V_{REF}(dc) to V_{IL}(ac),max for falling edges.For differential signals (e.g. CK – CK#) slew rate for rising edges is measured from CK – CK# = - 250 mV to CK -CK# = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) V_{ID} is the magnitude of the difference between the input voltage on CK and the input voltage on CK#, or between DQS and DQS# for differential strobe.

NOTE 3: DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as bellow

Figure 7. Slew rate test load



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NOTE 4: Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS#. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS#, must be tied externally to V_{SS} through a 20 Ω to 10 kΩ resistor to insure proper operation.

NOTE 5: AC timings are for linear signal transitions.

NOTE 6: All voltages are referenced to V_{SS}.

NOTE 7: These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

NOTE 8: Tests for AC timing, I_{DD}, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific notes for dedicated AC parameters

NOTE 1: User can choose which active power down exit timing to use via MRS (bit 12). t_{XARD} is expected to be used for fast active power down exit timing. t_{XARDS} is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

NOTE 2: AL = Additive Latency.

NOTE 3: This is a minimum requirement. Minimum read to precharge timing is AL+BL/2 provided that the t_{RTP} and t_{RAS} (min) have been satisfied.

NOTE 4: A minimum of two clocks (2* t_{CK}) is required irrespective of operating frequency.

NOTE 5: Timings are specified with command/address input slew rate of 1.0 V/ns.

NOTE 6: Timings are specified with DQs, DM, and DQS's (in single ended mode) input slew rate of 1.0V/ns.

NOTE 7: Timings are specified with CK/CK# differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode.

NOTE 8: Data setup and hold time derating.

For all input signals the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet. $t_{DS(base)}$ and $t_{DH(base)}$ value to the Δt_{DS} and Δt_{DH} derating value respectively.
Example: t_{DS} (total setup time) $= t_{DS\ (base)} + \Delta t_{DS}$.For slew rates in between the values listed in Tables 28, the derating values may obtained by linear interpolation.These values are typically not subject to production test. They are verified by design and characterization.

Table 28. DDR2-800 t_{DS}/t_{DH} derating with differential data strobe

tDS, tDH derating values for DDR2-800 (All units in 'ps'; the note applies to the entire table)																		
		DQS,DQS# Differential Slew Rate																
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH	ΔtDS	Δ tDH
DQ Slew Rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

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NOTE 9: t_{IS} and t_{IH} (input setup and hold) derating

For all input signals the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet $t_{IS(base)}$ and $t_{IH(base)}$ value to the Δt_{IS} and Δ_{tIH} derating value respectively.
Example: t_{IS} (total setup time) = t_{IS}(base) + Δt_{IS}
For slew rates in between the values listed in Tables 29, the derating values may obtained by linear interpolation.These values are typically not subject to production test. They are verified by design and characterization.

Table 29. Derating values for DDR2-800

tIS and tIH Derating Values for DDR2-800									
		CK,CK# Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		tIS	tIH	tIS	tIH	tIS	tIH	Units	Notes
Command/ Address Slew rate (V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

NOTE 10: The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

NOTE 11: MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

NOTE 12: t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (t_{CH}, t_{CL}). t_{QHS} accounts for:

1) The pulse duration distortion of on-chip clock circuits; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

NOTE 13: t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / DQS# and associated DQ in any given cycle.

NOTE 14: t_{DAL} = WR + RU{ t_{RP}[ns] / t_{CK}[ns] }, where RU stands for round up.WR refers to the t_{WR} parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period.

NOTE 15: The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down.

NOTE 16: ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted as 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

NOTE 17: ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-800, if t_{CK}(avg) = 2.5 ns is assumed, t_{AOFD} is 1.25 ns (= 0.5 x 2.5 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

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NOTE 18: t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}).

NOTE 19: t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). The actual voltage measurement points are not critical as long as the calculation is consistent.

NOTE 20: Input waveform timing t_{DS} with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the V_{IH}(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the V_{IL}(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS# signals must be monotonic between V_{IL}(dc)max and V_{IH}(dc)min.

NOTE 21: Input waveform timing t_{DH} with differential data strobe enabled MR[bit10]=0, is referenced from the differential data strobe crosspoint to the input signal crossing at the V_{IH}(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the V_{IL}(dc) level for a rising signal applied to the device under test. DQS, DQS# signals must be monotonic between V_{IL}(dc)max and V_{IH}(dc)min.

NOTE 22: Input waveform timing is referenced from the input signal crossing at the V_{IH}(ac) level for a rising signal and V_{IL}(ac) for a falling signal applied to the device under test.

NOTE 23: Input waveform timing is referenced from the input signal crossing at the V_{IL}(dc) level for a rising signal and V_{IH}(dc) for a falling signal applied to the device under test.

NOTE 24: t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

NOTE 25: t_{CKE}min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

NOTE 26: If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

NOTE 27: These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. t_{JIT}(per), t_{JIT}(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

NOTE 28: These parameters are measured from a data strobe signal (LDQS/UDQS) crossing to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. t_{JIT}(per), t_{JIT}(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

NOTE 29: These parameters are measured from a data signal ((L/U) DM, (L/U) DQ0, (L/U) DQ1, etc.) transition edge to its respective data strobe signal (LDQS/UDQS/LDQS#/UDQS#) crossing.

NOTE 30: For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / t_{CK}(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

NOTE 31: t_{DAL} [t_{CK}] = WR [t_{CK}] + tRP [t_{CK}] = WR + RU {t_{RP} [ps] / t_{CK}(avg) [ps] }, where WR is the value programmed in the mode register set.

NOTE 32: New units, 't_{CK}(avg)' is introduced in DDR2-800. Unit 't_{CK}(avg)' represents the actual t_{CK}(avg) of the input clock under operation.

NOTE 33: Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

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Table 30. Input clock jitter spec parameter

Parameter	Symbol	-25		Units	Notes
		Min.	Max.		
Clock period jitter	t_{JIT} (per)	-100	100	ps	33
Clock period jitter during DLL locking period	t_{JIT} (per,lck)	-80	80	ps	33
Cycle to cycle clock period jitter	t_{JIT} (cc)	-200	200	ps	33
Cycle to cycle clock period jitter during DLL locking period	t_{JIT} (cc,lck)	-160	160	ps	33
Cumulative error across 2 cycles	t_{ERR} (2per)	-150	150	ps	33
Cumulative error across 3 cycles	t_{ERR} (3per)	-175	175	ps	33
Cumulative error across 4 cycles	t_{ERR} (4per)	-200	200	ps	33
Cumulative error across 5 cycles	t_{ERR} (5per)	-200	200	ps	33
Cumulative error across n cycles, n=6...10, inclusive	t_{ERR} (6-10per)	-300	300	ps	33
Cumulative error across n cycles, n=11...50, inclusive	t_{ERR} (11-50per)	-450	450	ps	33
Duty cycle jitter	t_{JIT} (duty)	-100	100	ps	33

Definitions:

- t_{CK}(avg)

t_{CK}(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$t_{CK}(avg) = \left[\sum_{j=1}^{N} t_{CK_j}\right] / N \qquad \text{where N=200}$$

- t_{CH}(avg) and t_{CL}(avg)

t_{CH}(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$t_{CH}(avg) = \left[\sum_{j=1}^{N} t_{CH_j}\right] / \left(N \times t_{CK}(avg)\right) \qquad \text{where N=200}$$

t_{CL}(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$t_{CL}(avg) = \left[\sum_{j=1}^{N} t_{CL_j}\right] / \left(N \times t_{CK}(avg)\right) \qquad \text{where N=200}$$

t_{JIT} (duty) is defined as the cumulative set of t_{CH} jitter and t_{CL} jitter. t_{CH} jitter is the largest deviation of any single t_{CH} from t_{CH}(avg). t_{CL} jitter is the largest deviation of any single t_{CL} from t_{CL}(avg).

- t_{JIT}(duty) = Min/max of {t_{JIT}(CH), t_{JIT}(CL)}

  where,

  t_{JIT}(CH) = {t_{CHi}- t_{CH}(avg) where i=1 to 200}

  t_{JIT}(CL) = {t_{CLi}- t_{CL}(avg) where i=1 to 200}

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- t_{JIT}(per), t_{JIT}(per,lck)
  t_{JIT}(per) is defined as the largest deviation of any single tCK from t_{CK}(avg).
  t_{JIT}(per) = Min/max of {t_{CKi}- t_{CK}(avg) where i=1 to 200}
  t_{JIT}(per) defines the single period jitter when the DLL is already locked.
  t_{JIT}(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
  t_{JIT}(per) and $_{tJIT}$(per,lck) are not guaranteed through final production testing.

- t_{JIT}(cc), t_{JIT}(cc,lck)
  t_{JIT}(cc) is defined as the difference in clock period between two consecutive clock cycles:
  t_{JIT}(cc) = Max of $|t_{CKi+1} - t_{CKi}|$
  t_{JIT}(cc) defines the cycle to cycle jitter when the DLL is already locked.
  t_{JIT}(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
  t_{JIT}(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

- t_{ERR}(2per), t_{ERR} (3per), t_{ERR} (4per), t_{ERR} (5per), t_{ERR} (6-10per) and t_{ERR} (11-50per)
  t_{ERR} is defined as the cumulative error across multiple consecutive cycles from t_{CK}(avg).

$$t_{ERR}(nper) = \left[\sum_{j=1}^{i+N-1} t_{CK_j}\right] - \left(N \times t_{CK}(avg)\right) \quad \text{where} \begin{cases} n=2 & \text{for } t_{ERR}(2per) \\ n=3 & \text{for } t_{ERR}(3per) \\ n=4 & \text{for } t_{ERR}(4per) \\ n=5 & \text{for } t_{ERR}(5per) \\ 6 \le n \le 10 & \text{for } t_{ERR}(6-10per) \\ 11 \le n \le 50 & \text{for } t_{ERR}(11-50per) \end{cases}$$

NOTE 34: These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min andmax of SPEC values are to be used for calculations in the table below.)

Table 31. Absolute clock period average values

Parameter	Symbol	Min.	Max.	Units
Absolute clock period	t_{CK} (abs)	t_{CK}(avg),min + t_{JIT}(per),min	t_{CK}(avg),max + t_{JIT}(per),max	ps
Absolute clock HIGH pulse width	t_{CH} (abs)	t_{CH}(avg),min * t_{CK}(avg),min + t_{JIT}(duty),min	t_{CH}(avg),max * t_{CK}(avg),max + t_{JIT}(duty),max	ps
Absolute clock LOW pulse width	t_{CL} (abs)	t_{CL}(avg),min * t_{CK}(avg),min + t_{JIT}(duty),min	t_{CL}(avg), max * t_{CK}(avg),max + t_{JIT}(duty), max	ps

NOTE 35: t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for tQH calculation is determined by the following equation;

t_{HP} = Min (t_{CH}(abs), t_{CL}(abs)),

where,

t_{CH}(abs) is the minimum of the actual instantaneous clock HIGH time;

t_{CL}(abs) is the minimum of the actual instantaneous clock LOW time;

NOTE 36: t_{QHS} accounts for:

1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

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NOTE 37: $t_{QH} = t_{HP} – t_{QHS}$, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.}

NOTE 38: When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{ERR}(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

NOTE 39: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

NOTE 40: When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{JIT}(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

NOTE 41: When the device is operated with input clock jitter, this parameter needs to be derated by { - t_{JIT}(duty),max - t_{ERR}(6-10per),max } and { - t_{JIT}(duty),min - t_{ERR}(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.)

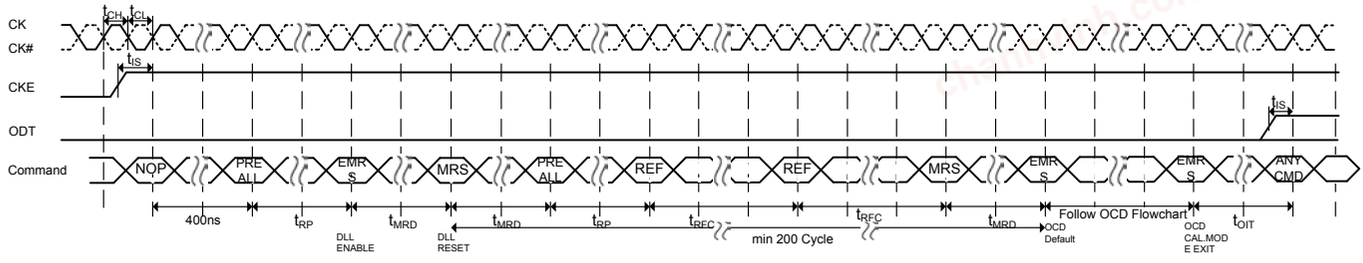
NOTE 42: For t_{AOFD} of DDR2-800, the 1/2 clock of t_{CK} in the 2.5 x t_{CK} assumes a t_{CH}(avg), average input clock HIGH pulse width of 0.5 relative to t_{CK}(avg). t_{AOF},min and t_{AOF},max should each be derated by the same amount as the actual amount of t_{CH}(avg) offset present at the DRAM input with respect to 0.5.

NOTE 43: If refresh timing is violated, data corruption may occur and the data must be re-writtern with valid data before a valid READ can be executed.

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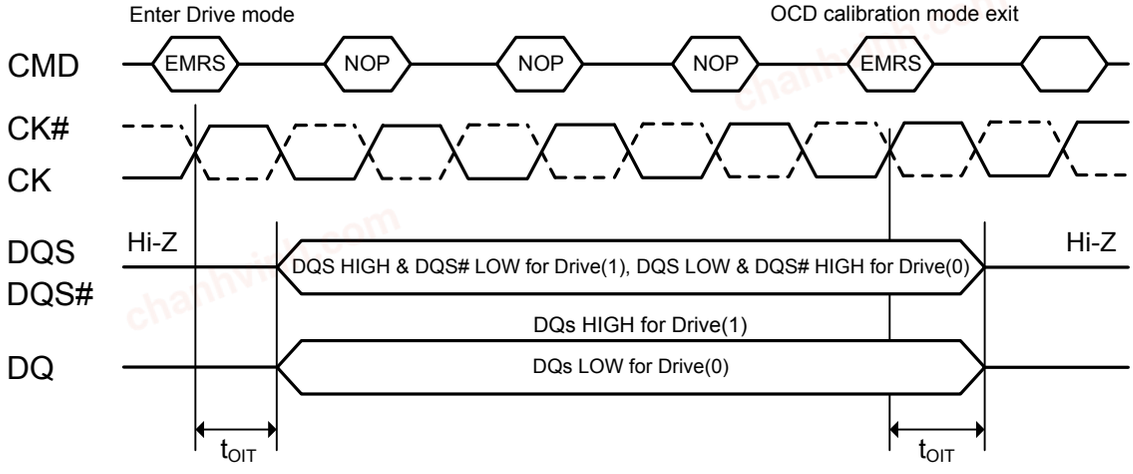
Timing Waveforms

Figure 8. Initialization sequence after power-up



NOTE 1: To guarantee ODT off, V_{REF} must be valid and a LOW level must be applied to the ODT pin.

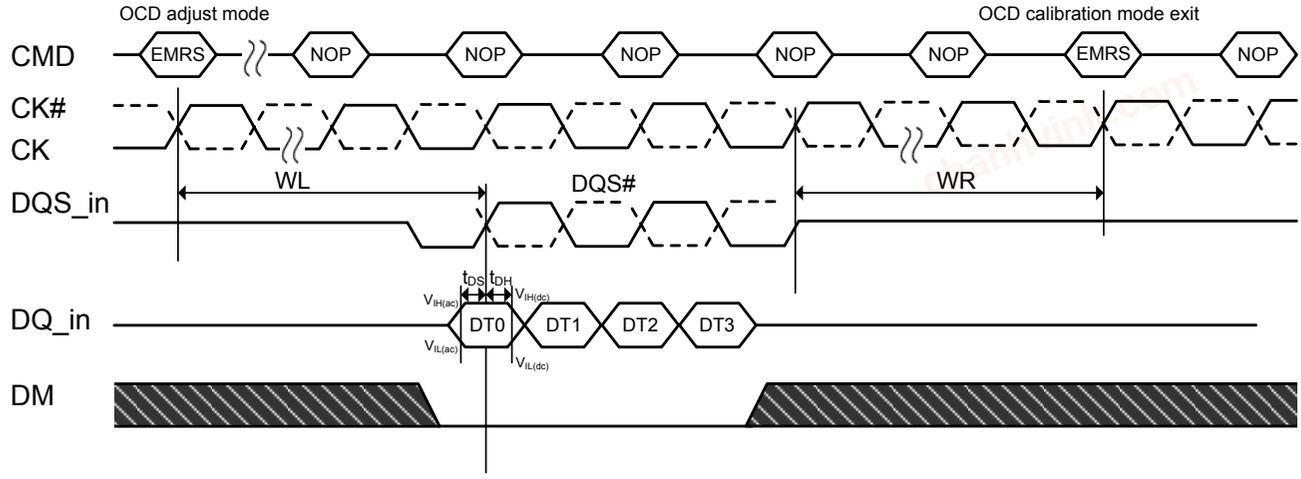
Figure 9. OCD drive mode



NOTE : Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance.In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command.

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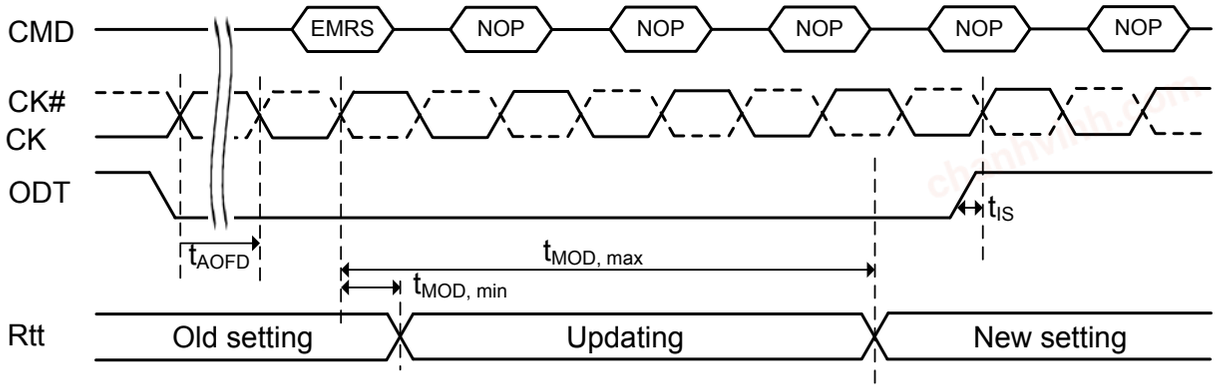
Figure 10. OCD adjust mode



NOTE 1: For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1t_{CK} and t_{DS}/t_{DH} should be met as shown in the figure.
NOTE 2: For input data pattern for adjustment, DT0-DT3 is a fixed order and is not affected by burst type (i.e., sequential or interleave)

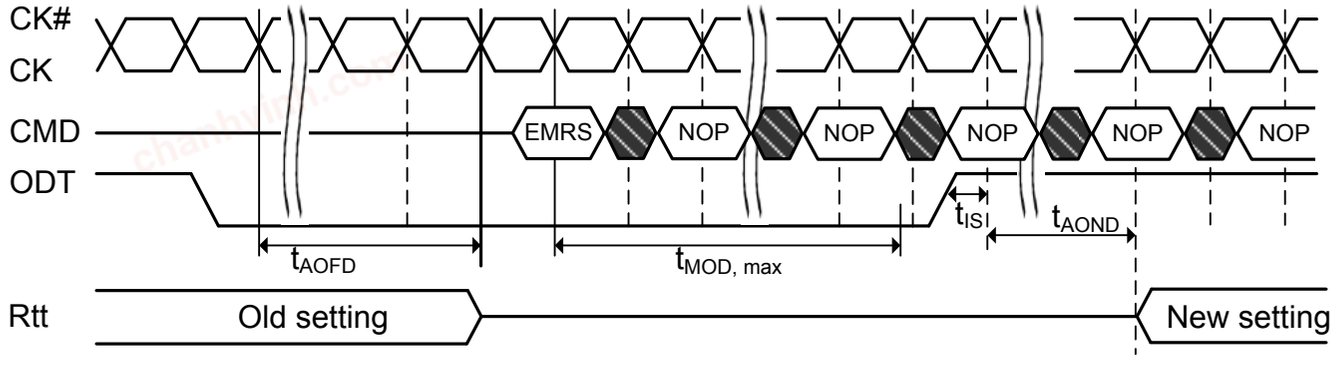
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Figure 11. ODT update delay timing-tMOD



NOTE 1: To prevent any impedance glitch on the channel, the following conditions must be met:
- t_{AOFD} must be met before issuing the EMRS command.
- ODT must remain LOW for the entire duration of t_{MOD} window, until t_{MOD}, max is met.
then the ODT is ready for normal operation with the new setting, and the ODT signal may be raised again to turned on the ODT.
NOTE 2: EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
NOTE 3: "setting" in this diagram is the Register and I/O setting, not what is measured from outside.

Figure 12. ODT update delay timing-t_{MOD}, as measured from outside



NOTE 1: EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
NOTE 2: "setting" in this diagram is measured from outside.

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Figure 13. ODT timing for active standby mode

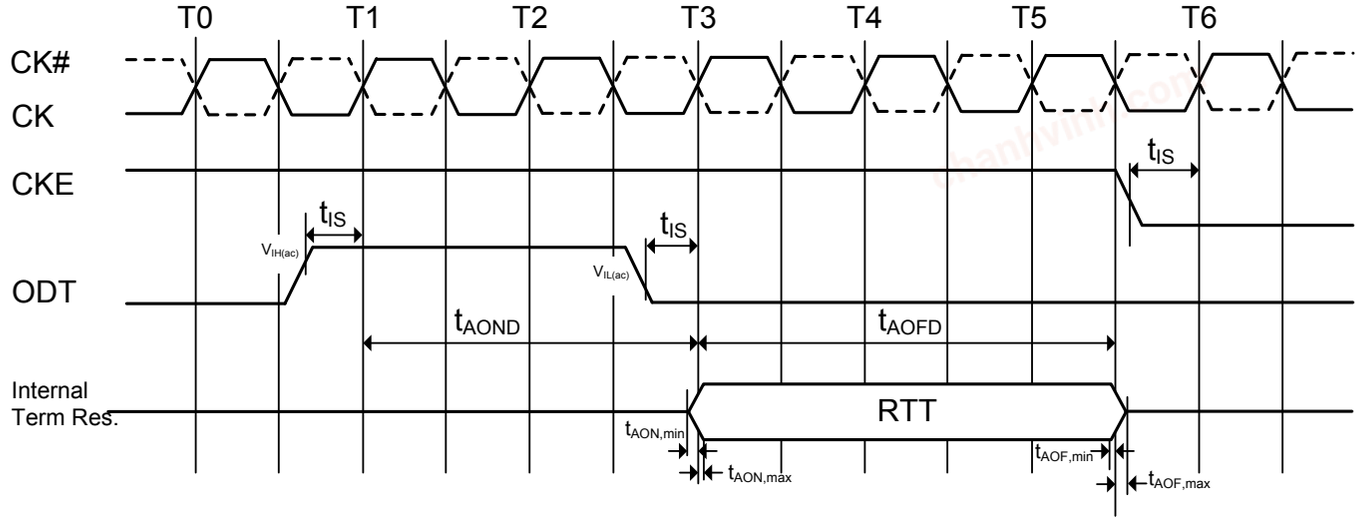
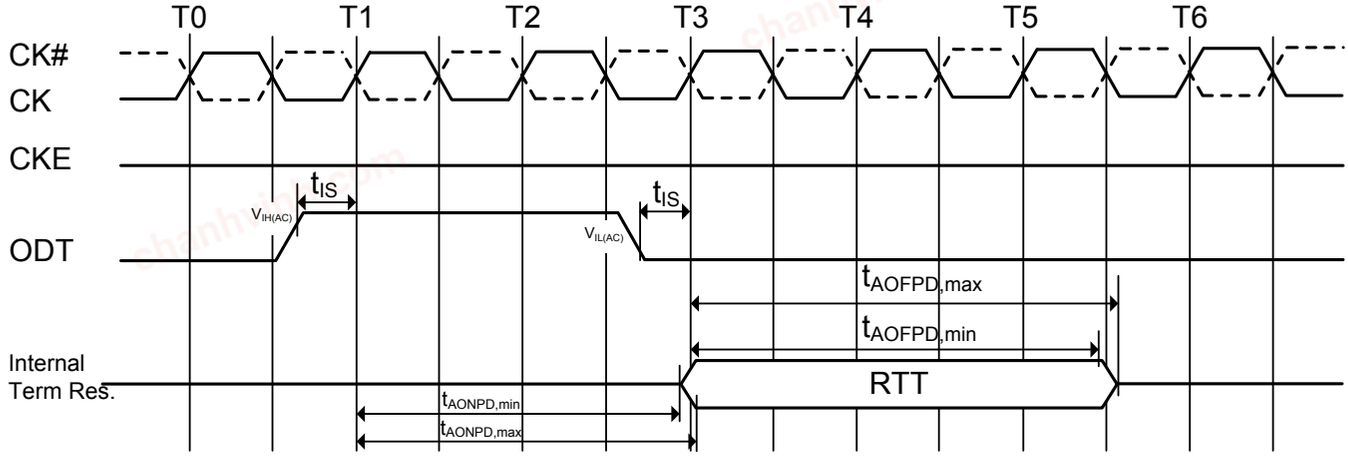
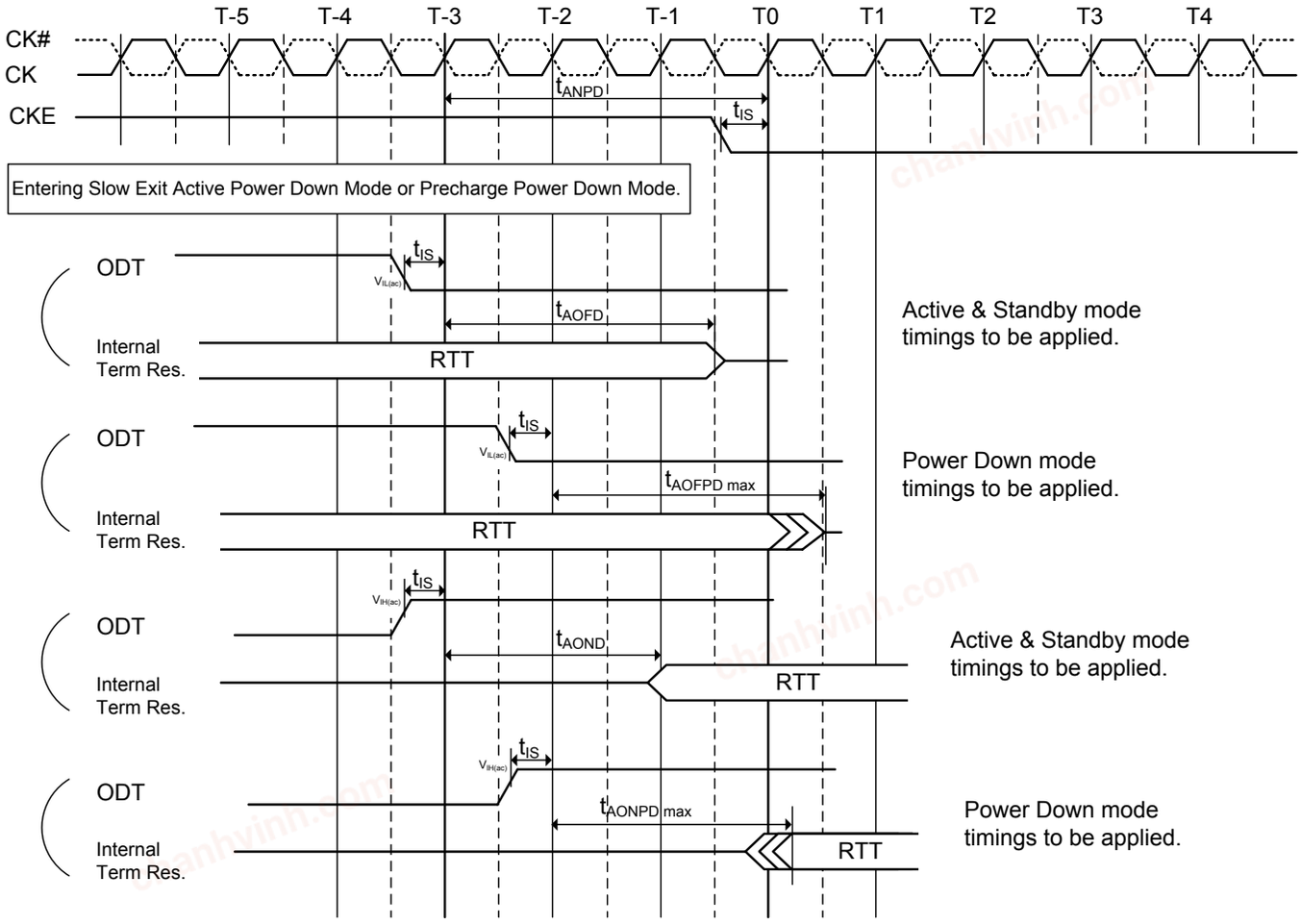


Figure 14. ODT timing for power-down mode



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Figure 15. ODT timing mode switch at entering power-down mode



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Figure 16. ODT timing mode switch at exit power-down mode

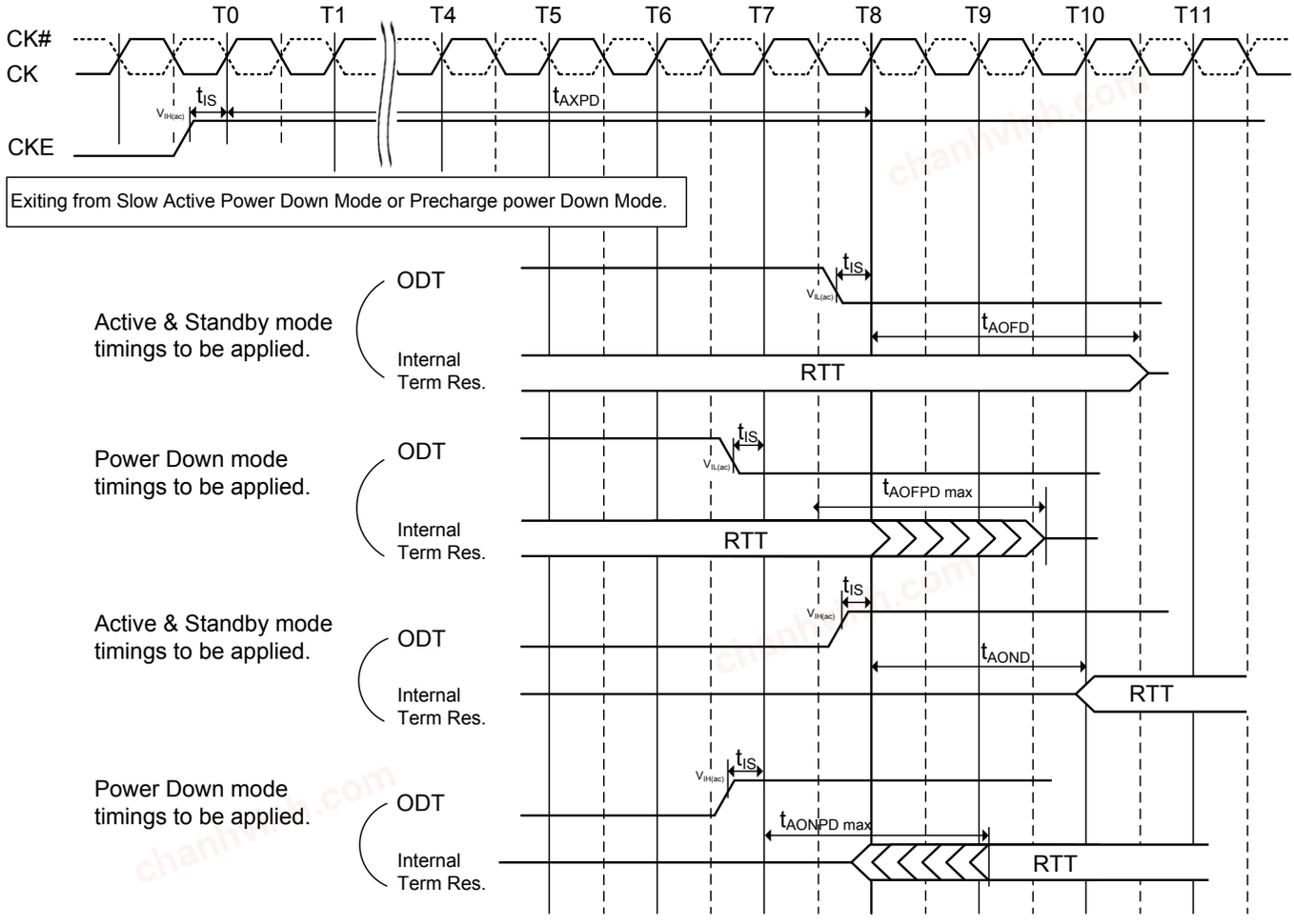
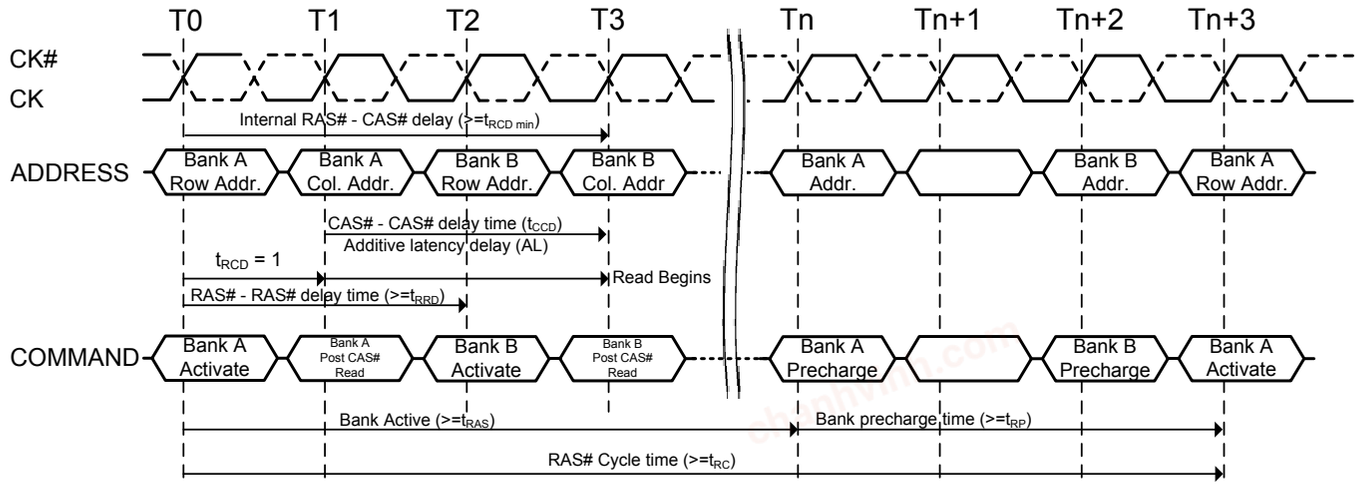
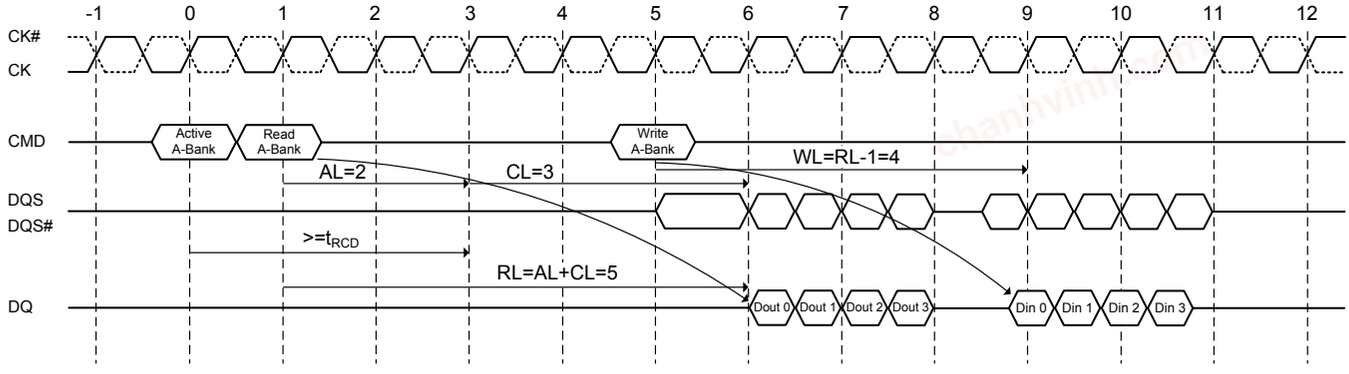


Figure 17. Bank activate command cycle (t_{RCD}=3, AL=2, t_{RP}=3, t_{RRD}=2, t_{CCD}=2)



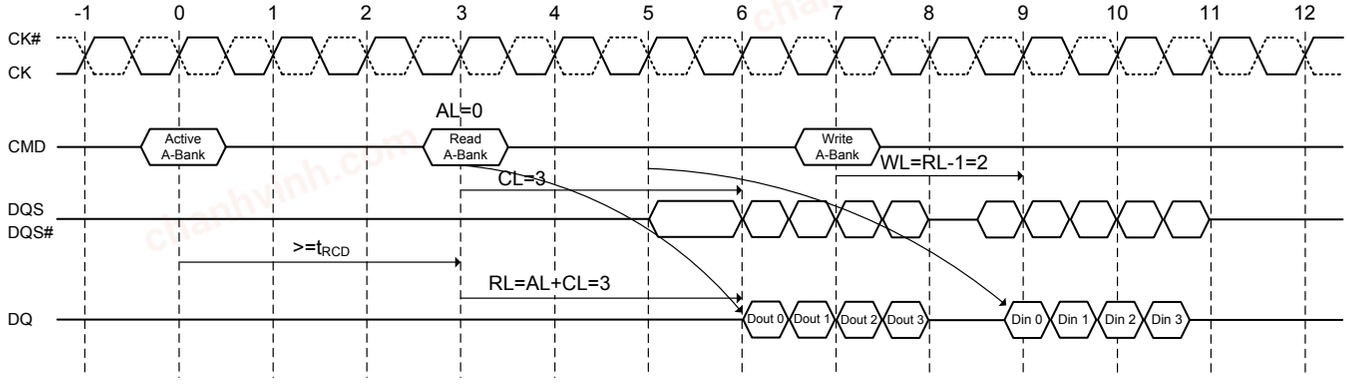
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Figure 1 8. Posted CAS# operation: AL=2
Read followed by a write to the same bank



[AL=2 and CL=3, RL= (AL+CL)=5, WL= (RL-1)=4, BL=4]

Figure 19. Posted CAS# operation: AL=0
Read followed by a write to the same bank



[AL=0 and CL=3, RL= (AL+CL)=3, WL= (RL-1)=2, BL=4]

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Figure 20. Data output (read) timing

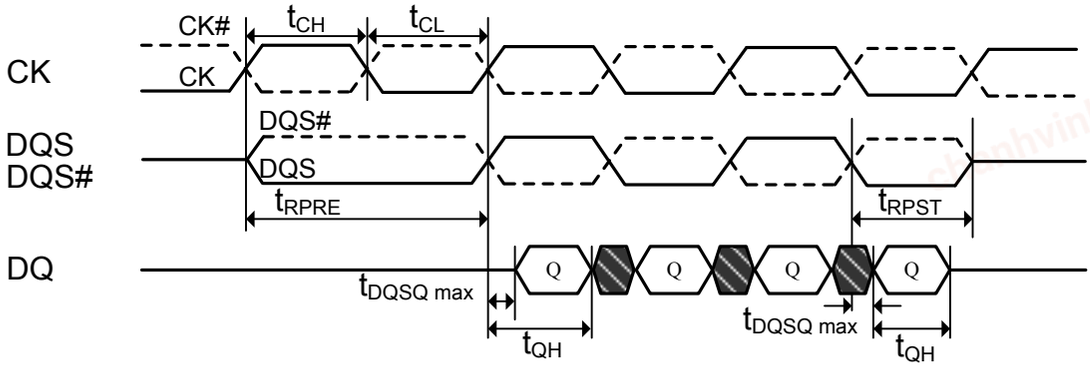


Figure 21. Burst read operation: RL=5 (AL=2, CL=3, BL=4)

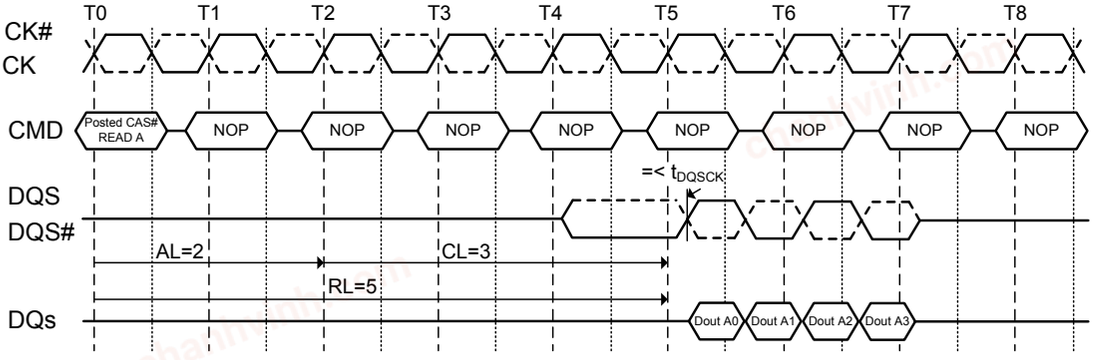
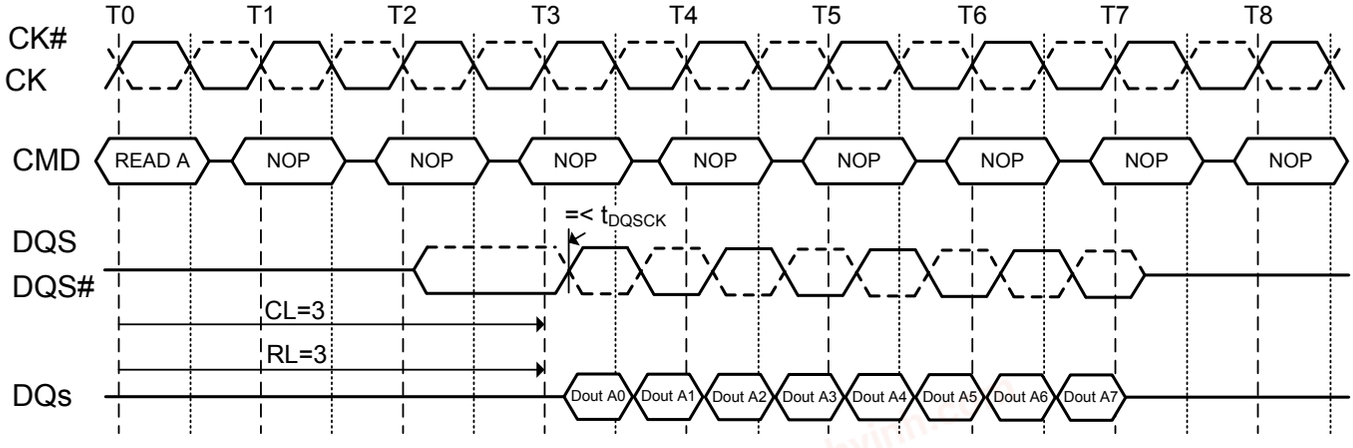
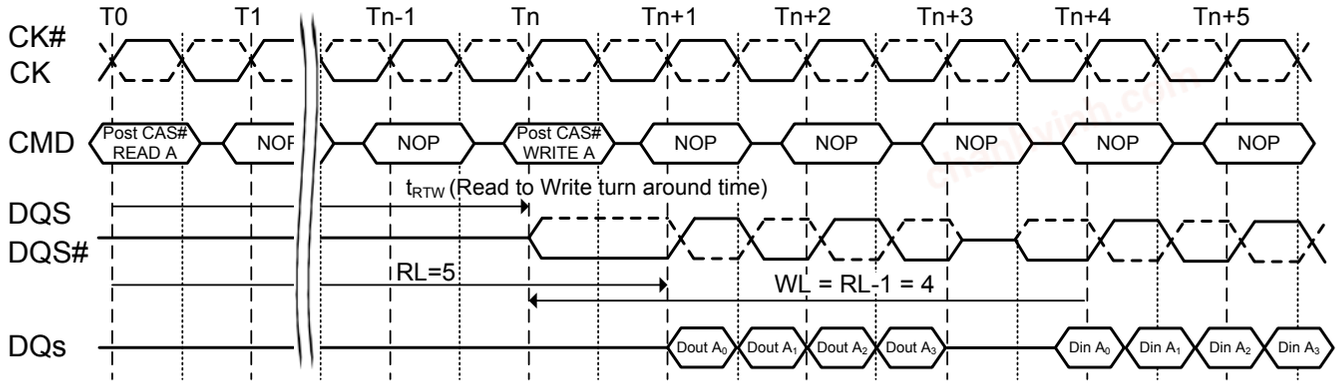


Figure 22. Burst read operation: RL=3 (AL=0, CL=3, BL=8)



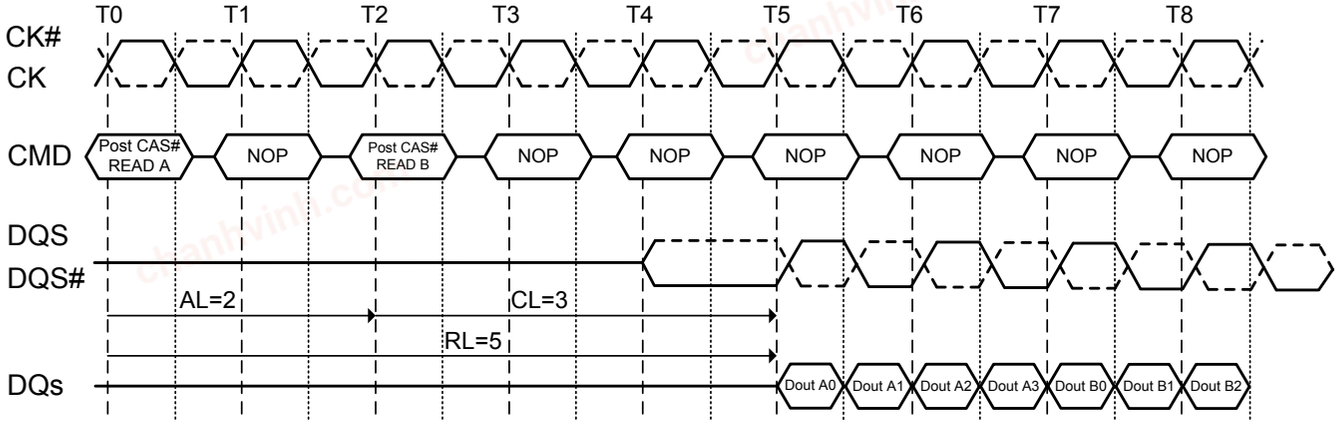
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Figure 23. Burst read followed by burst write: RL=5, WL= (RL-1) =4, BL=4



NOTE : The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

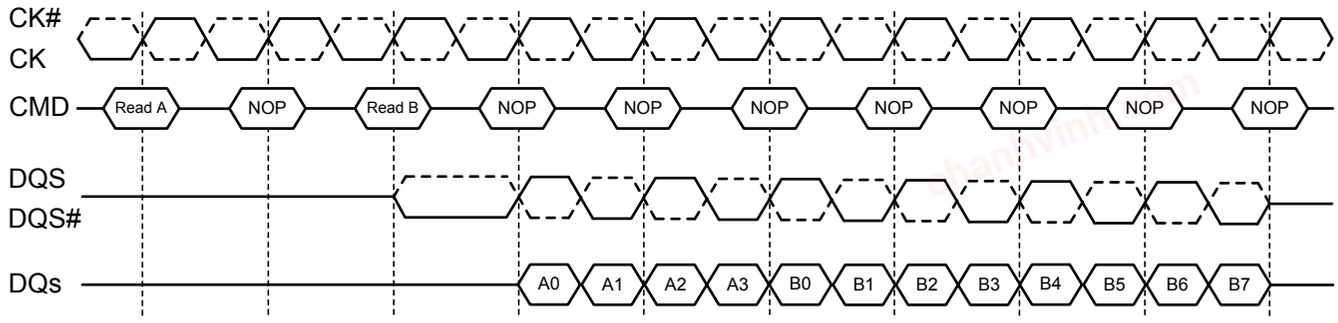
Figure 24. Seamless burst read operation: RL=5, AL=2, CL=3, BL=4



NOTE : The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL =8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

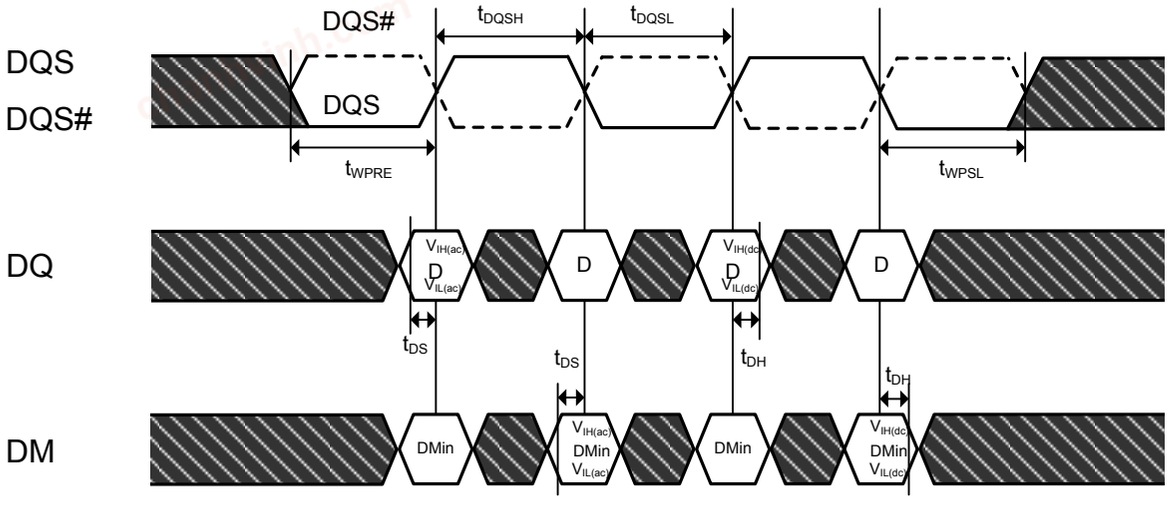
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Figure 25. Read burst interrupt timing: (CL=3, AL=0, RL=3, BL=8)



NOTE 1: Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
NOTE 2: Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
NOTE 3: Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
NOTE 4: Read burst interruption is allowed to any bank inside DRAM.
NOTE 5: Read burst with Auto Precharge enabled is not allowed to interrupt.
NOTE 6: Read burst interruption is allowed by another Read with Auto Precharge command.
NOTE 7: All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL+BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

Figure 26. Data input (write) timing



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Figure 27. Burst write operation: RL=5 (AL=2, CL=3), WL=4, BL=4

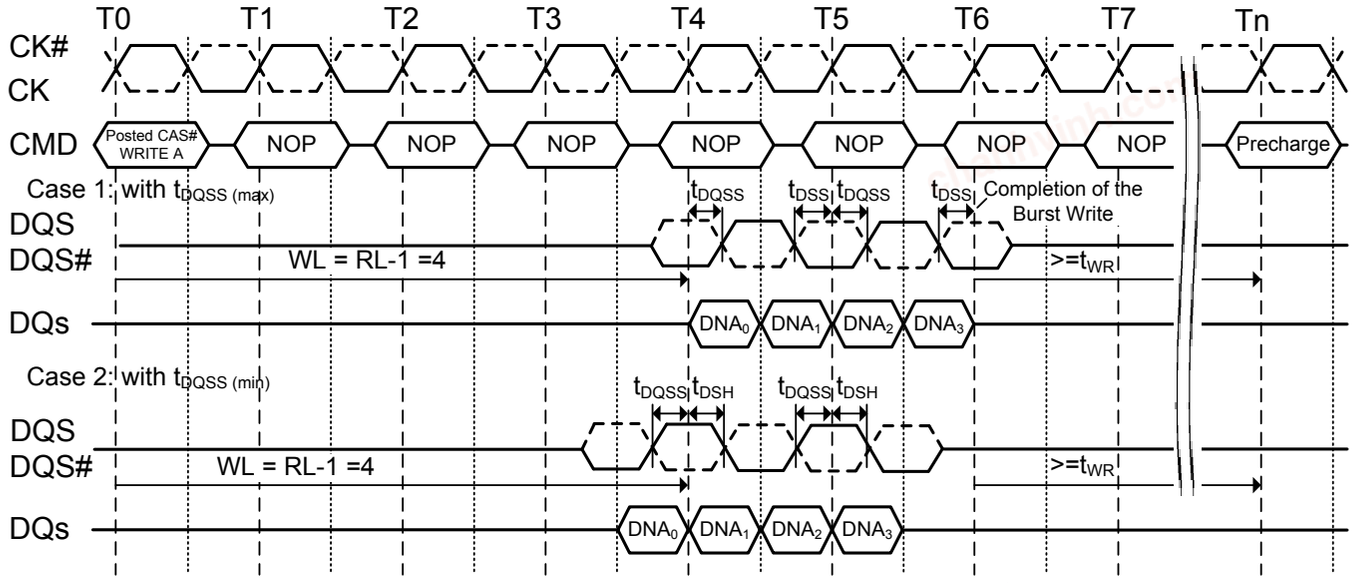
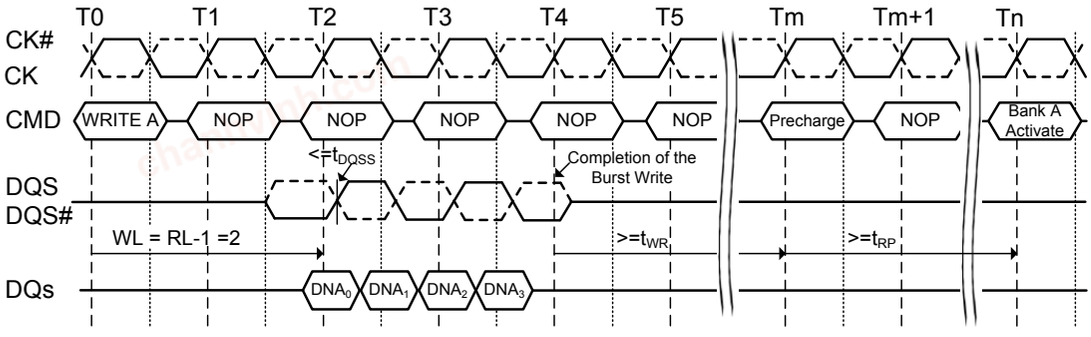
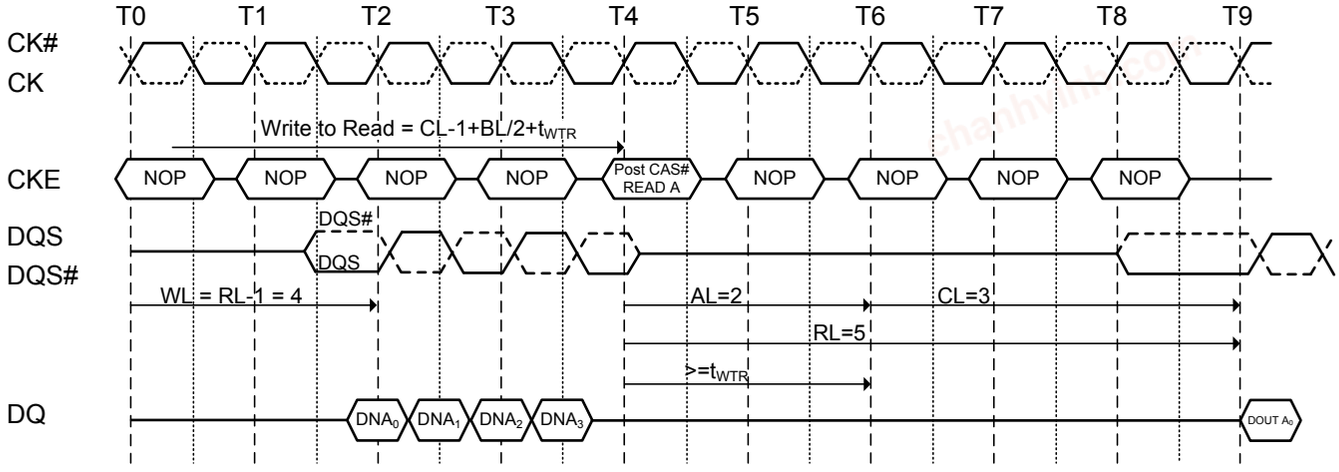


Figure 28. Burst write operation: RL=3 (AL=0, CL=3), WL=2, BL=4



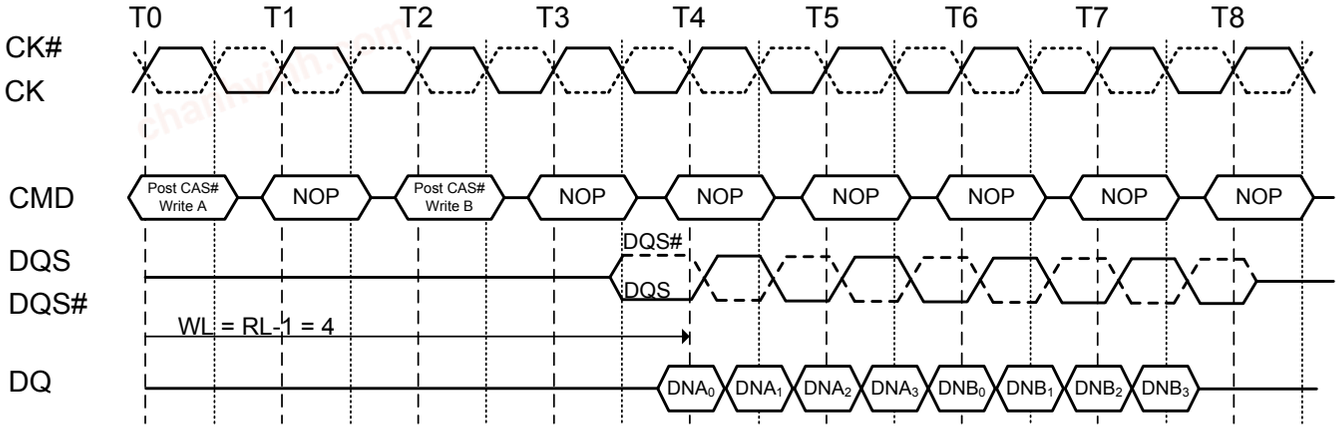
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Figure 29. Burst write followed by burst read: RL=5 (AL=2, CL=3, WL=4, t_{WTR}=2, BL=4)



NOTE : The minimum number of clock from the burst write command to the burst read command is [CL-1 + BL/2 + t_{WTR}]. This t_{WTR} is not a write recovery time (t_{WR}) but the time required to transfer the 4 bit write data from the input buffer into sense amplifiers in the array. t_{WTR} is defined in the timing parameter table of this standard.

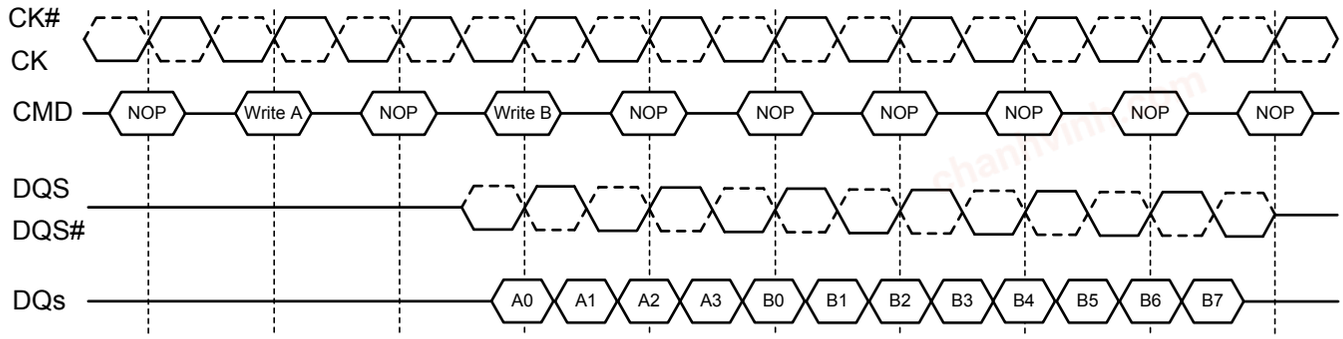
Figure 30. Seamless burst write operation RL=5, WL=4, BL=4



NOTE : The seamless burst write operation is supported by enabling a write command every other clock for BL= 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

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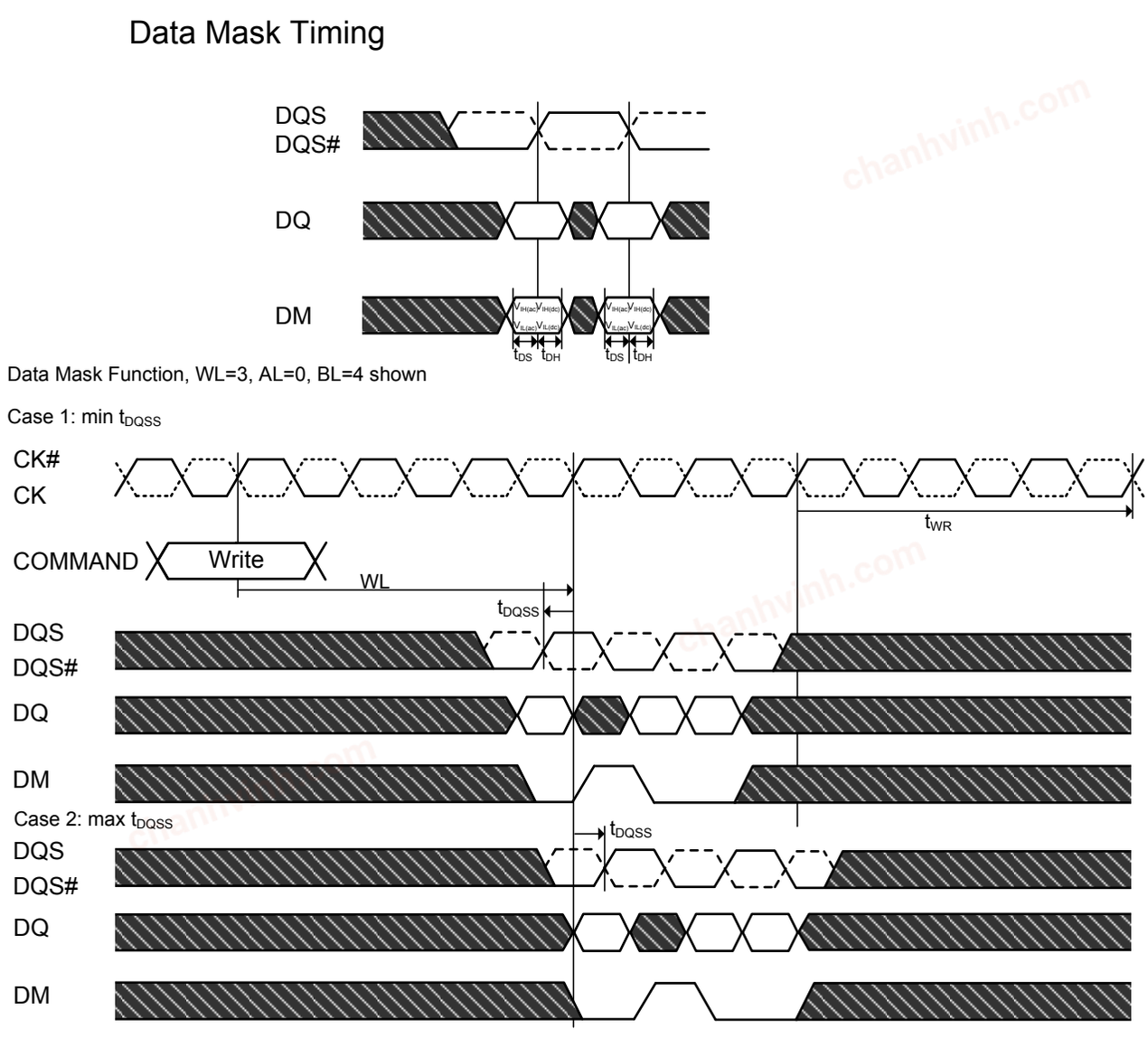
Figure 31. Write burst interrupt timing: (CL=3, AL=0, RL=3, WL=2, BL=8)



NOTE 1: Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
NOTE 2: Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.
NOTE 3: Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.
NOTE 4: Write burst interruption is allowed to any bank inside DRAM.
NOTE 5: Write burst with Auto Precharge enabled is not allowed to interrupt.
NOTE 6: Write burst interruption is allowed by another Write with Auto Precharge command.
NOTE 7: All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL + BL/2 + tWR where tWR starts with the rising clock after the uninterrupted burst end and not from the end of actual burst end.

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Figure 32. Write data mask



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Figure 33. Burst read operation followed by precharge: (RL=4, AL=1, CL=3, BL=4, $t_{RTP} \leqq 2$ clocks)

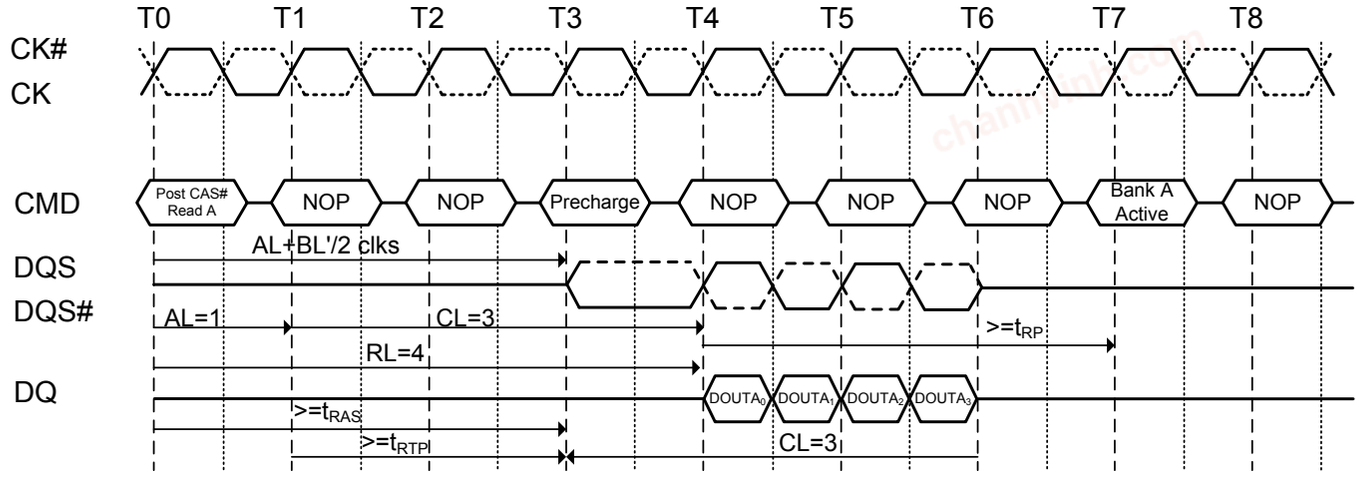
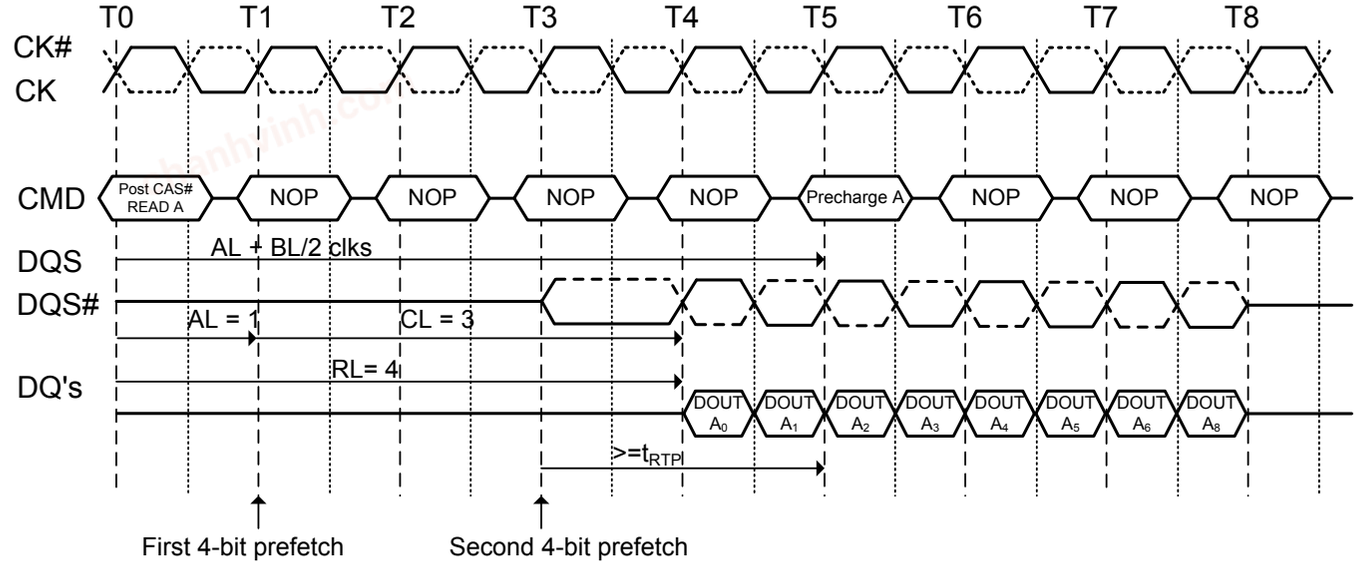


Figure 34. Burst read operation followed by precharge: (RL=4, AL=1, CL=3, BL=8, $t_{RTP} \leqq 2$ clocks)



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Figure 35. Burst read operation followed by precharge: (RL=5, AL=2, CL=3, BL=4, $t_{RTP} \leqq 2$ clocks)

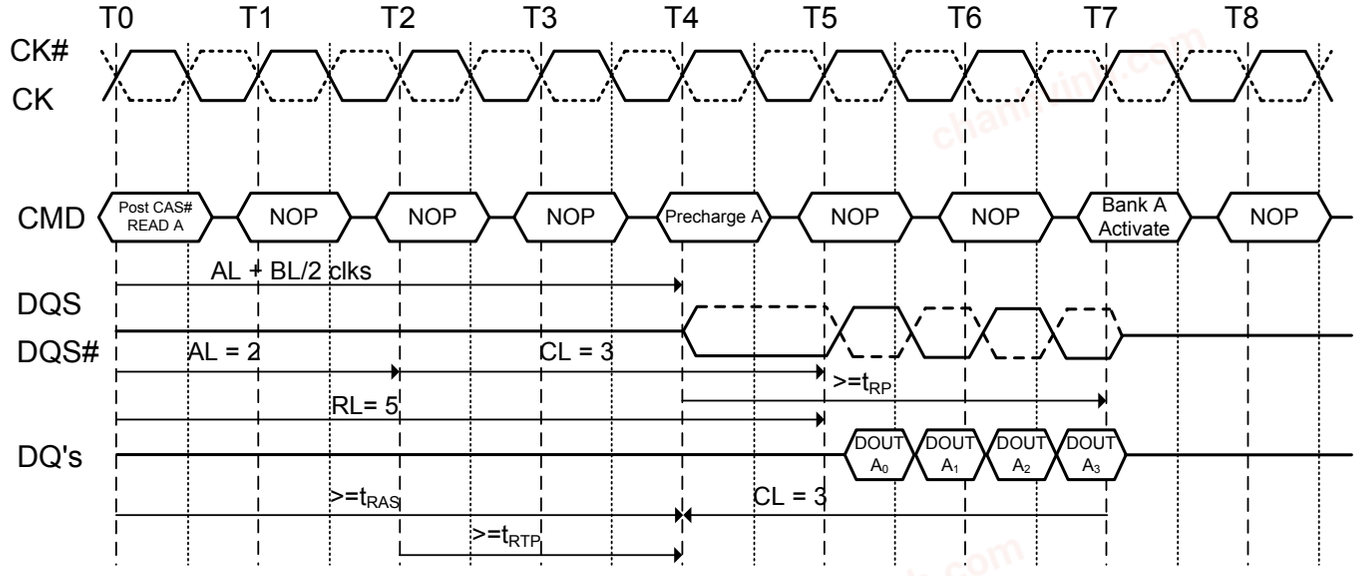
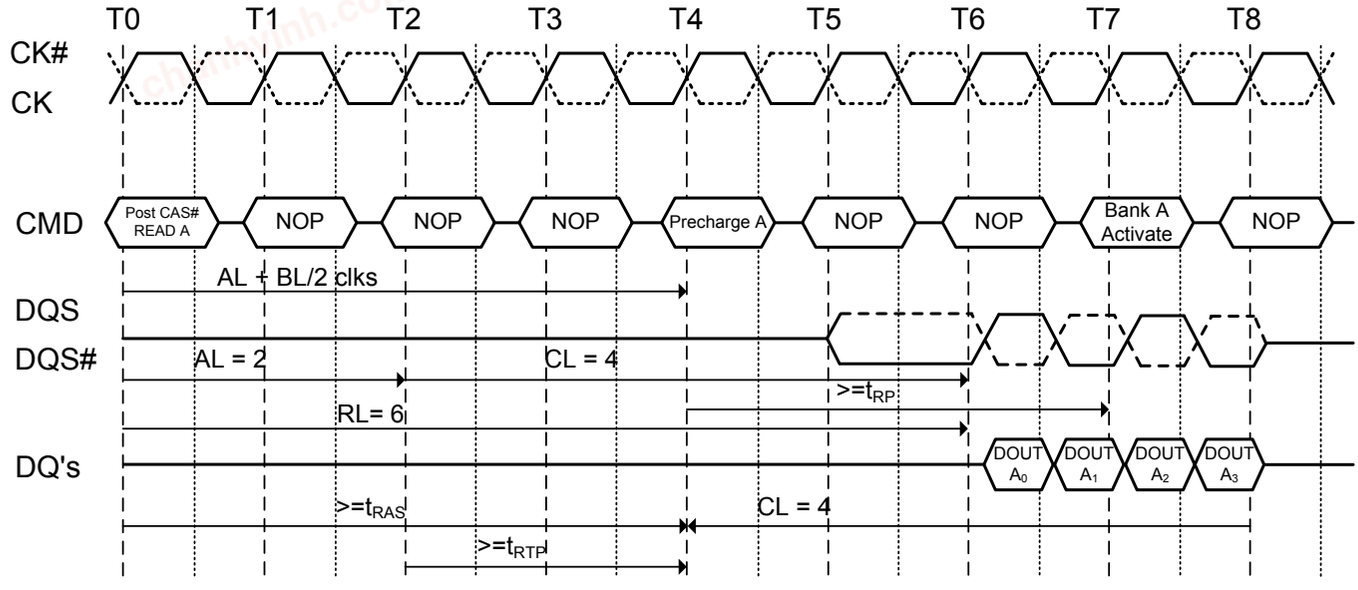
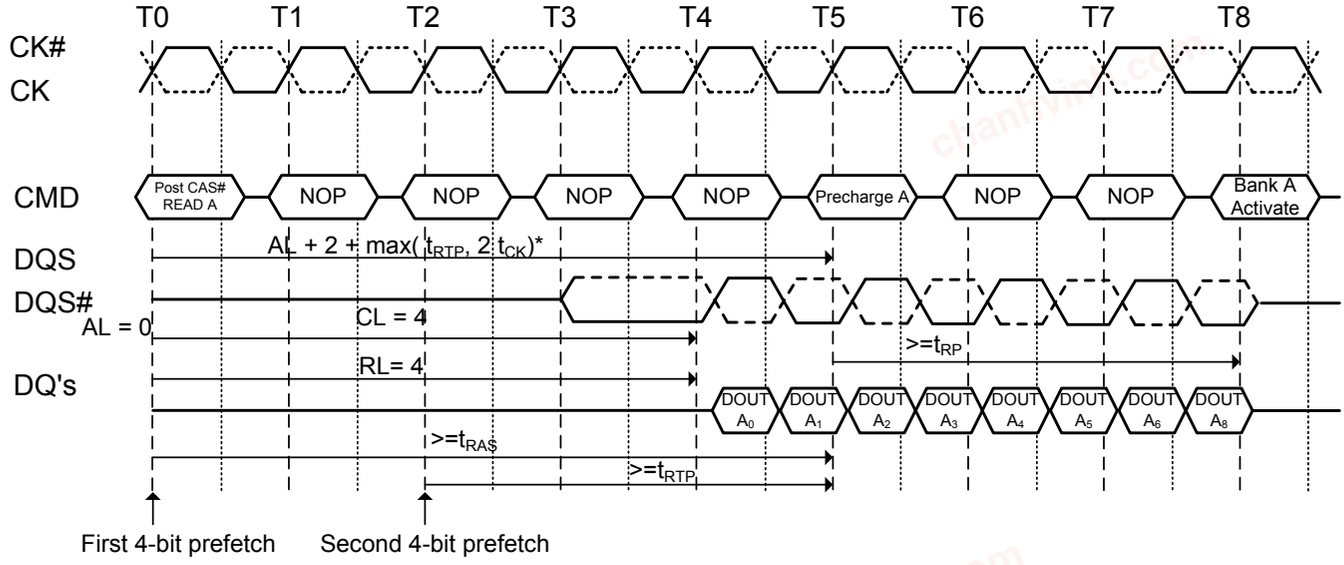


Figure 36. Burst read operation followed by precharge: (RL=6, AL=2, CL=4, BL=4, $t_{RTP} \leqq 2$ clocks)



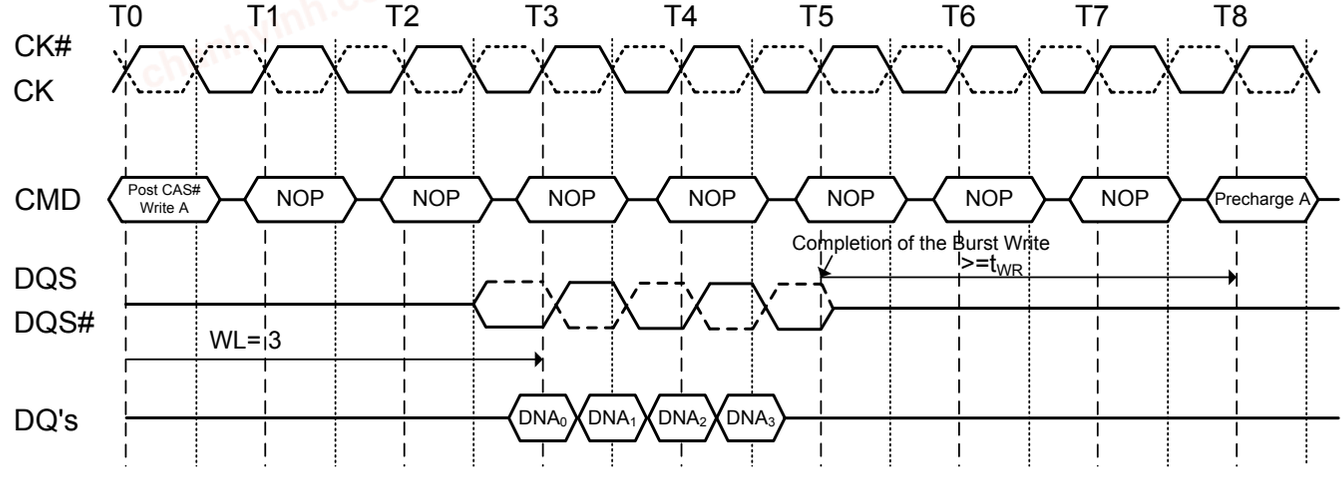
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Figure 37. Burst read operation followed by precharge: (RL=4, AL=0, CL=4, BL=8, t_{RTP}>2 clocks)



*: rounded to next integer.

Figure 38. Burst write operation followed by precharge: WL= (RL-1) =3



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Figure 39. Burst write followed by precharge: WL= (RL-1) =4

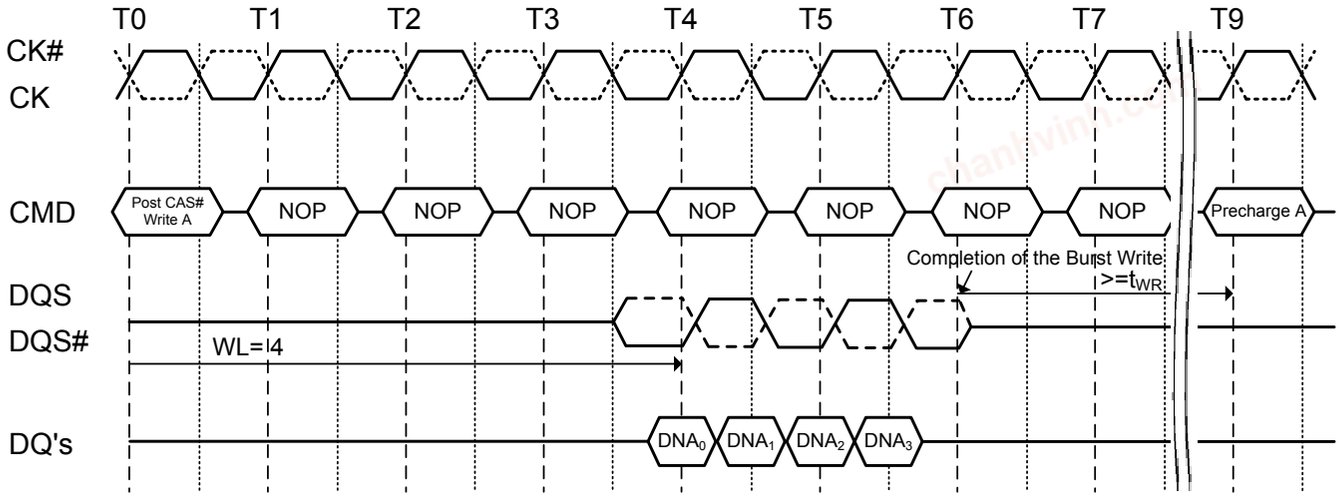
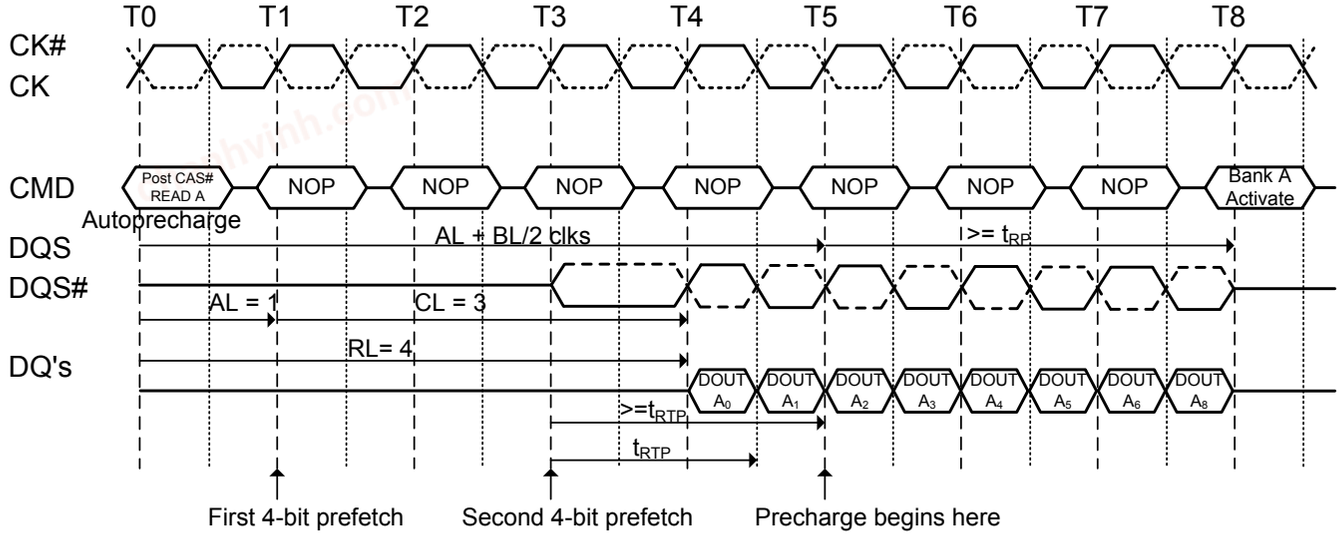


Figure 40. Burst read operation with auto precharge:
(RL=4,AL=1, CL=3, BL=8, t_{RTP}≦2 clocks)



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Figure 41. Burst read operation with auto precharge: (RL=4, AL=1, CL=3, BL=4, t_{RTP}>2 clocks)

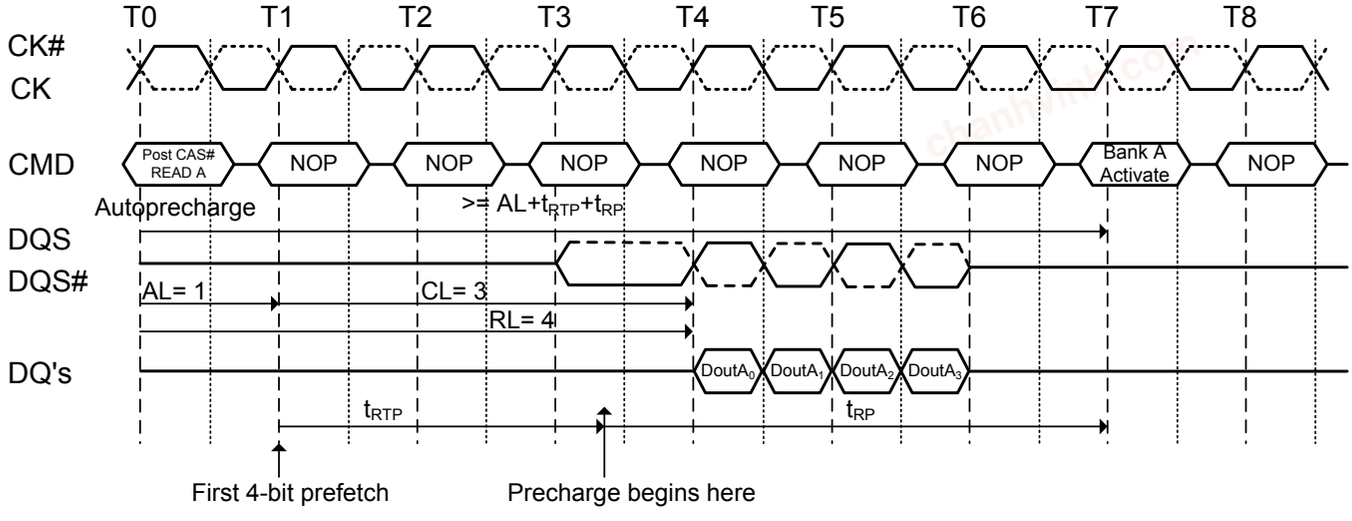
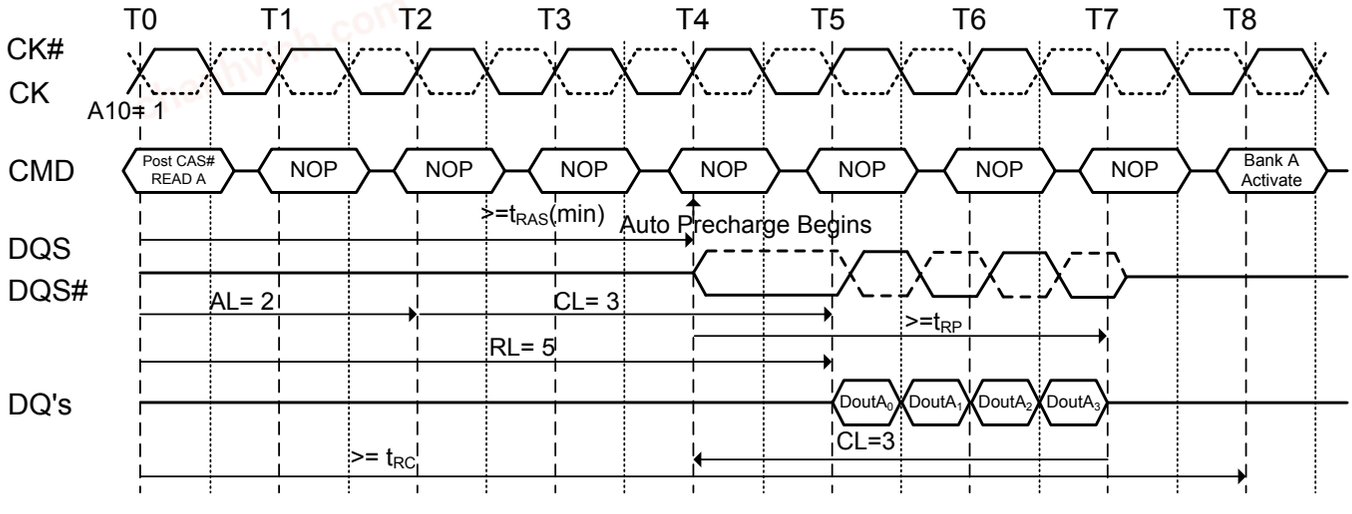


Figure 42. Burst read operation with auto precharge followed by activation to the same bank (t_{RC} Limit): RL=5(AL=2, CL=3, internal t_{RCD}=3, BL=4, t_{RTP}≦2 clocks)



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Figure 43. Burst read operation with auto precharge followed by an activation to the same bank (t_{RP} Limit): (RL=5 (AL=2, CL=3, internal t_{RCD}=3, BL=4, t_{RTP}≦2 clocks)

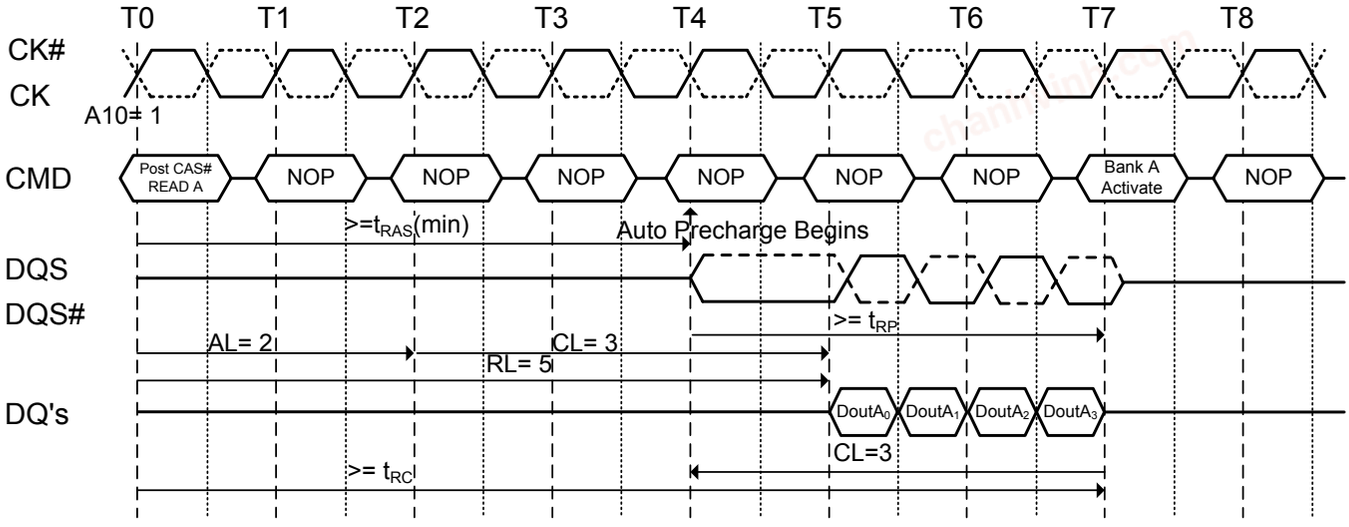
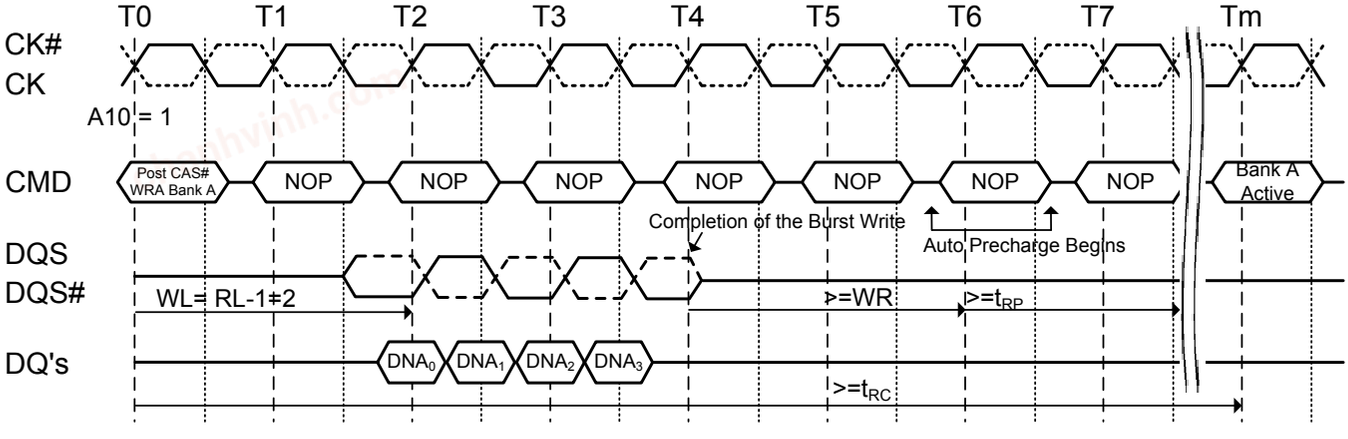


Figure 44. Burst write with auto-precharge (t_{RC} Limit): WL=2, WR=2, BL=4, t_{RP}=3



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Figure 45. Burst write with auto-precharge (WR+t_{RP}): WL=4, WR=2, BL=4, t_{RP}=3

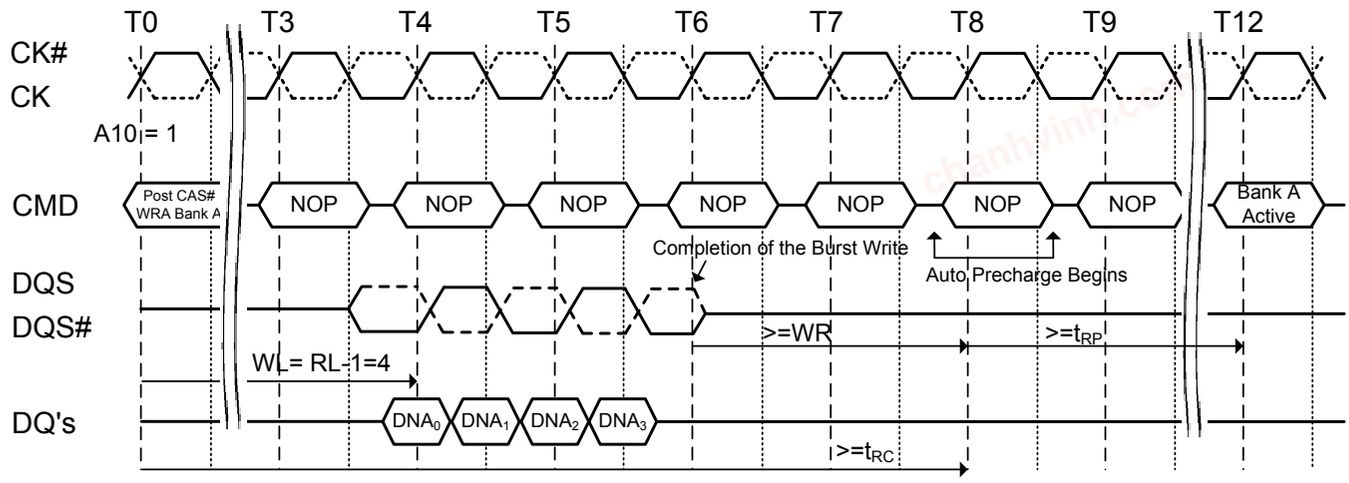
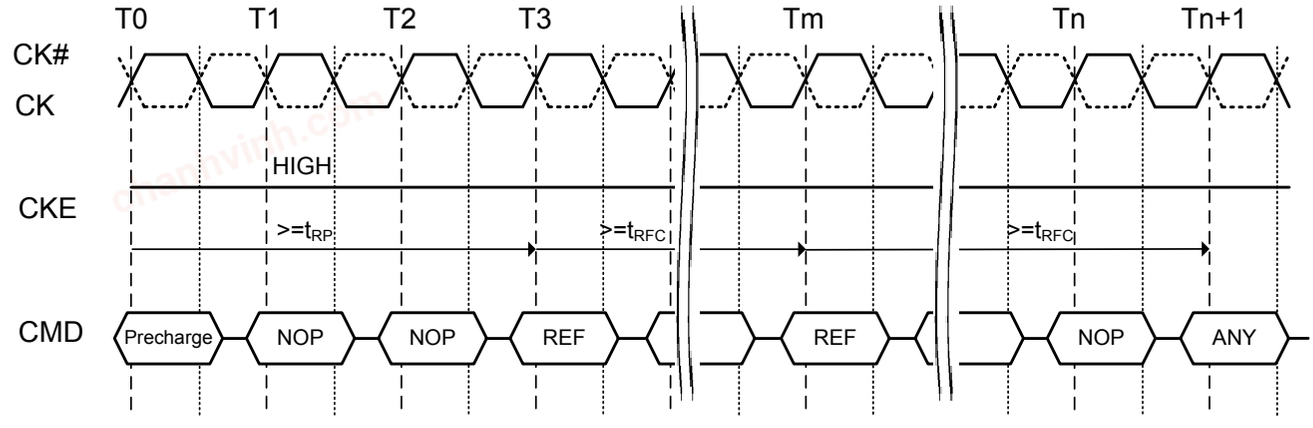
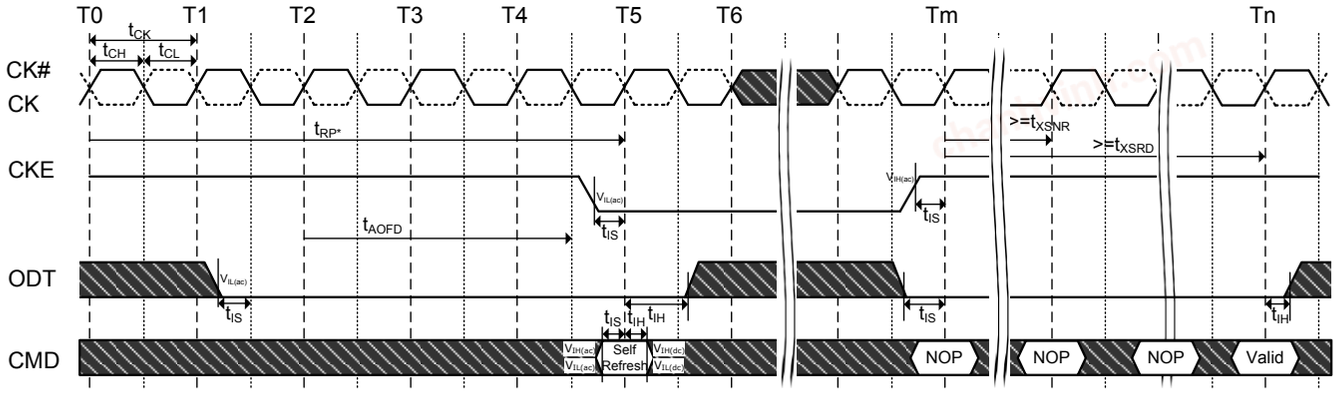


Figure 46. Refresh command



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Figure 47. Self refresh operation



NOTE 1 Device must be in the "All banks idle" state prior to entering Self Refresh mode.

NOTE 2 ODT must be turned off t_{AOFD} before entering Self Refresh mode, and can be turned on again when t_{XSRD} timing is satisfied.

NOTE 3 t_{XSRD} is applied for Read or a Read with autoprecharge command.

t_{XSNR} is applied for any command except a Read or a Read with autoprecharge command.

Figure 48. Basic power down entry and exit timing diagram

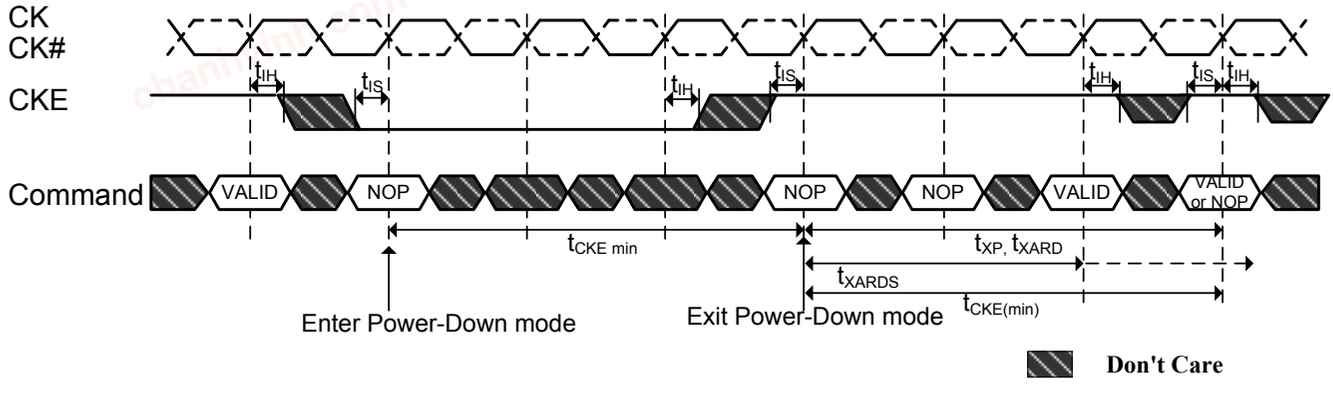
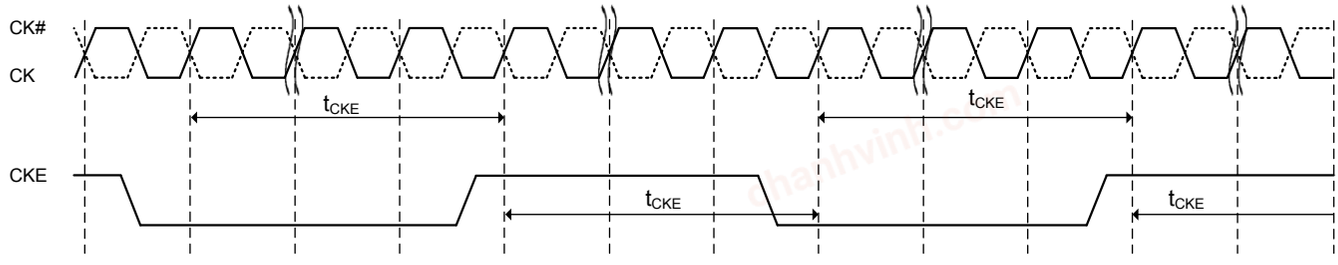


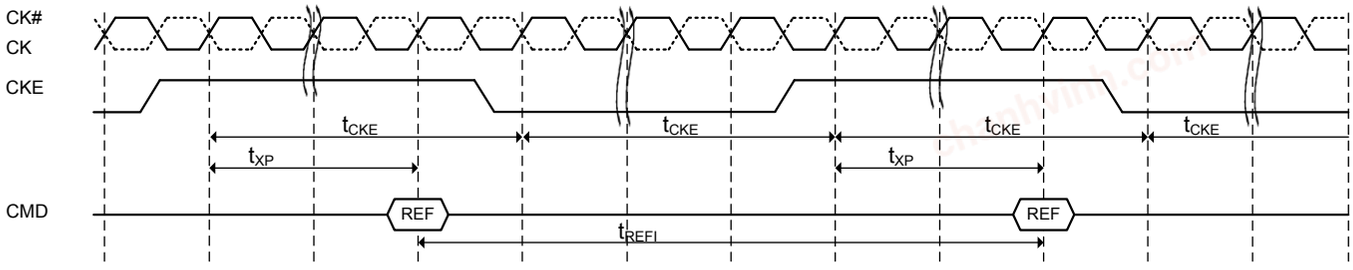
Figure 49. CKE intensive environment



NOTE: DRAM guarantees all AC and DC timing & voltage specifications and proper DLL operation with intensive CKE operation

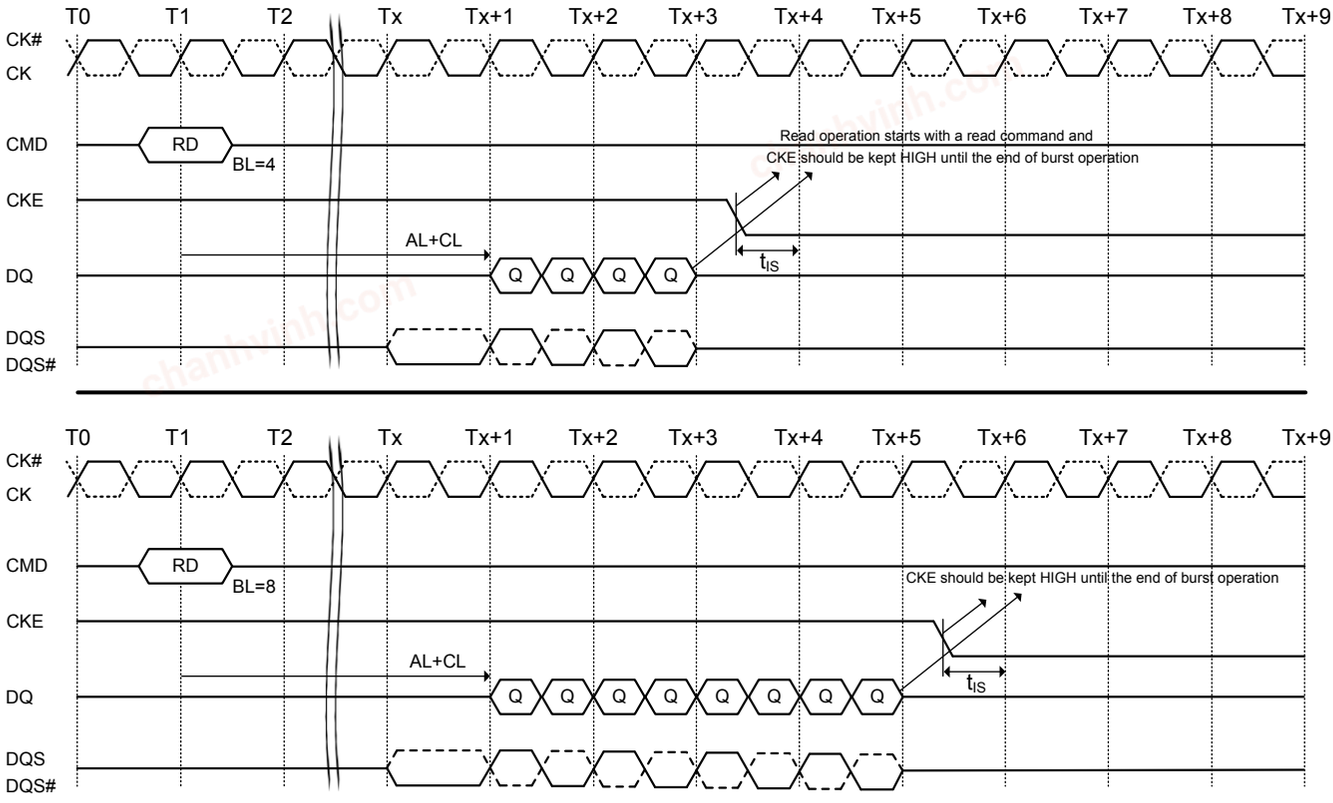
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Figure 50. CKE intensive environment



NOTE: The pattern shown above can repeat over a long period of time. With this pattern, DRAM guarantees all AC and DC timing & voltage specifications and DLL operation with temperature and voltage drift

Figure 51. Read to power-down entry



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Figure 52. Read with autoprecharge to power-down entry

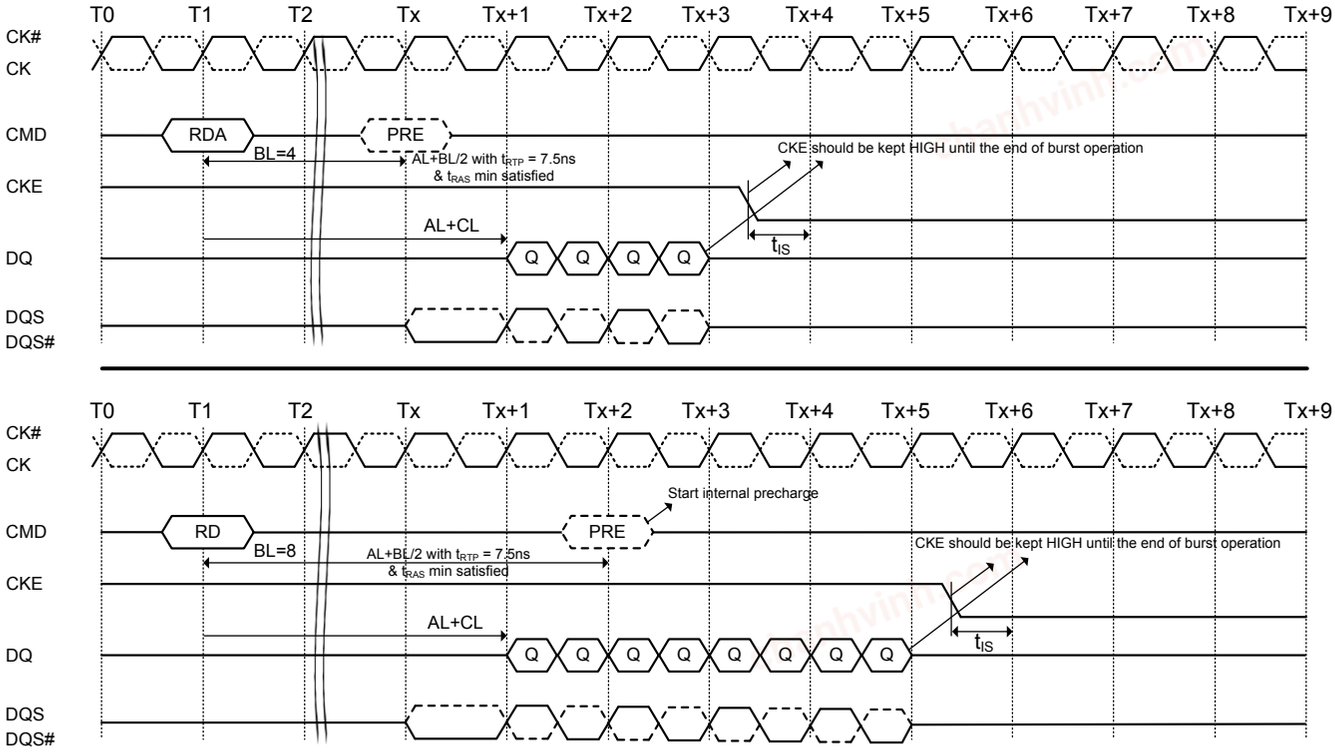
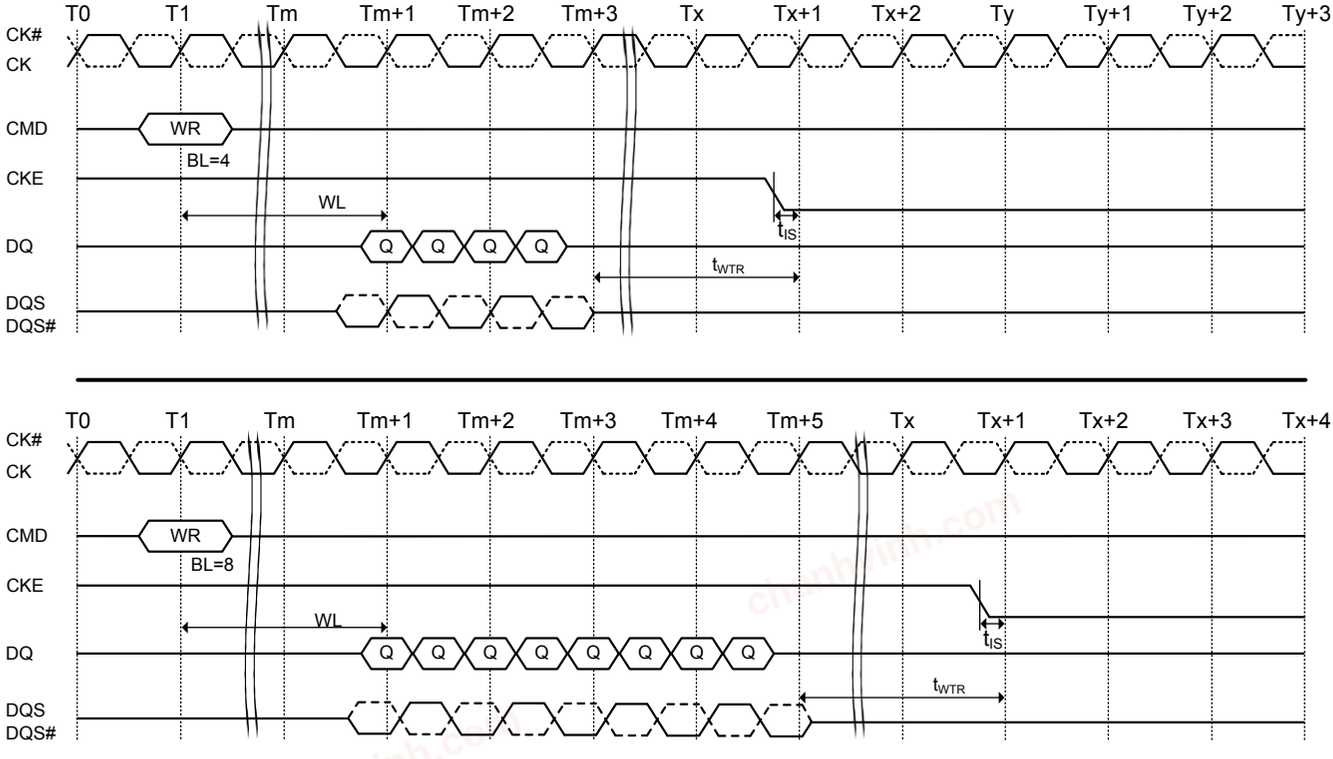


Figure 53. Write to power-down entry



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Figure 54. Write with autoprecharge to power-down entry

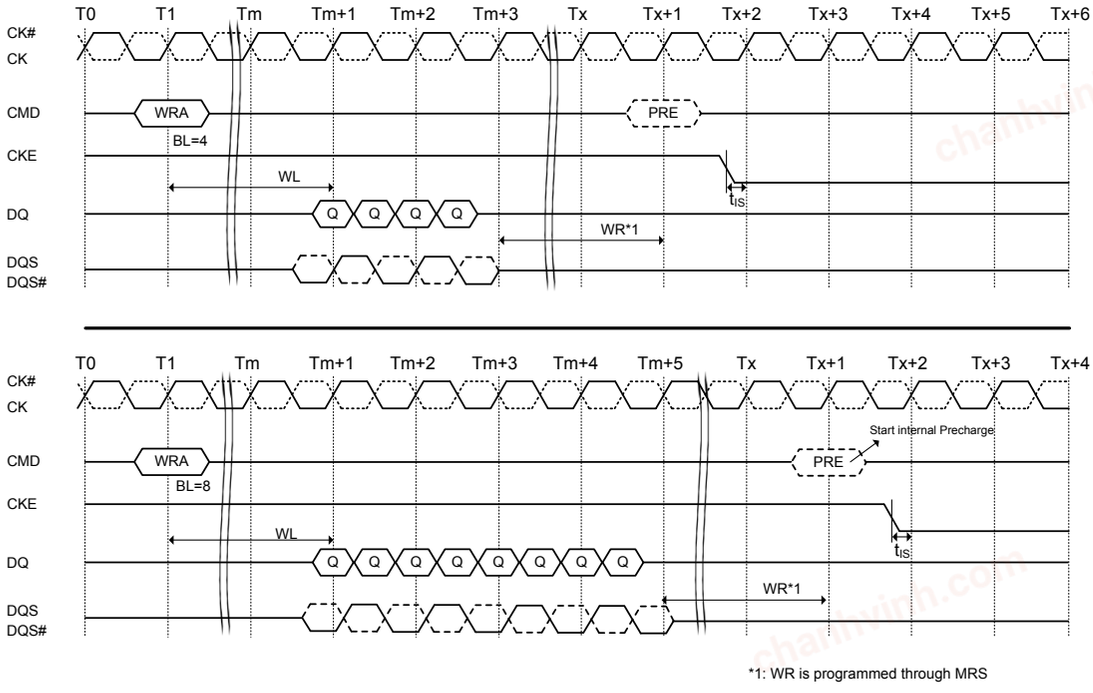


Figure 55. Refresh command to power-down entry

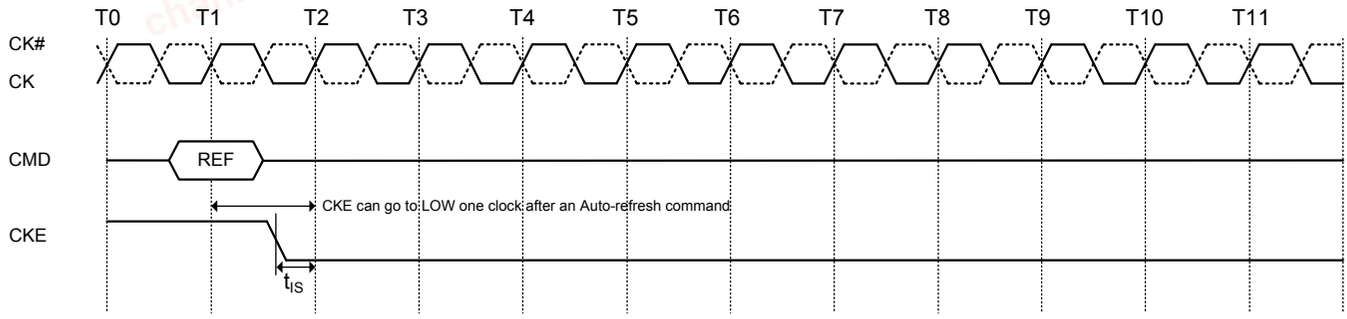
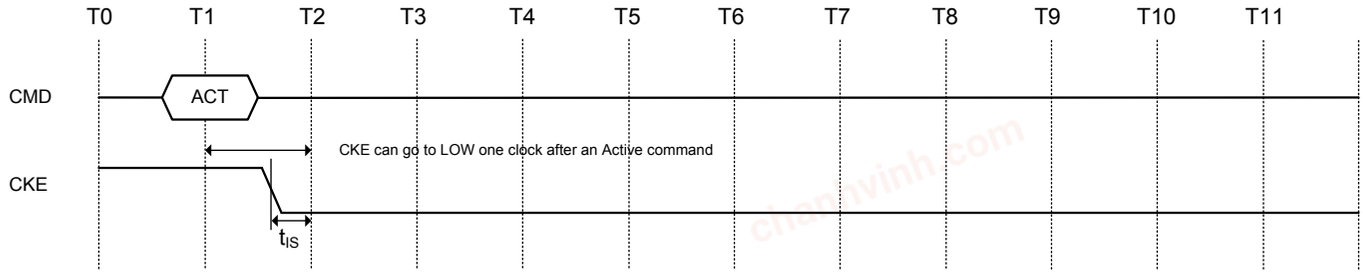


Figure 56. Active command to power-down entry



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Figure 57. Precharge/precharge-all command to power-down entry

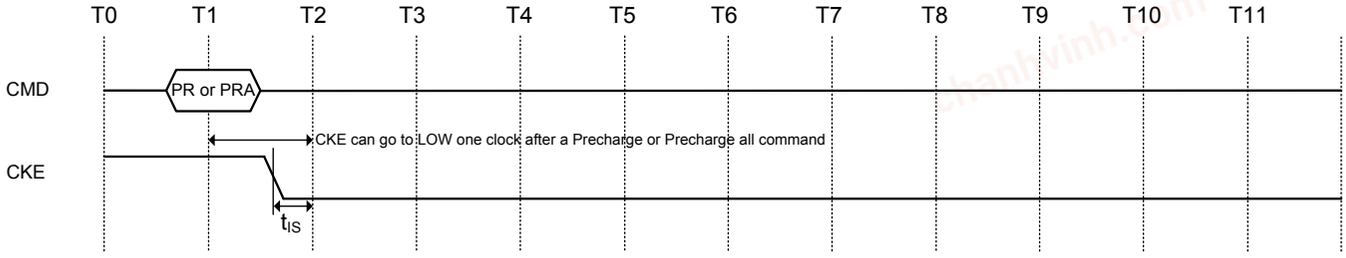


Figure 58. MRS/EMRS command to power-down entry

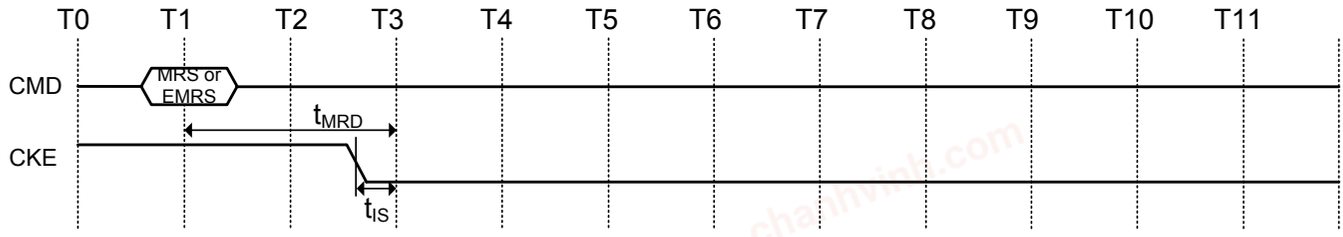


Figure 59. Asynchronous CKE LOW event

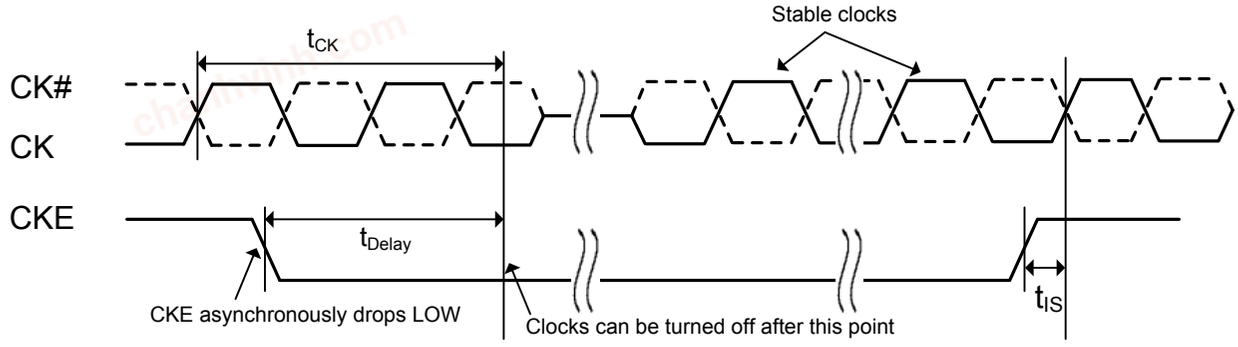
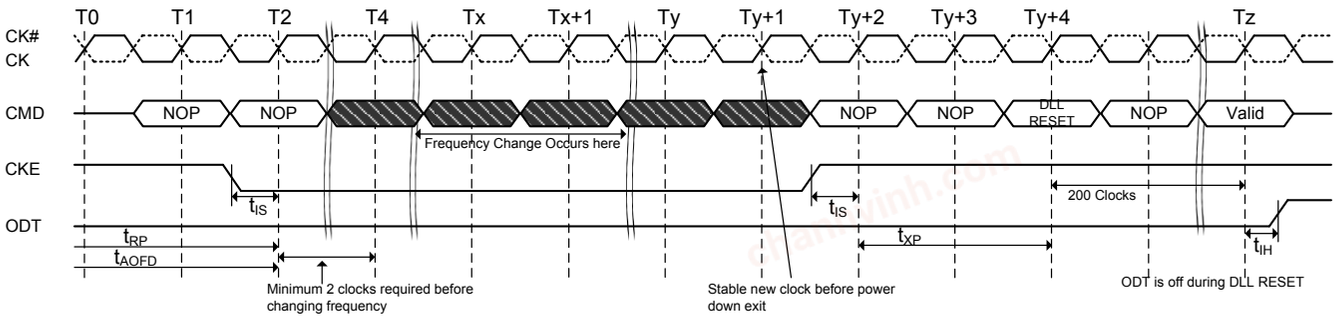
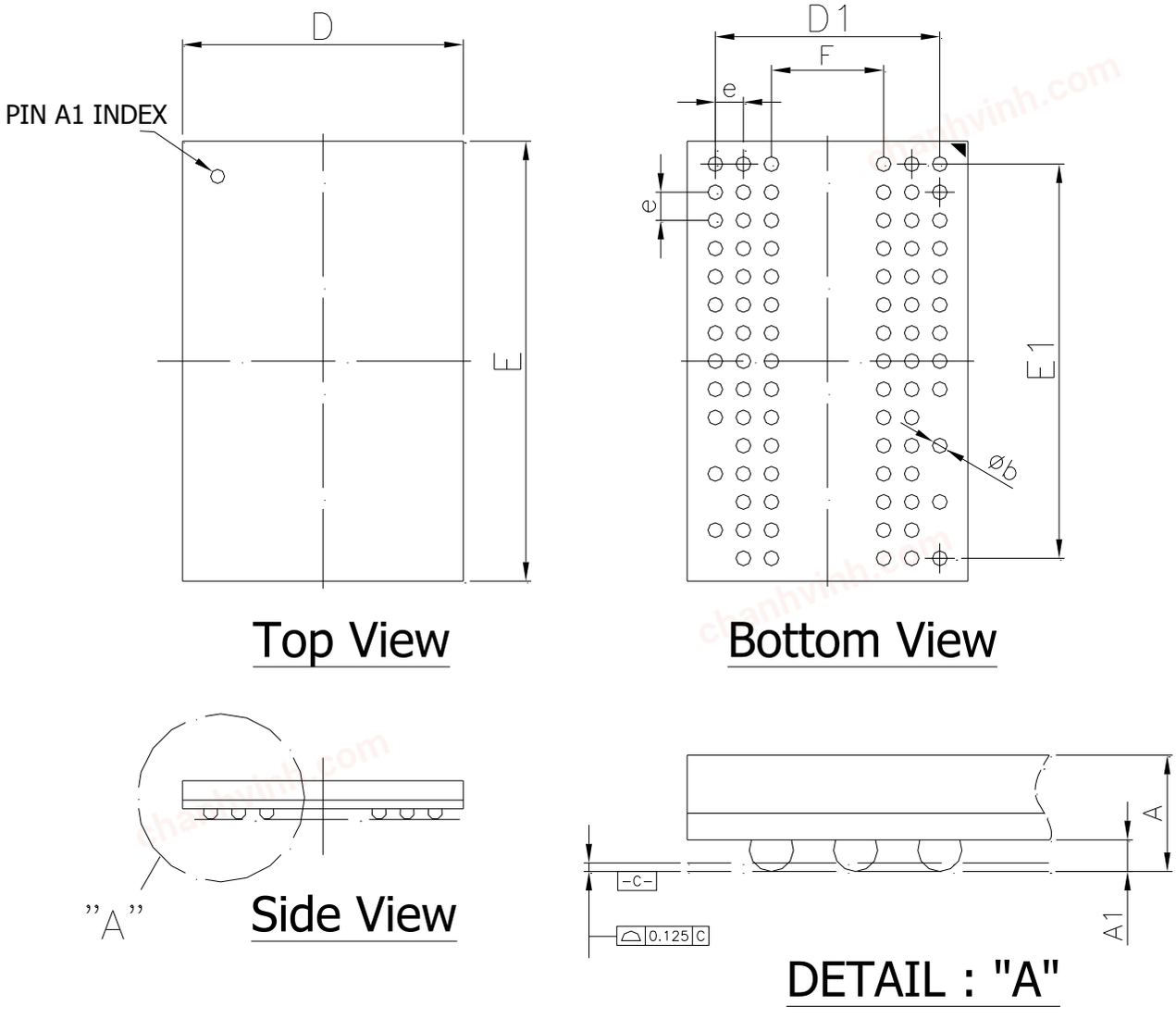


Figure 60. Clock frequency change in precharge power down mode



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Figure 61. 84-Ball TFBGA Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.010	--	0.016	0.25	--	0.40
D	0.311	0.315	0.319	7.9	8.0	8.1
E	0.488	0.492	0.496	12.4	12.5	12.6
D1	--	0.252	--	--	6.40	--
E1	--	0.441	--	--	11.2	--
F	--	0.126	--	--	3.2	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50

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PART NUMBERING SYSTEM

AS4C	128M16D2A	25	B	C/I	N
DRAM	128M16=128Mx16 D2=DDR2 A=A Die	25=400MHz	B = FBGA	C=Commercial (0° C～85° C) I=Industrial (-40° C～95° C)	Indicates Pb and Halogen Free

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Fax: 650-620-9211
www.alliancememory.com

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